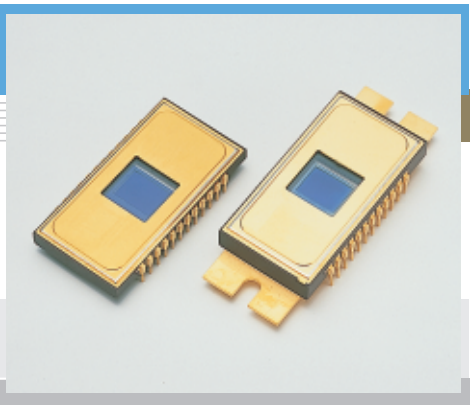

CCD area image sensor
S7986-01, S7987-01

Back-thinned FT-CCD for low-light-level NTSC B/W TV application

The S7986-01 and S7987-01 are a family of FT-CCD area image sensors specifically designed for high speed operation. A high frame rate is attained by employing a wide band width on-chip amplifier. In area scan operation, The S7986-01 and S7987-01 can be used as a high frame rate camera, and 2/3-inch NTSC B/W TV correspondence. The S7986-01 and S7987-01 also feature low dark signal (MPP mode operation). The S7986-01 and S7987-01 have an effective pixel size of 14 × 14 µm and is available in image areas of 9.212 (H) × 6.860 (V) mm.
One-stage peltier cooler is built into the package for thermoelectric cooling (S7987-01). At room temperature operation, the device can be cooled down to -10 ˚C (typ.) without using any other cooling technique. In addition, since both the CCD chip and the peltier cooler are hermetically sealed, no dry air is required, thus allowing easy handling.

Features

- High-speed on-chip amplifier
  (14 MHz, 2/3-inch NTSC B/W TV correspondence)
- Greater than 90% quantum efficiency
- Wide spectrum range
- MPP operation
- Non-cooled types: S7986-01
  One-stage TE-cooled types: S7987-01
  (Two-stage TE-cooled types are optional)

Applications

- High-speed UV imaging
- Semiconductor inspection
- Microscope

■ Selection and order guide

Type No.	Cooling	Number of total pixels	Number of active pixels	Active area [mm (H) × mm (V)]
S7986-01	Non-cooled	680 × 500	658 × 490	9.212 × 6.860
S7987-01	One-stage TE-cooled			

■ General ratings

Parameter	Specification
CCD structure	Frame transfer (2/3-inch NTSC B/W TV correspondence)
Pixel size	14 (H) × 14 (V) µm
Vertical clock phase	2-phase
Horizontal clock phase	2-phase
Output circuit	Two-stage MOSFET source follower
Package	24-pin ceramic package
Window*1	Sapphire

*1: Temporary window type (ex. S7986-01N) is available upon request.

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■ Absolute maximum ratings (Ta=25 °C)

Parameter	Symbol	Min.	Typ.	Max.	Unit
Operating temperature*2	Topr	-50	-	+30	°C
Storage temperature	Tstg	-50	-	+70	°C
OD voltage	V_{OD}	-0.5	-	+25	V
RD voltage	V_{RD}	-0.5	-	+18	V
ISV voltage	V_{ISV}	-0.5	-	+18	V
ISH voltage	V_{ISH}	-0.5	-	+18	V
IGV voltage	V_{IG1V}, V_{IG2V}	-10	-	+15	V
IGH voltage	V_{IG1H}, V_{IG2H}	-10	-	+15	V
SG voltage	V_{SG}	-10	-	+15	V
OG voltage	V_{OG}	-10	-	+15	V
RG voltage	V_{RG}	-10	-	+15	V
TG voltage	V_{TG}	-10	-	+15	V
Vertical clock voltage (image area)	V_{P1VI}, V_{P2VI}	-10	-	+15	V
Vertical clock voltage (storage area)	V_{P1VS}, V_{P2VS}	-10	-	+15	V
Horizontal clock voltage	V_{P1H}, V_{P2H}	-10	-	+15	V

*2: Chip temperature

■ Operating conditions (MPP mode, Ta=25 °C)

Parameter			Symbol	Min.	Typ.	Max.	Unit
Output transistor drain voltage			V_{OD}	12	15	18	V
Reset drain voltage			V_{RD}	11.5	12	12.5	V
Output gate voltage			V_{OG}	1	3	5	V
Substrate voltage			V_{SS}	-	0	-	V
Test point	Vertical input source		V_{ISV}	-	V_{RD}	-	V
	Horizontal input source		V_{ISH}	-	V_{RD}	-	V
	Vertical input gate		V_{IG1V}, V_{IG2V}	-9	-8	-	V
	Horizontal input gate		V_{IG1H}, V_{IG2H}	-9	-8	-	V
Vertical shift register clock voltage (Image area)		High	V_{P1VIH}, V_{P2VIH}	4	6	8	V
		Low	V_{P1VIL}, V_{P2VIL}	-9	-8	-7	
Vertical shift register clock voltage (Storage area)		High	V_{P1VSH}, V_{P2VSH}	4	6	8	V
		Low	V_{P1VSL}, V_{P2VSL}	-9	-8	-7	
Horizontal shift register clock voltage		High	V_{P1HH}, V_{P2HH}	4	6	8	V
		Low	V_{P1HL}, V_{P2HL}	-9	-8	-7	
Summing gate voltage		High	V_{SGH}	4	6	8	V
		Low	V_{SGL}	-9	-8	-7	
Reset gate voltage		High	V_{RGH}	4	6	8	V
		Low	V_{RGL}	-9	-8	-7	
Transfer gate voltage		High	V_{TGH}	4	6	8	V
		Low	V_{TGL}	-9	-8	-7	
External load resistance			R_L	2.0	2.2	2.4	kΩ

■ Electrical characteristics (Ta=25 °C)

Parameter	Symbol	Min.	Typ.	Max.	Unit
Signal output frequency	fc	-	1	14	MHz
Vertical shift register capacitance (Image area)	C_{P1VI} C_{P2VI}	-	3000	-	pF
Vertical shift register capacitance (Storage area)	C_{P1VS} C_{P2VS}	-	3000	-	pF
Horizontal shift register capacitance	C_{P1H}, C_{P2H}	-	90	-	pF
Summing gate capacitance	C_{SG}	-	30	-	pF
Reset gate capacitance	C_{RG}	-	30	-	pF
Charge transfer gate capacitance	C_{TG}	-	70	-	pF
Transfer efficiency*3	CTE	0.99995	0.99999	-	-
DC output level	Vout	-	8	-	V
Output impedance	Zo	-	500	-	Ω
Power consumption*4	P	-	60	-	mW

*3: Charge transfer efficiency per pixel, measured at half of the full well capacity.
*4: Power consumption of the on-chip amplifier plus load resistance

■ Electrical and optical characteristics (Ta=25 °C, unless otherwise noted)

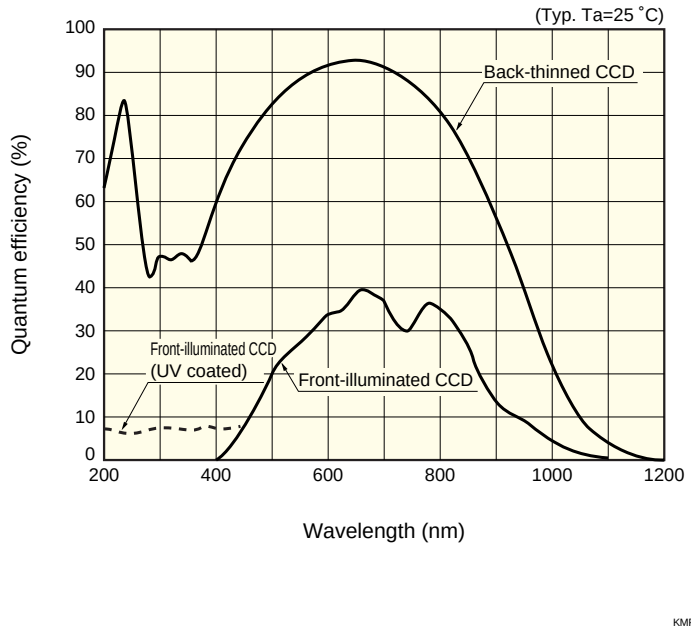
Parameter			Symbol	Min.	Typ.	Max.	Unit
Saturation output voltage			Vsat	-	Fw × Sv	-	V
Full well capacity	Vertical		Fw	30	65	-	ke⁻
	Horizontal			60	130	-	
CCD node sensitivity			Sv	1.5	2.0	-	μV/e⁻
Dark current*5 (MPP mode)	25 °C		DS	-	50	500	e⁻/pixel/s
	0 °C			-	5	50	
Readout noise*6			Nr	-	150	300	e⁻rms
Dynamic range (area scanning)*7			DR	200	430	-	-
Photo response non-uniformity*8			PRNU	-	-	±10	%
Spectral response range			λ	-	200 to 1100	-	nm
Blemish	Point defect*9	White spots	-	-	-	0	-
		Black spots		-	-	10	-
	Cluster defect*10			-	-	3	-
	Column defect*11			-	-	0	-

*5: Dark current nearly doubles for every 5 to 7 °C increase in temperature.
*6: -50 °C, Operating frequency is 12 MHz.
*7: Dynamic range (DR) = Full well/Readout noise
*8: Measured at one-half of the saturation output (full well capacity) using LED light (peak emission wavelength: 660 nm)

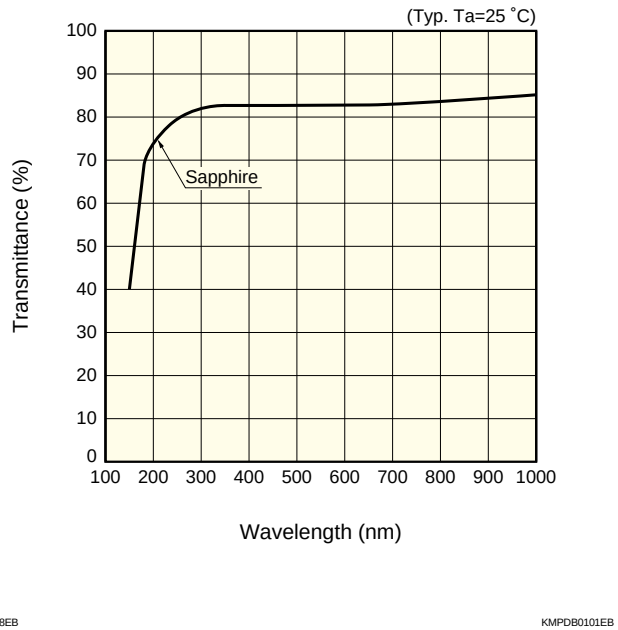
$$\text{Photo response non-uniformity (PRNU) (\%)} = \frac{\text{Fixed pattern noise (peak to peak)}}{\text{Signal}} \times 100$$

*9: White spots
Pixels whose dark current is higher than 1 ke⁻ after one-second integration at 0 °C
Black spots
Pixels whose sensitivity is lower than one-half of the average pixel output (measured with uniform light producing one-half of the saturation charge)
*10: 2 to 9 contiguous defective pixels
*11: 10 or more contiguous defective pixels

■ Spectral response (without window)*12

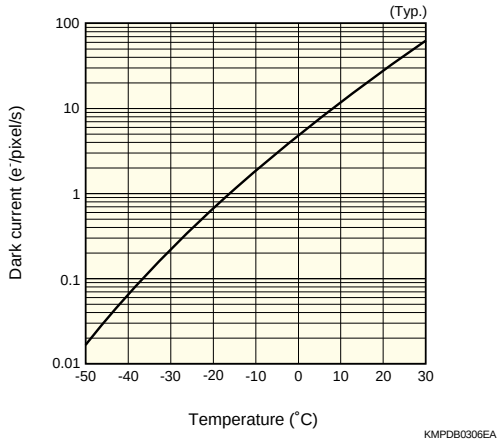


■ Spectral transmittance characteristic of window material



*14: Spectral response with sapphire is decreased according to the spectral transmittance characteristic of window material.

■ Dark current vs. temperature

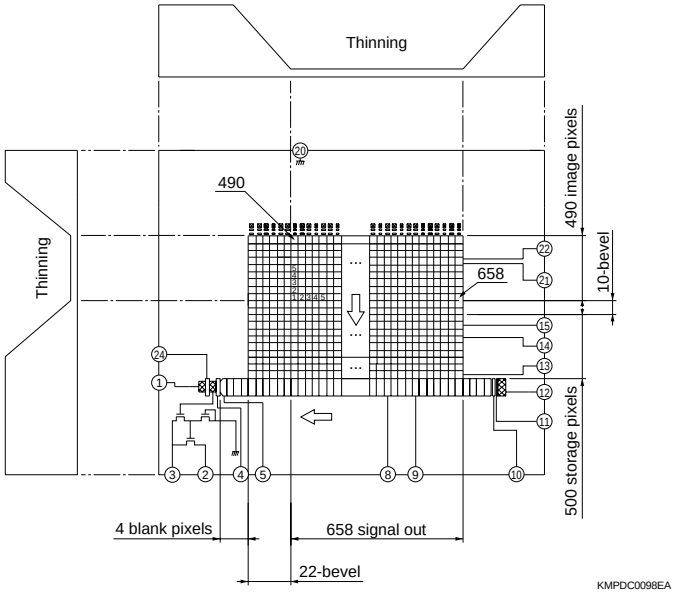


● Window material

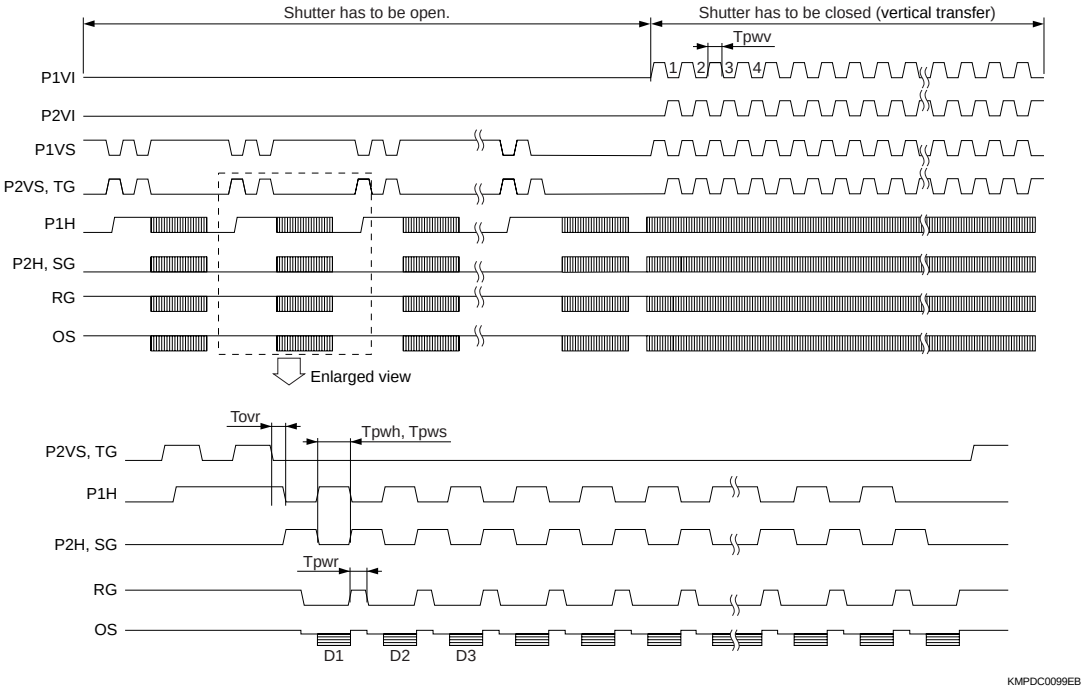
Type no.	Window material
S7986-01	Sapphire*13
S7987-01	(option: window-less)

*13: Hermetic sealing

■ Device structure (Conceptual drawing of top view)



■ Timing chart (2-line binning TV rate operation)

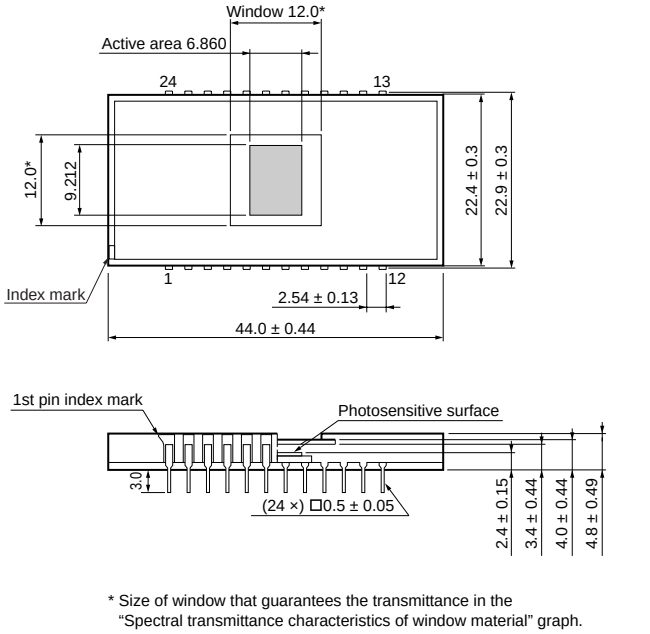


Parameter		Symbol	Min.	Typ.	Max.	Unit
P1VI, P2VI, P1VS, P2VS, TG*14	Pulse width	Tpwv	1	-	-	µs
	Rise and fall times	Tprv, Tpfv	20	-	-	ns
P1H, P2H*14	Pulse width	Tpwh	35	-	-	ns
	Rise and fall times	Tprh, Tpfh	10	-	-	ns
	Duty ratio	-	-	50	-	%
SG	Pulse width	Tpws	35	-	-	ns
	Rise and fall times	Tprs, Tpfs	10	-	-	ns
	Duty ratio	-	-	50	-	%
RG	Pulse width	Tpwr	15	-	-	ns
	Rise and fall times	Tprr, Tpfr	5	-	-	ns
TG - P1H	Overlap time	Tovr	3	-	-	µs

*14: Symmetrical clock pulses should be overlapped at 50% of maximum amplitude.

■ Dimensional outlines (unit: mm)

S7986-01



* Size of window that guarantees the transmittance in the "Spectral transmittance characteristics of window material" graph.

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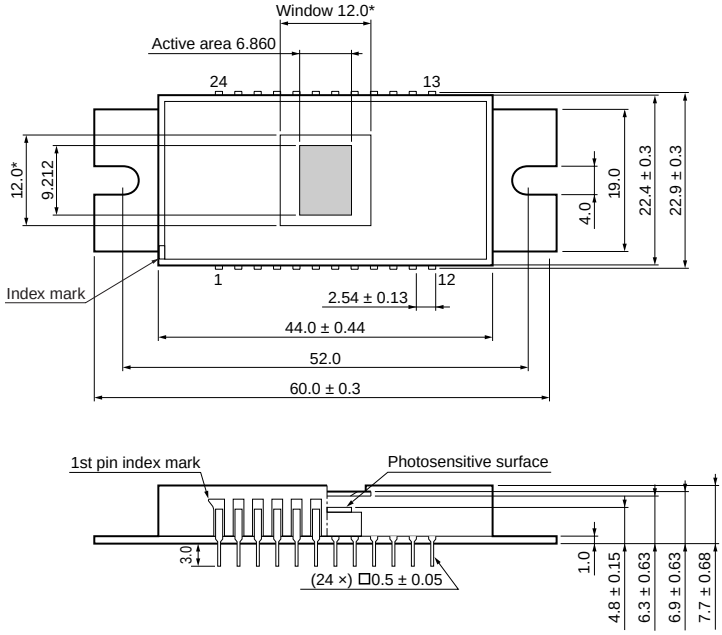
S7987-01



* Size of window that guarantees the transmittance in the "Spectral transmittance characteristics of window material" graph.

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■ Pin connections

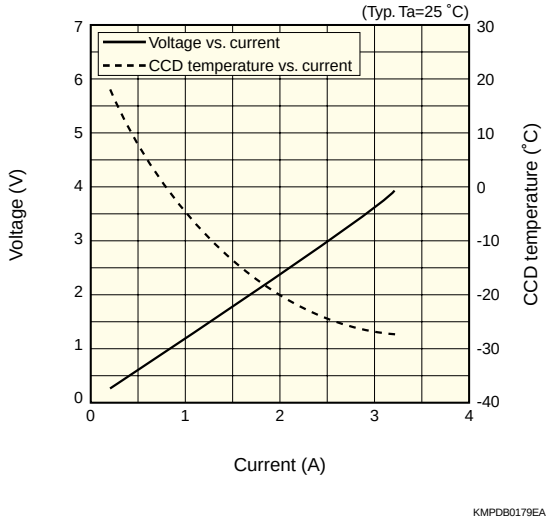
Pin no.	S7986-01		S7987-01		Remark (standard operation)
	Symbol	Function	Symbol	Function	
1	RD	Reset drain	RD	Reset drain	+12 V
2	OS	Output transistor source	OS	Output transistor source	R_L=2.2 kΩ
3	OD	Output transistor drain	OD	Output transistor drain	+15 V
4	OG	Output gate	OG	Output gate	+3 V
5	SG	Summing gate	SG	Summing gate	Same timing as P2H
6	-		-		
7	-		-		
8	P2H	CCD horizontal register clock-2	P2H	CCD horizontal register clock-2	
9	P1H	CCD horizontal register clock-1	P1H	CCD horizontal register clock-1	
10	IG2H	Test point (horizontal input gate-2)	IG2H	Test point (horizontal input gate-2)	-8 V
11	IG1H	Test point (horizontal input gate-1)	IG1H	Test point (horizontal input gate-1)	-8 V
12	ISH	Test point (horizontal input source)	ISH	Test point (horizontal input source)	Shorted to RD
13	TG	Transfer gate	TG	Transfer gate	Same timing as P2VS*15
14	P2VS	CCD vertical register clock-2 (storage area)	P2VS	CCD vertical register clock-2 (storage area)	
15	P1VS	CCD vertical register clock-1 (storage area)	P1VS	CCD vertical register clock-1 (storage area)	
16	-		Th1	Thermistor	
17	-		Th2	Thermistor	
18	-		P-	TE-cooler-	
19	-		P+	TE-cooler+	
20	SS	Substrate (GND)	SS	Substrate (GND)	GND
21	P2VI	CCD vertical register clock-2 (image area)	P2VI	CCD vertical register clock-2 (image area)	
22	P1VI	CCD vertical register clock-1 (image area)	P1VI	CCD vertical register clock-1 (image area)	
23	-		-		
24	RG	Reset gate	RG	Reset gate	

*15: TG is an isolation gate between vertical register and horizontal resister.
In standard operation, the same pulse of P2VS should be applied to the TG.

■ Specifications of built-in TE-cooler (Typ.)

Parameter	Symbol	Condition	Value	Unit
Internal resistance	Rint	Ta=25 °C	1.2	Ω
Maximum current*16	Imax	Tc*17=Th*18=25 °C	3.0	A
Maximum voltage	Vmax	Tc*17=Th*18=25 °C	3.6	V
Maximum heat absorption*19	Qmax		5.1	W
Maximum temperature of hot side	-		70	°C

*16: If the current is greater than Imax, the heat absorption begins to decrease due to the Joule heat. It should be noted that this value is not a damage threshold. To protect the thermoelectric cooler and maintain stable operation, the supply current should be less than 60 % of this maximum current.
*17: Temperature of cooling side of thermoelectric cooler
*18: Temperature of heat radiating side of thermoelectric cooler
*19: This is a heat absorption when the maximum current is supplied to the TE-cooler.



KMPDB0179EA

■ Specifications of built-in temperature sensor (S7987-01)

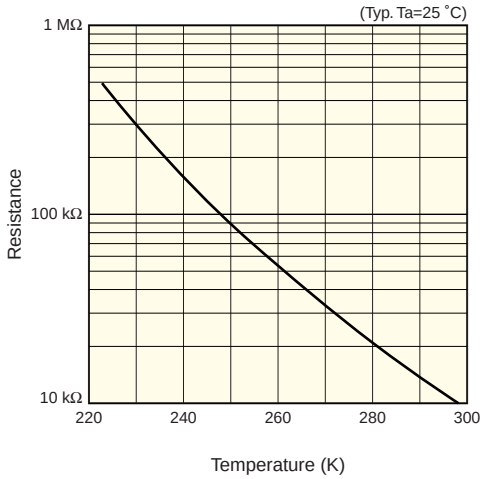
A chip thermistor is built in the same package with a CCD chip, and the CCD chip temperature can be monitored with it. A relation between the thermistor resistance and absolute temperature is expressed by the following equation.

$R_{T1} = R_{T2} \times \exp B_{T1/T2} (1/T1 - 1/T2)$

R_{T1}: Resistance at absolute temperature T1 [K]
R_{T2}: Resistance at absolute temperature T2 [K]
$B_{T1/T2}$: B constant [K]

The characteristics of the thermistor used are as follows.

R_{298}=10 kΩ
$B_{298/323}$=3450 K



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■ Precaution for use (electrostatic countermeasures)

- Handle these sensors with bare hands or wearing cotton gloves. In addition, wear anti-static clothing or use a wrist band with an earth ring, in order to prevent electrostatic damage due to electrical charges from friction.
- Avoid directly placing these sensors on a work-desk or work-bench that may carry an electrostatic charge.
- Provide ground lines or ground connection with the work-floor, work-desk and work-bench to allow static electricity to discharge.
- Ground the tools used to handle these sensors, such as tweezers and soldering irons.

It is not always necessary to provide all the electrostatic measures stated above. Implement these measures according to the amount of damage that occurs.

■ Element cooling/heating temperature gradient rate

When using an external cooler, the element cooling/heating temperature gradient rate should be set at less than 5 K/min.

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