High density UV erasable programmable logic device

PLV5000/L

DESCRIPTION

The PLV5000/L is an easy to use, high density programmable logic device. Its simple, regular architecture translates into increased utilization and high performance.

The PLV5000/L has one programmable combinatorial logic array. This guarantees easy interconnection of and uniform performance from all nodes. "Sum terms", which are easy to use groupings of AND-OR gates, provide combinatorial logic blocks. Sum terms can be wire-OR'd together to integrate larger logic blocks. To expand the levels of logic, buried sum terms feed back into the logic array. The 52 I/O pins can each be driven by a register or a sum term. Each I/O pin has an individually enabled input latch.

All 128 registers are configurable as D or T types without using extra logic gates. Individual sum terms, asynchronous presets, resets and clocks give each flip-flop added flexibility. A direct "clock from pin" option guarantees synchronization and fast clock to output performance.

Standard off-the-shelf third party software tools and programmers support the PLV5000/L. This minimizes start-up investment and improves product support.

APPLICATIONS

- High speed microprocesser interface
- Peripheral control
- Bus interface
- Instrumentation control
- Industial process control
- Telecom interface

FEATURES

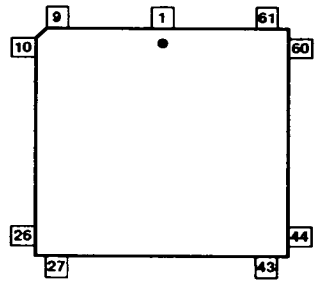
- Advanced programmable logic device—high gate utilization
- Flexible interconnect architecture—universal routing
- Flexible logic cells—128 flip-flops and 52 latches
- Multiple flip-flop types—synchronous or asynchronous registers
- High speed—50MHz operation
- Complete third party software support
  - No placement, routing or layout software required
- Proven and reliable high speed CMOS EPROM process
  - 2000V ESD protection
  - 200mA latchup immunity
- Reprogrammable—tested 100% for programmability

PIN DESCRIPTIONS

PIN NAME	FUNCTION
IN	Logic and clock inputs
Pins 2, 32, 36, 66	Input/Register Clocks 1–4
Pins 1, 34, 35, 68	Input/Latch Clocks 1–4
I/O	Bi-directional buffers
V_{CC}	+5V Supply
GND	Ground

PIN CONFIGURATION

A and KA Packages



Pin	Function	Pin	Function	Pin	Function
1	IN	24	I/O	47	I/O
2	IN	25	I/O	48	I/O
3	VCC	26	I/O	49	I/O
4	I/O	27	I/O	50	GND
5	I/O	28	I/O	51	I/O
6	I/O	29	I/O	52	I/O
7	I/O	30	I/O	53	I/O
8	I/O	31	I/O	54	VCC
9	I/O	32	IN	55	I/O
10	I/O	33	GND	56	I/O
11	I/O	34	IN	57	I/O
12	I/O	35	IN	58	I/O
13	I/O	36	IN	59	I/O
14	I/O	37	VCC	60	I/O
15	I/O	38	I/O	61	I/O
16	GND	39	I/O	62	I/O
17	I/O	40	I/O	63	I/O
18	I/O	41	I/O	64	I/O
19	I/O	42	I/O	65	I/O
20	VCC	43	I/O	66	IN
21	I/O	44	I/O	67	GND
22	I/O	45	I/O	68	IN
23	I/O	46	I/O		

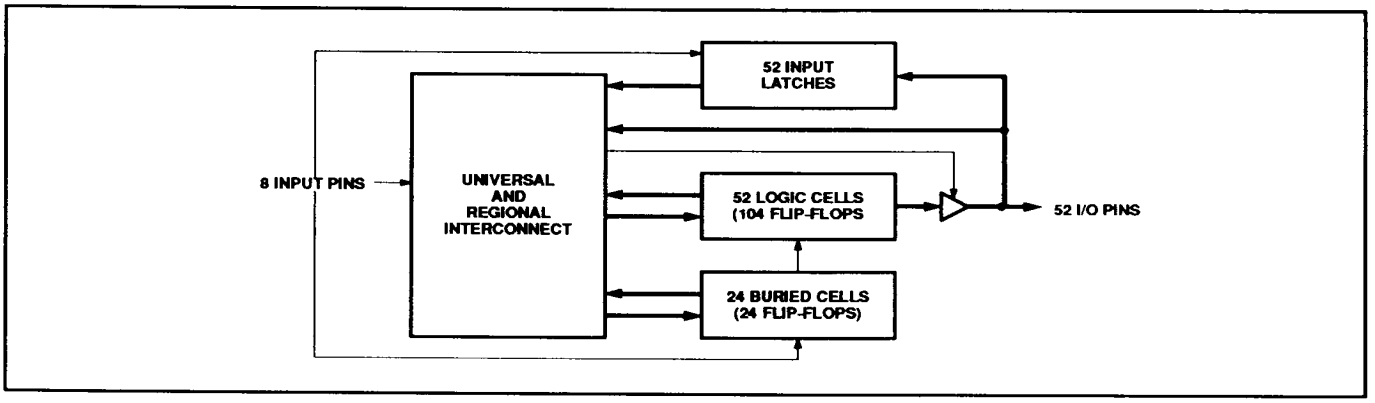
ORDERING INFORMATION

DESCRIPTION	ORDER CODE
68-Pin Cerquad J-Bend Package with Quartz Window (t_{PD} = 25ns)	PLV5000-25KA
68-Pin Plastic Leaded Chip Carrier (t_{PD} = 25ns)	PLV5000-25A
68-Pin Cerquad J-Bend Package with Quartz Window (t_{PD} = 30ns)	PLV5000-30KA, PLV5000L30KA
68-Pin Plastic Leaded Chip Carrier (t_{PD} = 30ns)	PLV5000-30A, PLV5000L-30A
68-Pin Cerquad J-Bend Package with Quartz Window (t_{PD} = 35ns)	PLV5000L35KA
68-Pin Plastic Leaded Chip Carrier (t_{PD} = 35ns)	PLV5000L-35A

High density UV erasable programmable logic device

PLV5000/L

FUNCTIONAL BLOCK DIAGRAM



PLV5000 BLOCK DIAGRAM

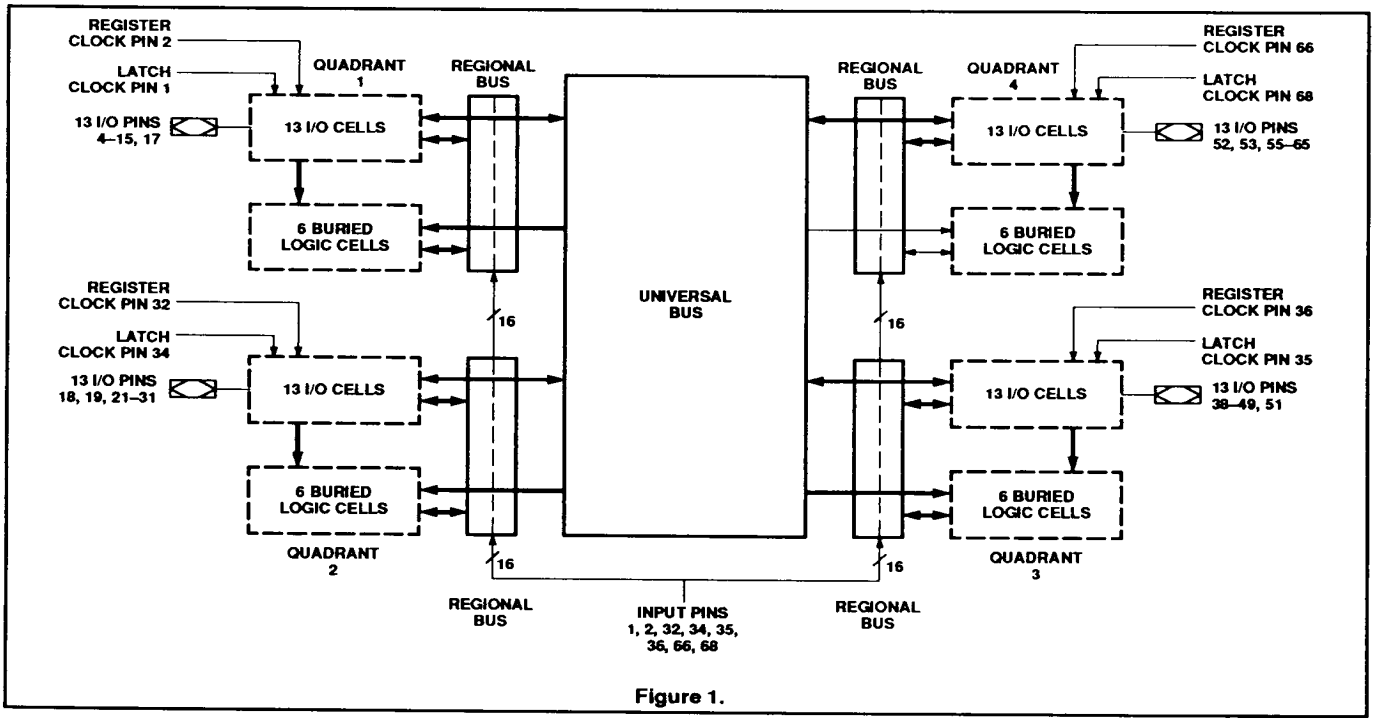


Figure 1.

FUNCTIONAL LOGIC DIAGRAM DESCRIPTION

There are 52 identical Input/Output logic cells and 24 identical buried logic cells in the PLV5000. Each I/O cell has 2 flip-flops, up to 3 sum terms, individual clock, reset, and preset terms per flip-flop, and one output enable term. Independent of output configuration, all flip-flops are always usable, and have at least 4 product terms inputs each.

Each I/O pin (52 total) signal or its latched version drives the logic array. There is one latch clock per quadrant.

The PLV5000 has 4 identical quadrants (see Figure 1). The Universal Bus routs true and false signals from each of the 52 I/O pins to all four quadrants. regional buses route each quadrant's flip-flop Q and $\overline{Q}$ locally. The 8 input-only pins are available in all 4 regional buses.

Each logic cell has a number of "regional" and "universal" product terms (see Figure 2). The I/O logic cells contain 3 sum terms, 2 flip-flops, and an I/O buffer.

The buried logic cells each contain 1 flip-flop. In addition, in each buried logic cell the sum term can drive the regional bus. This allows for logic expansion.

Serial register preload and observability simplify testing. All registers automatically clear at power up.

QUADRANT FUNCTIONAL LOGIC DIAGRAM PLV5000

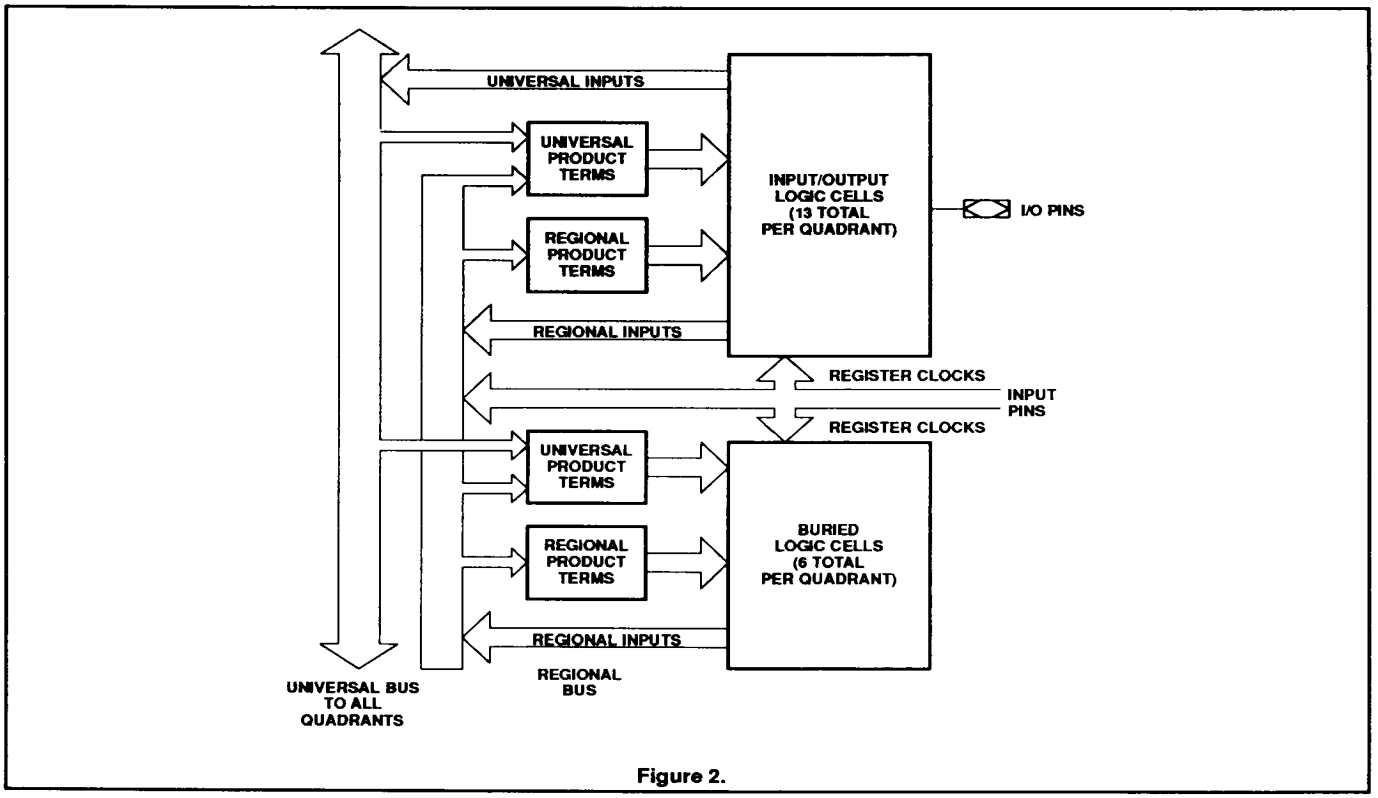


Figure 2.

QUADRANT LOGIC DIAGRAM AND DESCRIPTION

The PLV5000 has: 4 identical quadrants, 52 identical input/output logic cells, and 24 identical buried logic cells. The universal bus routes true and false signals from each of the 52 I/O pins to all four quadrants. Regional buses route each quadrant's flip-flop Q and $\overline{Q}$ locally. The 8 input-only pins are available in every regional bus.

Each logic cell has a number of "regional" and "universal" product terms (see Figure 3).

Regional product terms have as inputs all quadrant flip-flop outputs (or buried flip-flop inputs) and the 8 dedicated input pins. Universal product terms have the same inputs plus the 52 I/O pins and their complements.

The buried logic cells (Figure 4) each contain 1 flip-flop. The sum term has 1 universal product term and 4 regional product terms for a total of 5. The flip-flop has universal Asynchronous Preset, Reset, and Clock terms. In addition, in each buried logic cell the sum term can be fed back into the regional bus instead of the flip-flop. This allows for logic expansion.

The I/O logic cells (Figure 5, Figure 6, and Figure 7) contain 3 sum terms, 2 flip-flops, and an I/O buffer. Sum term B has 5 product terms – 2 universal and 3 regional. Flip-flop Q1 has global Asynchronous Preset, Reset, and Clock product terms. Flip-flop Q2 has universal Asynchronous Reset and Clock terms and a regional Asynchronous Preset term. There is 1 universal product term for the I/O pin Output Enable.

QUADRANT CLOCK PIN ASSIGNMENTS

QUADRANT NUMBER	REGISTER CLOCK PIN	LATCH CLOCK PIN
1	2	1
2	32	34
3	36	35
4	66	68

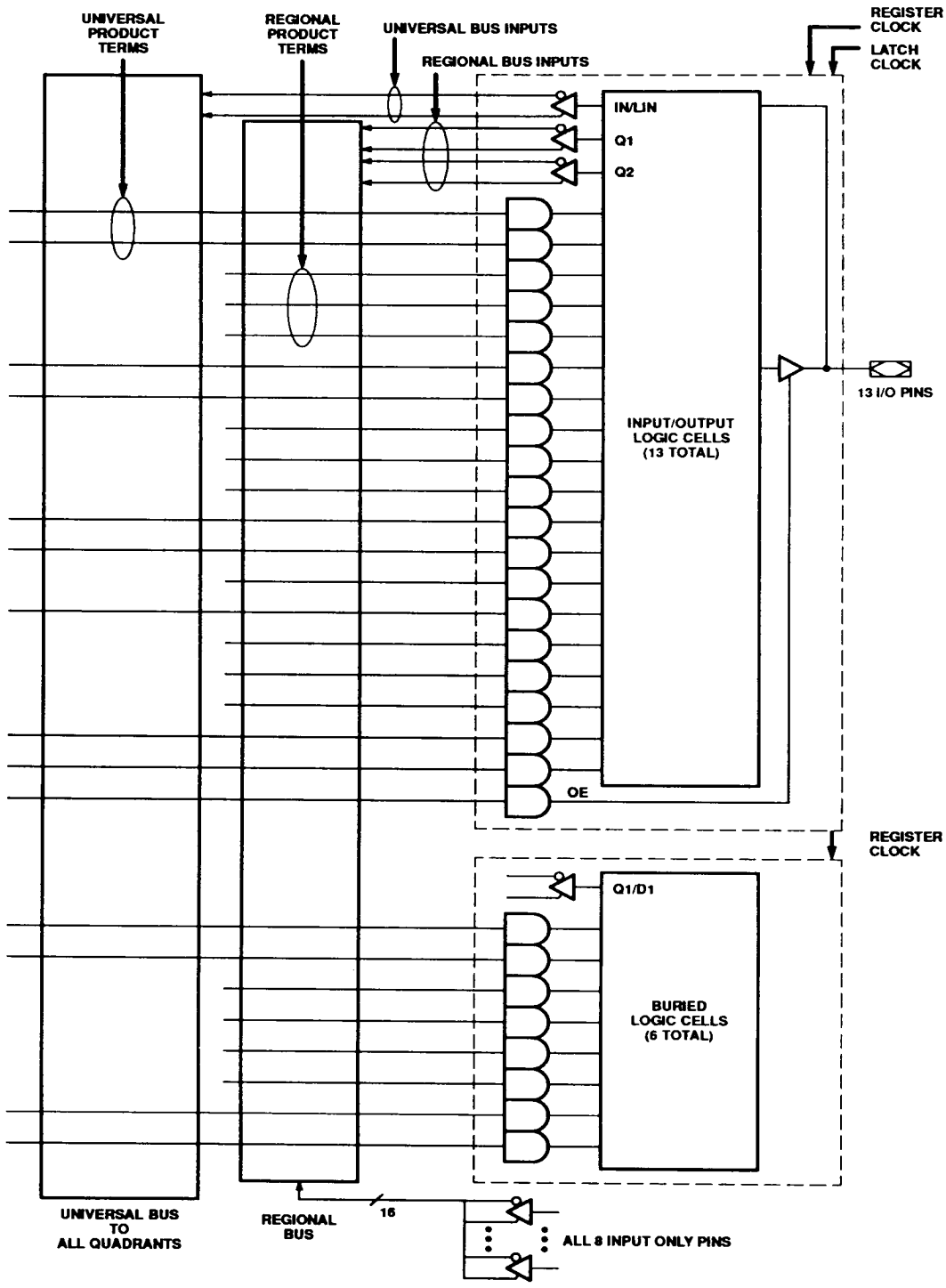


Figure 3. Quadrant Structure

LOGIC CELL OPTIONS

The PLV5000 logic cells contain most of the chip's logic options. The standard logic cell contains 2 flip-flops, 3 sum terms and 3 array inputs. the 3 sum terms can be combined to provide sum term options of 4, 5, 9, or 13 product terms. A combinatorial signal or the output of Q1 can be sent to the I/O cell.

The PLV5000 retains the PLV2500's ability to bury both registers in the I/O cell and still output a combinatorial signal (see Figure 6). A new feature, unique to the PLV5000, is the ability to output Q1 and feedback the combinatorial term directly (see Figure 5). this high speed logic expansion term increases the device's flexibility and gate utilization.

BURIED LOGIC CELLS

Each quadrant has six buried logic cells (see Figure 4). Each cell contains one sum term with 5 product terms, a flip-flop, and individual preset, clear and clock terms. A configuration bit selects either the Q output or the D input for feedback into the regional bus.

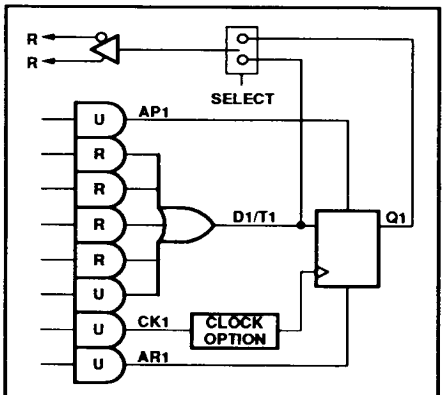


Figure 4. Buried Logic Cells

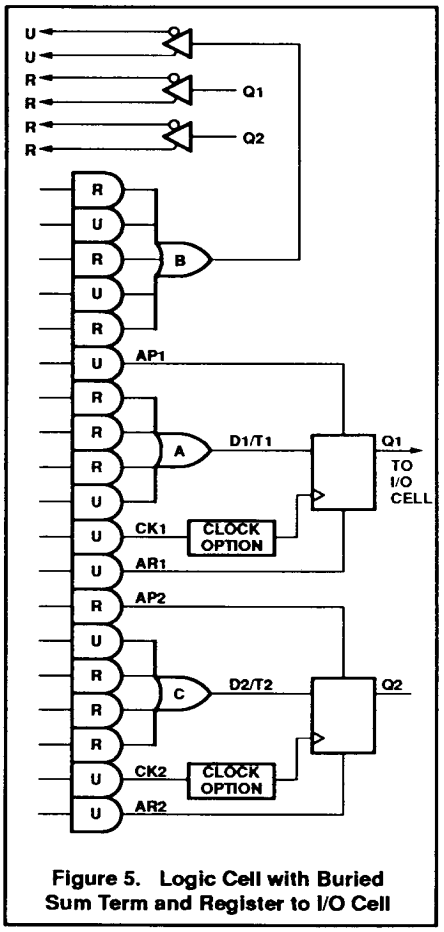


Figure 5. Logic Cell with Buried Sum Term and Register to I/O Cell

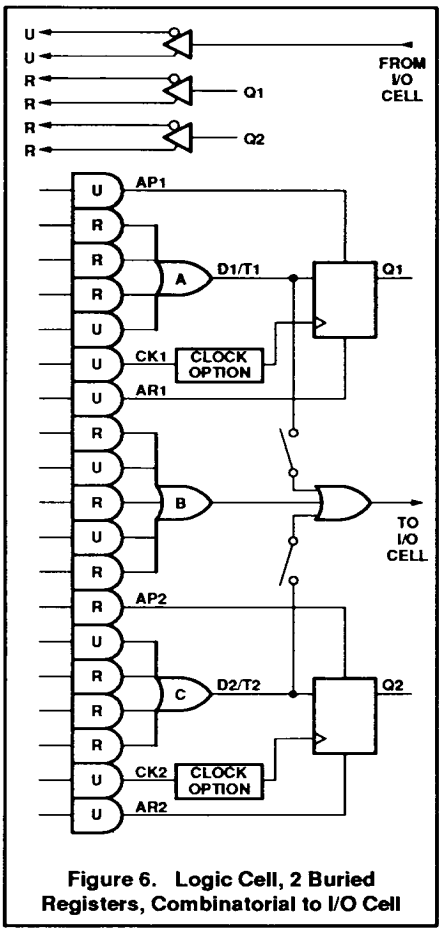


Figure 6. Logic Cell, 2 Buried Registers, Combinatorial to I/O Cell

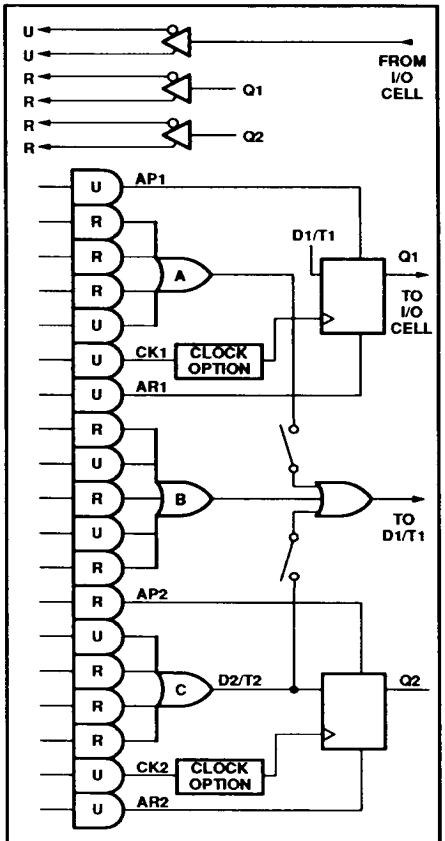


Figure 7. Logic Cell with Combinable Sum Terms, Register to I/O Cell

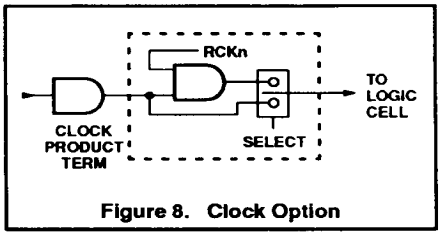


Figure 8. Clock Option

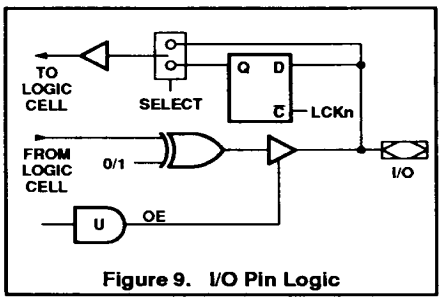


Figure 9. I/O Pin Logic

FLIP-FLOP CLOCK OPTIONS

Each register may be connected to its regional clock to provide fast clock to output timing (see Figure 8). In this "synchronous" mode, the clock is one of four input pins, a unique clock pin for each chip quadrant. One product term defines each flip-flop's clock in the "asynchronous" mode.

In the "synchronous" mode, the regional clock is ANDed with the product term. This provides the fast timing of a synchronous clock with the local control of the product term.

I/O PIN LATCHES

Each I/O pin of the PLV5000 has an input latch which can be individually enabled or disabled (see Figure 9). Each chip quadrant has a unique latch clock. When the latch is inactive, pin input flows directly into the array. When activated, the latch is flow-through when the clock signal is LOW, and data is captured on the clock's rising edge.

FLIP-FLOP TYPES

Each flip-flop in the PLV5000 may be configured as either a T or D type flip-flop. A T type flip-flop can also easily be configured into a JK or SR flip-flop.

ABSOLUTE MAXIMUM RATINGS[1]

SYMBOL	PARAMETER	RATINGS	UNIT
V_{IN}	Voltage on any pin with respect to ground[2]	–2.0 to +7.0	V_{DC}
V_{IP}	Voltage on input pins with respect to ground during programming[2]	–2.0 to +14.0	V_{DC}
V_{PP}	Programming voltage with respect to ground[2]	–2.0 to +14.0	V
—	Integrated UV erase dose	7258	Wsec/cm^2
T_{bias}	Temperature under bias	–55 to +125	°C
T_{stg}	Storage temperature	–65 to +150	°C

NOTES:

1. Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.
2. Minimum voltage is $-0.6V_{DC}$ which may undershoot to –2.0V for pulses of less than 20ns. Maximum output pin voltage is $V_{CC} + 0.75V_{DC}$ which may overshoot to +7.0V for pulses of less than 20ns.

DC ELECTRICAL CHARACTERISTICS

$0°C \leq T_{amb} \leq 70°C$, $4.5V \leq V_{CC} \leq 5.5V$

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS			UNIT
			MIN	TYP	MAX	
I_{LI}	Input load current	$V_{IN} = -0.1V$ to $V_{CC} + 1V$			10	µA
I_{LO}	Output leakage current	$V_{OUT} = -0.1V$ to $V_{CC} + 0.1V$			10	µA
I_{CC}	Power supply current, PLV5000	V_{CC} = MAX, V_{IN} = GND or V_{CC}, Outputs Open		200	350	mA
	Power supply current, PLV5000L	V_{CC} = MAX, V_{IN} = GND or V_{CC}, Outputs Open		20	40	mA
I_{CC2}	Clocked power supply current (PLV5000L only)	f = 1MHz, V_{CC} = MAX, Outputs Open		30	50	mA
I_{OS}	Output short circuit current[1]	$V_{OUT} = 0.5V$			–90	mA
V_{IL}	Input Low voltage		–0.6		0.8	V
V_{IH}	Input High voltage		2.0		V_{CC}+0.75	V
V_{OL}	Output Low voltage	$V_{IN} = V_{IH}$ or V_{IL}, I_{OL} = 8mA			0.5	V
V_{OH}	Output High voltage	$I_{OH} = -100µA$	V_{CC}–0.3			V
		$I_{OH} = -4.0mA$	2.4			V
C_{IN}	Input capacitance[2]	$V_{IN} = 0V$, f = 1MHz, T_{amb} = 25°C		6	8	pF
C_{OUT}	Output capacitance[2]	$V_{OUT} = 0V$, f = 1MHz, T_{amb} = 25°C		8	12	pF

NOTES:
1. Not more than one output at a time should be shorted. Duration of short circuit test should not exceed 30 seconds.
2. Typical values for nominal supply voltage. This parameter is only sampled and is not 100% tested.

REGISTER AC ELECTRICAL CHARACTERISTICS, INPUT PIN CLOCK

SYMBOL	PARAMETER	LIMITS						UNIT
		PLV5000-25		PLV5000/L-30		PLV5000L-35		
		MIN	MAX	MIN	MAX	MIN	MAX	
t_{COS}	Clock to output		15		20		25	ns
t_{CFS}	Clock to feedback	0	5	0	7	0	8	ns
t_{SIS}	Input setup time[1]	16		17		20		ns
t_{SFS}	Feedback setup time[1]	15		18		22		ns
t_{HS}	Hold time	0		0		0		ns
t_{WS}	Clock width	10		12		15		ns
t_{PS}	Clock period	20		25		30		ns
f_{MAXS}	Maximum frequency ($1/t_{PS}$)		50		40		33	MHz
t_{ARS}	Asynchronous Reset/Preset recovery time	20		25		30		ns

NOTES:
1. Add 3ns for Universal product terms.

REGISTER AC ELECTRICAL CHARACTERISTICS, PRODUCT TERM CLOCK

SYMBOL	PARAMETER	LIMITS						UNIT
		PLV5000-25		PLV5000/L-30		PLV5000L-35		
		MIN	MAX	MIN	MAX	MIN	MAX	
t_{COA}	Clock to output		25		30		35	ns
t_{CFA}	Clock to feedback	7	20	10	25	12	27	ns
t_{SIA}	Input setup time[1]	10		12		15		ns
t_{SFA}	Feedback setup time[1]	5		8		13		ns
t_{HA}	Hold time	8		10		12		ns
t_{WA}	Clock width	12		15		15		ns
t_{PA}	Clock period	25		33		40		ns
f_{MAXA}	Maximum frequency ($1/t_{PA}$)		40		30		25	MHz
t_{ARA}	Asynchronous Reset/Preset recovery time	15		20		25		ns

NOTES:
1. Add 3ns for Universal product terms.

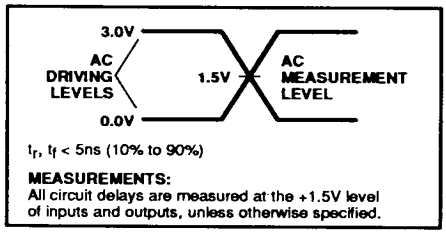
AC ELECTRICAL CHARACTERISTICS

$0°C \leq T_{amb} \leq 70°C$, $4.5V \leq V_{CC} \leq 5.5V$

SYMBOL	PARAMETER	LIMITS						UNIT
		PLV5000-25		PLV5000/L-30		PLV5000L-35		
		MIN	MAX	MIN	MAX	MIN	MAX	
t_{PD1}	Input to non-registered output[1]		25		30		35	ns
t_{PD2}	Feedback to non-registered output[1]		20		25		30	ns
t_{PD3}	Input to non-registered feedback[1]		20		25		30	ns
t_{PD4}	Feedback to non-registered feedback[1]		15		18		22	ns
t_{EA1}	Input to Output Enable		30		35		40	ns
t_{ER1}	Input to Output Disable		30		35		40	ns
t_{EA2}	Feedback to Output Enable		25		30		35	ns
t_{ER2}	Feedback to Output Disable		25		30		35	ns
t_S	Input latch setup time	5		6		7		ns
t_H	Input latch hold time	5		5		5		ns
t_W	Clock width	10		12		12		ns
t_P	Clock period	20		25		30		ns
f_{MAX}	Maximum frequency ($1/t_P$)		50		40		33	MHz
t_{AW}	Asynchronous Reset/Preset width	15		20		20		ns
t_{AP}	Asynchronous Reset/Preset to Registered Output		30		35		40	ns
t_{APF}	Asynchronous Reset/Preset to Registered Feedback		25		30		35	ns

NOTES:
1. Add 3ns for Universal product terms.

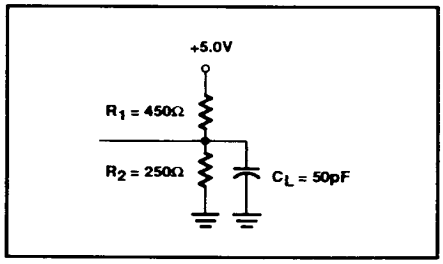
INPUT TEST WAVEFORMS AND MEASUREMENT LEVELS



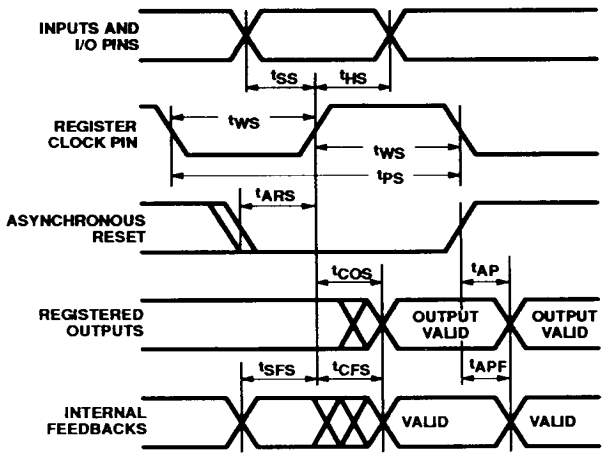
t_r, t_f < 5ns (10% to 90%)

MEASUREMENTS:
All circuit delays are measured at the +1.5V level of inputs and outputs, unless otherwise specified.

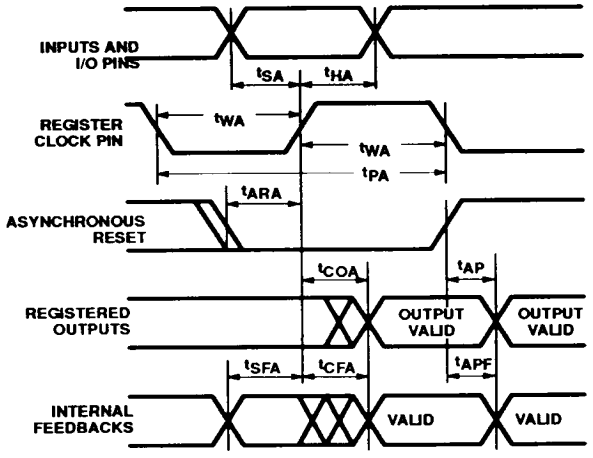
OUTPUT TEST LOAD



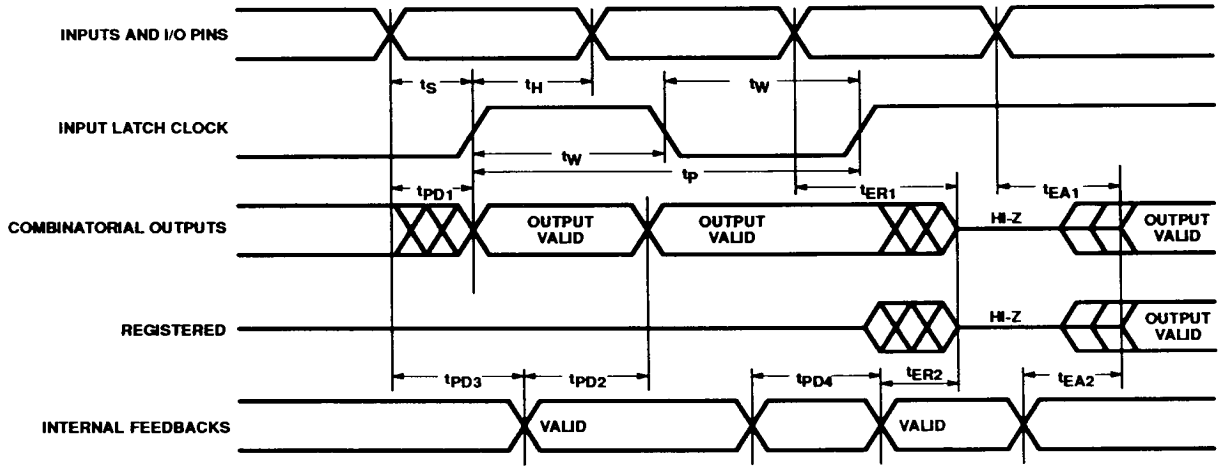
TIMING DIAGRAMS



Input Pin Clock



Product Term Clock



MEASUREMENTS:
Timing measurement reference is 1.5V. Input AC driving levels are 0.0V and 3.0V, unless otherwise specified.

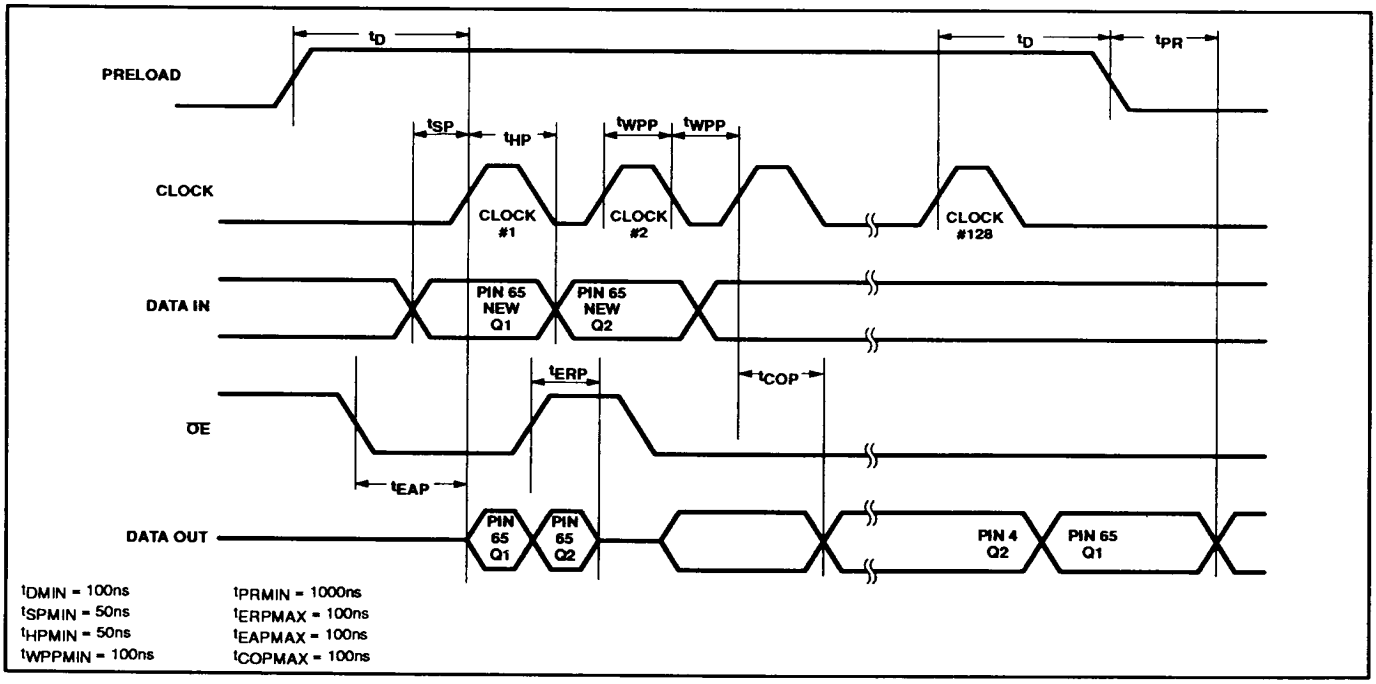
PRELOAD AND OBSERVABILITY OF REGISTERS

The PLV5000's registers include circuitry to load and unload them serially. This feature simplifies testing. Any state can be forced into the registers to control test sequencing, and all registers may be observed, independent of being buried. A V_{IH} level on the Data In pin will force the appropriate register HIGH; a V_{IL} will force it LOW, independent of the polarity or other configuration bit settings.

The Preload/Observe state is entered by placing an 11V to 14V signal on Pin 68. when the clock (Pin 1) is pulsed high, data (Pin 2) is clocked serially through all registers in the device, as in the following table. All register contents are also clocked out of the device on Pin 65 in FIFO fashion. If observability only is required, data out should be connected back to data in. If preload only is required, $\overline{OE}$ (Pin 66) can be held HIGH and data out (Pin 65) will remain high impedance.

Any user contemplating the use of register preload/observability is encouraged to contact Signetics PLD applications group.

NOTE: All register clock terms or pins must be LOW prior to entering the Preload/Observe state, and LOW prior to leaving the Preload/Observe state. Pin 1 must be LOW prior to entering the Preload/Observe state.



PRELOAD / OBSERVE REGISTER SCAN ORDER

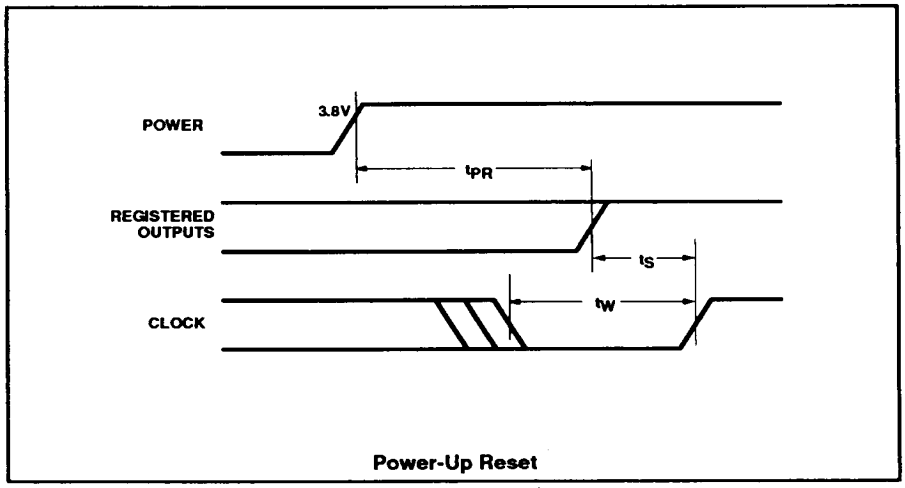
QUADRANT	PIN
Quadrant 1	Pin 4 5 6 ... 15 17 D_{IN} → Q2 → Q1 → B23 → Q2 → Q1 → Q2 → Q1 ... B18 → Q2 → Q1 → Q2 → Q1 → (Quadrant 2)
Quadrant 2 (Quadrant 1)→	Pin 18 19 21 22 ... 31 Q2 → Q1 → Q2 → Q1 → B17 → Q2 → Q1 → Q2 → Q1 ... B12 → Q2 → Q1 → (Quadrant 3)
Quadrant 3 (Quadrant 2)→	Pin 38 39 40 ... 49 51 Q2 → Q1 → B11 → Q2 → Q1 → Q2 → Q1 ... B6 → Q2 → Q1 → Q2 → Q1 → (Quadrant 4)
Quadrant 4 (Quadrant 3)→	Pin 52 53 55 56 ... 65 Q2 → Q1 → Q2 → Q1 → B5 → Q2 → Q1 → Q2 → Q1 ... B0 → Q2 → Q1 → D_{OUT}

POWER-UP RESET

The registers in the PLV5000 are designed to reset during power up. At a point delayed slightly from V_{CC} crossing 3.8V, all registers will be reset to the LOW state. The output state will depend on the polarity of the output buffer.

This feature is critical for state machine initialization. However, due to the asynchronous nature of reset and the uncertainty of how V_{CC} actually rises in the system, the following conditions are required:

1. The V_{CC} rise must be monotonic,
2. After reset occurs, all input and feedback setup times must be met before driving the clock term HIGH, and
3. The signals from which the clock is derived must remain stable during t_{PR}.



Power-Up Reset

PARAMETER	DESCRIPTION	MIN	TYP	MAX	UNIT
t_{PR}	Power-Up Reset time		600	1000	ns

USING THE PLV5000

The PLV5000's simple, regular architecture means that only simple logic compilers are required to configure the device. No layout or route and place are required. These software tools are readily available from companies such as Data I/O Corporation (ABEL™), Logical Devices (CUPL™), and ISDATA (LOGiC™).

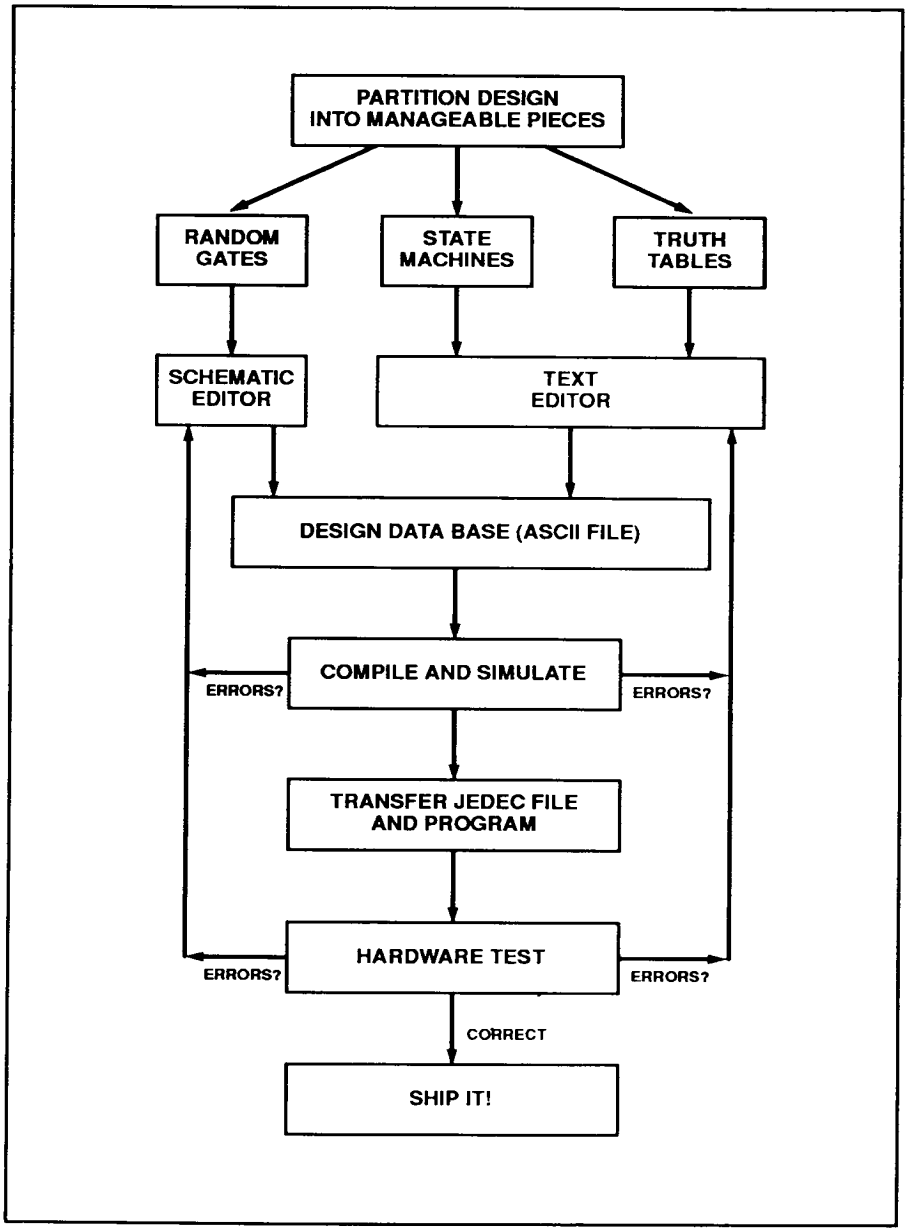
The first step in designing a device as complex as the PLV5000 is to partition your design into manageable blocks. These blocks are then allocated proportionally to each of the four quadrants of the PLV5000. Random gates can be described either with Boolean equations (a behavioral description) or with a schematic editor. Truth table logic and state machines are best described behaviorally and entered with a text editor. The design is then combined into one ASCII file, which is then submitted to the logic compiler. Compilation, logic reduction, simulation, JEDEC file creation and documentation are then completed by all of the popular compilers.

Assignment of signals to pins or buried nodes as well as selecting the various options of the PLV5000 (such as register clocks and input latches) can be done manually in the design data base file, or an automatic fitter may be used.

A logic fitter assigns pins and nodes to make best use of the features in the PLV5000, and frees the designer from being required to learn all of the features of a complex device such as the PLV5000. For further information on fitters for the PLV5000, contact Signetics' PLD applications department.

After correcting any syntax and logic errors discovered by the compiler, the JEDEC file is ready to download to an EPLD programmer. These are available from a number of manufacturers. Programmed devices are usually first tested in the programmer with your supplied test vectors. The next step is to check out your "custom chip" in the target system. When this hardware debug step is complete, your system is ready to go—all in a matter of hours.

DESIGN FLOW DIAGRAM



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OPERATING MODES

MODE	(68-Lead PLCC or Cerquad J-Bend Packages) PIN #								
	1	2	36	34	68	66	V_{CC} (3, 20, 37, 54)	I/Os	I/O Pin 65
"EPLD"	X[1]	X	X	X	X	X	5V	I/O	I/O
Program	V_{PP}	V_{IL}	V_{IL}	V_{IH}	V_{IH}	X	6V	ADD/D_{IN}	ADD
PGM Verify	V_{PP}	V_{IH}	V_{IH}	V_{IL}	V_{IL}	X	6V	ADD/D_{OUT}	ADD
PGM Inhibit	V_{PP}	V_{IH}	V_{IH}	V_{IH}	V_{IH}	X	6V	Hi-Z	Hi-Z
Preload/Observe	⎍	D_{IN}	X	X	V_H[2]	$\overline{OE}$	5V	Hi-Z	D_{OUT}

NOTES:
1. X can be V_{IL} or V_{IH}.
2. V_H = 11.0V to 14.0V.

SECURITY FUSE USAGE

A single fuse is provided to prevent unauthorized copying of the PLV5000 fuse patterns. Once programmed, the outputs appear programmed during verify. The security fuse should be programmed last (after verifying all other programmed bits), as its effect is immediate.

The security fuse also inhibits Preload and Observability.

ERASURE CHARACTERISTICS

The entire memory array of a PLV5000 is erased after exposure to ultraviolet light at a wavelength of 2537Å. Complete erasure is assured after a minimum of 20 minutes exposure using 12,000 $\mu W/cm^2$ intensity lamps spaced one inch away from the chip. Minimum erase time for lamps at other intensity ratings can be calculated from the minimum integrated erasure dose of 15W·sec/cm^2. To prevent unintentional erasure, an opaque label is recommended to cover the clear window on any UV erasable PLD which will be subjected to continuous fluorescent indoor lighting or sunlight.

High density UV erasable programmable logic device

PLV5000/L

DEFINITIONS

Data Sheet Identification	Product Status	Definition
Objective Specification	Formative or In Design	This data sheet contains the design target or goal specifications for product development. Specifications may change in any manner without notice.
Preliminary Specification	Preproduction Product	This data sheet contains preliminary data, and supplementary data will be published at a later date. Signetics reserves the right to make changes at any time without notice in order to improve design and supply the best possible product.
Product Specification	Full Production	This data sheet contains Final Specifications. Signetics reserves the right to make changes at any time without notice, in order to improve design and supply the best possible product.

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Argentina: PHILIPS ARGENTINA S.A., Div. Philips Components, Vedia 3892, 1430 BUENOS AIRES, Tel. (01) 541-4261.
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