16-BIT, 500-MSPS, 2×–16× INTERPOLATING DUAL-CHANNEL DIGITAL-TO-ANALOG CONVERTER

FEATURES

- **500 MSPS Maximum Update Rate DAC**
- **WCDMA ACPR**
  - **1 Carrier: 76 dB Centered at 30.72-MHz IF, 245.76 MSPS**
  - **1 Carrier: 73 dB Centered at 61.44-MHz IF, 245.76 MSPS**
  - **2 Carrier: 72 dB Centered at 30.72-MHz IF, 245.76 MSPS**
  - **4 Carrier: 64 dB Centered at 92.16-MHz IF, 491.52 MSPS**
- **Selectable 2×, 4×, 8×, and 16× Interpolation**
  - **Linear Phase**
  - **0.05-dB Pass-Band Ripple**
  - **80-dB Stop-Band Attenuation**
  - **Stop-Band Transition 0.4–0.6 f_{DATA}**
- **32-Bit Programmable NCO**
- **On-Chip 2×–16× PLL Clock Multiplier With Bypass Mode**
- **Differential Scalable Current Outputs: 2 mA to 20 mA**
- **On-Chip 1.2-V Reference**
- **1.8-V Digital and 3.3-V Analog Supplies**
- **1.8-V/3.3-V CMOS Compatible Interface**
- **Power Dissipation: 950 mW at Full Maximum Operating Conditions**
- **Package: 100-Pin HTQFP**

APPLICATIONS

- **Cellular Base Transceiver Station Transmit Channel**
  - **CDMA: W-CDMA, CDMA2000, IS-95**
  - **TDMA: GSM, IS-136, EDGE/UWC-136**
- **Baseband I and Q Transmit**
- **Input Interface: Quadrature Modulation for Interfacing With Baseband Complex Mixing ASICs**
- **Single-Sideband Up-Conversion**
- **Diversity Transmit**
- **Cable Modem Termination System**

DESCRIPTION

The DAC5686 is a dual-channel 16-bit high-speed digital-to-analog converter (DAC) with integrated 2×, 4×, 8×, and 16× interpolation filters, a numerically controlled oscillator (NCO), onboard clock multiplier, and on-chip voltage reference. The DAC5686 has been specifically designed to allow for low input data rates between the DAC and ASIC, or FPGA, and high output transmit intermediate frequencies (IF). Target applications include high-speed digital data transmission in wired and wireless communication systems and high-frequency direct-digital synthesis DDS.

The DAC5686 provides three modes of operation: dual-channel, single-sideband, and quadrature modulation. In dual-channel mode, interpolation filtering increases the DAC update rate, which reduces sinx/x rolloff and enables the use of relaxed analog post-filtering.

Single-sideband mode provides an alternative interface to the analog quadrature modulators. Channel carrier selection is performed at baseband by mixing in the ASIC/FPGA. Baseband I and Q from the ASIC/FPGA are input to the DAC5686, which in turn performs a complex mix resulting in Hilbert transform pairs at the outputs of the DAC5686's two DACs. An external RF quadrature modulator then performs the final single-sideband up-conversion. The DAC5686's complex mixing frequencies are flexibly chosen with the 32-bit programmable NCO.

Unmatched gains and offsets at the RF quadrature modulator result in unwanted sideband and local oscillator feedthrough. Each DAC in the DAC5686 has an 11-bit offset adjustment and 12-bit gain adjustment, which compensate for quadrature modulator input imbalances, thus reducing RF filtering requirements.

In quadrature modulation mode, on-chip mixing provides baseband-to-IF up-conversion. Mixing frequencies are flexibly chosen with a 32-bit programmable NCO. Channel carrier selection is performed at baseband by complex mixing in the ASIC/FPGA. Baseband I and Q from the ASIC/FPGA are input to the DAC5686, which interpolates the low data-rate signal to higher data rates. The single DAC output from the DAC5686 is the final IF single-sideband spectrum presented to RF.

The 2×, 4×, 8×, and 16× interpolation filters are implemented as a cascade of half-band 2× interpolation filters. Unused filters for interpolation rates of less than 16× are shut off to reduce power consumption. The DAC5686 provides a full bypass mode, which enables the user to bypass all the interpolation and mixing.

The DAC5686 PLL clock multiplier controls all internal clocks for the digital filters and the DAC cores. The differential clock input and internal clock circuitry provides for optimum jitter performance. Sine wave clock input signal is supported. The PLL can be bypassed by an external clock running at the DAC core update rate. The clock divider of the PLL ensures that the digital filters operate at the correct clock frequencies.

The DAC5686 operates with an analog supply voltage of 3.3 V and a digital supply voltage of 1.8 V. Digital I/Os are 1.8-V and 3.3-V CMOS compatible. Power dissipation is 950 mW at maximum operating conditions. The DAC5686 provides a nominal full-scale differential current output of 20 mA, supporting both single-ended and differential applications. The output current can be directly fed to the load with no additional external output buffer required. The device has been specifically designed for a differential transformer-coupled output with a 50-Ω doubly terminated load. For a 20-mA full-scale output current, both a 4:1 impedance ratio (resulting in an output power of 4 dBm) and 1:1 impedance ratio transformer (–2-dBm output power) are supported.

The DAC5686 operational modes are configured by programming registers through a serial interface. The serial interface can be configured to either a 3- or 4-pin interface allowing it to communicate with many industry-standard microprocessors and microcontrollers. Data (I and Q) can be input to the DAC5686 as separate parallel streams on two data buses, or as a single interleaved data stream on one data bus.

An accurate on-chip 1.2-V temperature-compensated band-gap reference and control amplifier allows the user to adjust the full-scale output current from 20 mA down to 2 mA. This provides 20-dB gain range control capabilities. Alternatively, an external reference voltage can be applied for maximum flexibility. The device features a SLEEP mode, which reduces the standby power to approximately 10 mW, thereby minimizing the system power consumption.

The DAC5686 is available in a 100-pin HTQFP package. The device is characterized for operation over the industrial temperature range of –40°C to 85°C.

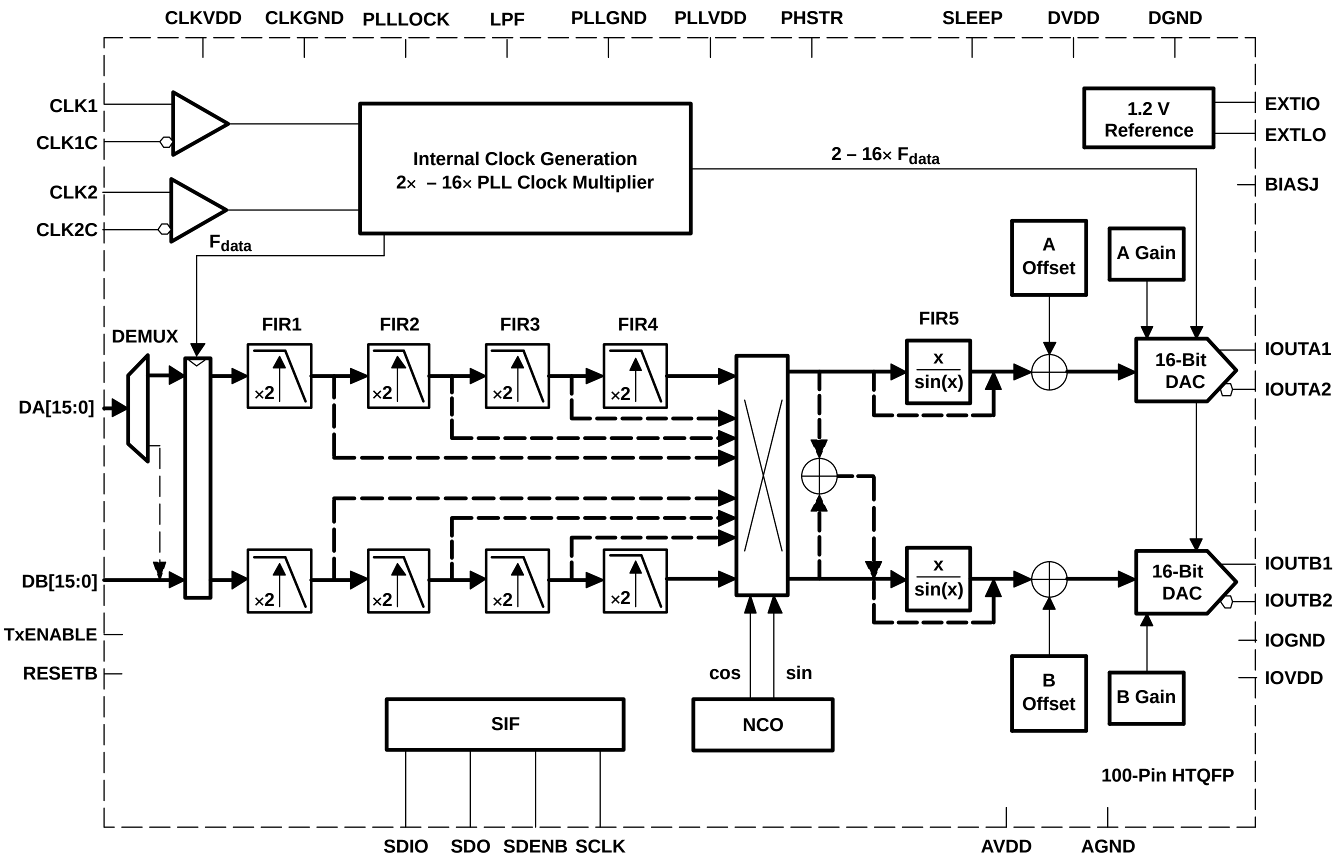
ORDERING INFORMATION

T_A	PACKAGE DEVICES
–40°C to 85°C	100 HTQFP(1) (PZP) PowerPAD™ Plastic Quad Flatpack
	DAC5686IPZP

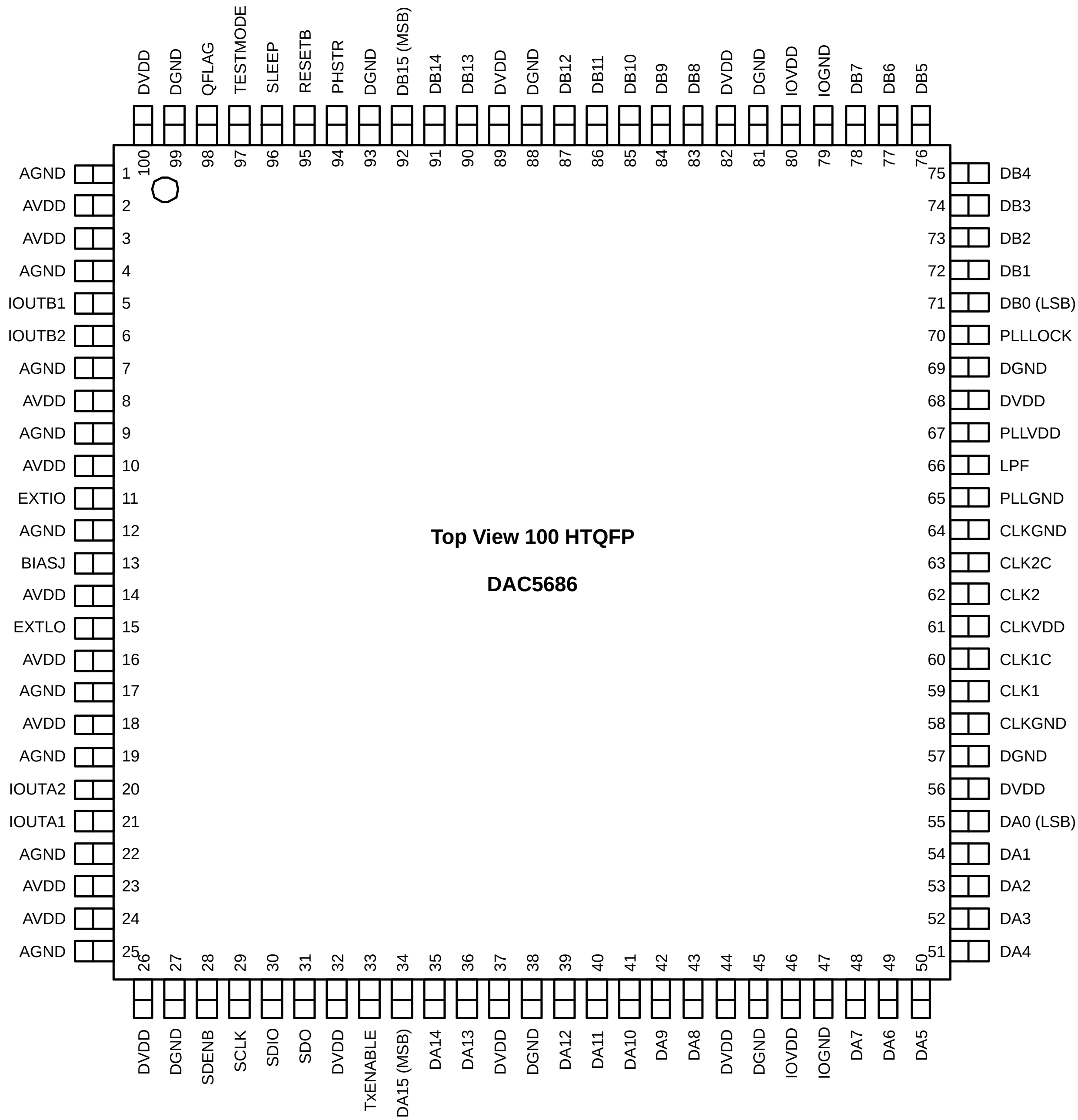
(1) Thermal pad size: 6 mm × 6 mm

FUNCTIONAL BLOCK DIAGRAM

Block Diagram of the DAC5686



PIN ASSIGNMENTS FOR THE DAC5686



DEVICE INFORMATION

Terminal Functions

TERMINAL NAME	TERMINAL NO.	I/O	DESCRIPTION
AGND	1, 4, 7, 9, 12, 17, 19, 22, 25	I	Analog ground return
AVDD	2, 3, 8, 10, 14, 16, 18, 23, 24	I	Analog supply voltage

DEVICE INFORMATION (continued)

Terminal Functions (continued)

TERMINAL NAME	TERMINAL NO.	I/O	DESCRIPTION
BIASJ	13	I/O	Full-scale output current bias
CLK1	59	I	External clock input; data clock input
CLK1C	60	I	Complementary external clock input; data clock input
CLK2	62	I	External clock input; sample clock for the DAC (optional if PLL disabled)
CLK2C	63	I	Complementary external clock input; sample clock for the DAC (optional if PLL disabled)
CLKGND	58, 64		Ground return for internal clock buffer
CLKVDD	61		Internal clock buffer supply voltage
DA[15:0]	34–36, 39–43, 48–55	I	A-channel data bits 0 through 15 DA15 is most significant data bit (MSB). DA0 is least significant data bit (LSB).
DB[0:15]	71–78, 83–87, 90–92	I	B-channel data bits 0 through 15 DB15 is most significant data bit (MSB). DB0 is least significant data bit (LSB). Note: The order of the B data bus can be reversed by register rev_bbus.
DGND	27, 38, 45, 57, 69, 81, 88, 93, 99		Digital ground return
DVDD	26, 32, 37, 44, 56, 68, 82, 89, 100		Digital supply voltage
EXTIO	11	I	Used as external reference input when internal reference is disabled (i.e., EXTLO connected to AVDD). Used as internal reference output when EXTLO = AGND, requires a 0.1-µF decoupling capacitor to AGND when used as reference output
EXTLO	15	I	Internal reference ground. Connect to AVDD to disable the internal reference
IOUTA1	21	O	A-channel DAC current output. Full scale when all input bits are set to 1
IOUTA2	20	O	A-channel DAC complementary current output. Full scale when all input bits are set to 0
IOUTB1	5	O	B-channel DAC current output. Full scale when all input bits are set to 1
IOUTB2	6	O	B-channel DAC complementary current output. Full scale when all input bits are set to 0
IOGND	47, 79		Digital I/O ground return
IOVDD	46, 80		Digital I/O supply voltage
LPF	66	I/O	PLL loop filter connection. Can be left open or connected to GND if PLL is not used (PLLVDD = 0 V).
PHSTR	94	I	The PHSTR pin has two functions. When the sync_phstr register is 0, a high on the PHSTR pin resets the NCO phase accumulator. When the sync_phstr register is 1, a PHSTR pin low-to-high transition sets the divided clock phase in external clock mode, and a high on the PHSTR pin resets the NCO phase accumulator.
PLLGND	65		Ground return for internal PLL
PLLVDD	67		PLL supply voltage. When PLLVDD is 0 V, the PLL is disabled.
PLLLOCK	70	O	PLL lock status bit. In PLL clock mode, PLLLOCK is high when PLL is locked to the input clock. In external clock mode, PLLLOCK outputs the input rate clock.
QFLAG	98	O	Used in the interleaved data input mode: When the qflag register bit is 1, the QFLAG pin is used as an output to identify the interleaved data sequence. QFLAG high identifies the data as channel B. Pin can be left open when not used.
RESETB	95	I	Resets the chip when low
SCLK	29	I	Serial interface clock
SDENB	28	I	Active-low serial data enable, always an input to the DAC5686
SDIO	30	I/O	Bidirectional serial-port data in the three-pin serial interface mode. Input-only serial data in the four-pin serial interface mode.
SDO	31	O	High-impedance state (the pin is not used) in the three-pin serial interface mode. Serial-port output data in the four-pin serial interface mode.
SLEEP	96	I	Asynchronous hardware power-down input. Active high. Internal pulldown
TESTMODE	97	I	TESTMODE is DGND for the user.

DEVICE INFORMATION (continued)

Terminal Functions (continued)

TERMINAL NAME	TERMINAL NO.	I/O	DESCRIPTION
TxENABLE	33	I	TxENABLE is used in interleaved mode. The rising edge of TxENABLE synchronizes the data of channels A and B. The first data after the rising edge of TxENABLE is treated as A data, while the next data is treated as B data and so on. In any mode, TxENABLE being low sets DAC outputs to midscale. Internal pulldown

ABSOLUTE MAXIMUM RATINGS

over operating free-air temperature range (unless otherwise noted) (1)

		UNIT
Supply voltage range	AVDD (2)	–0.5 V to 4 V
	DVDD (3)	–0.5 V to 2.3 V
	CLKVDD (2)	–0.5 V to 4 V
	IOVDD (2)	–0.5 V to 4 V
	PLLVDD (2)	–0.5 V to 4 V
Voltage between AGND, DGND, CLKGND, PLLGND, and IOGND		–0.5 V to 0.5 V
Supply voltage range	AVDD to DVDD	–0.5 V to 2.6 V
	DA[15:0] (3)	–0.5 V to IOVDD + 0.5 V
	DB[15:0] (3)	–0.5 V to IOVDD + 0.5 V
	SLEEP (3)	–0.5 V to IOVDD + 0.5 V
	CLK1, CLK2, CLK1C, CLK2C (3)	–0.5 V to CLKVDD + 0.5 V
	RESETB (3)	–0.5 V to IOVDD + 0.5 V
	LPF (3)	–0.5 V to PLLVDD + 0.5 V
	IOUT1, IOUT2 (2)	–1 V to AVDD + 0.5 V
	EXTIO, BIASJ (2)	–0.5 V to AVDD + 0.5 V
	EXTLO (2)	–0.5 V to IOVDD + 0.5 V
Peak input current (any input)		±20 mA
Operating free-air temperature range, T_A: DAC5686I		–40°C to 85°C
Storage temperature range		–65°C to 150°C
Lead temperature 1,6 mm (1/16 inch) from the case for 10 seconds		260°C

(1) Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) Measured with respect to AGND
(3) Measured with respect to DGND

ELECTRICAL CHARACTERISTICS (DC SPECIFICATIONS)(1)

over operating free-air temperature range, AVDD = 3.3 V, CLKVDD = 3.3 V, PLLVDD = 3.3 V, IOVDD = 3.3 V, DVDD = 1.8 V, $IOUT_{FS}$ = 20 mA (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
Resolution			16			
DC Accuracy (2)						
INL	Integral nonlinearity	1 LSB = $IOUT_{FS}$/216, T_{MIN} to T_{MAX}		±12		LSB
DNL	Differential nonlinearity			1.84e–4		$IOUT_{FS}$
				±9		LSB
				1.37e–4		$IOUT_{FS}$

(1) Specifications subject to change without notice.
(2) Measured differential across IOUTA1 and IOUTA2 or IOUTB1 and IOUTB2 with 25 Ω each to AVDD

ELECTRICAL CHARACTERISTICS (DC SPECIFICATIONS) (continued)

over operating free-air temperature range, AVDD = 3.3 V, CLKVDD = 3.3 V, PLLVDD = 3.3 V, IOVDD = 3.3 V, DVDD = 1.8 V, $IOUT_{FS}$ = 20 mA (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
Analog Output						
	Coarse gain linearity (INL)	LSB = 1/10th of full scale		±0.016		LSB
	Fine gain linearity (INL)			±3		LSB
	Offset error	Mid-code offset		0.003		%FSR
	Gain error	Without internal reference		0.7		%FSR
		With internal reference		0.7		
	Gain mismatch	With internal reference, dual DAC, SSB mode	–2		2	%FSR
	Full-scale output current(3)		2		20	mA
	Output compliance range(4)	$IOUT_{FS}$ = 20 mA	AVDD – 0.5		AVDD + 0.5	V
	Output resistance			300		kΩ
	Output capacitance			5		pF
Reference Output						
	Reference voltage		1.14	1.2	1.26	V
	Reference output current(5)			100		nA
Reference Input						
V_{EXTIO}	Input voltage range		0.1		1.25	V
	Input resistance			1		MΩ
	Small-signal bandwidth			2.5		kHz
	Input capacitance			100		pF
Temperature Coefficients						
	Offset drift			±3		ppm of FSR/°C
	Gain drift	Without internal reference		±15		ppm of FSR/°C
		With internal reference		±40		
	Reference voltage drift			±25		ppm/°C
Power Supply						
AVDD	Analog supply voltage		3	3.3	3.6	V
DVDD	Digital supply voltage		1.65	1.8	1.95	V
CLKVDD	Clock supply voltage		3	3.3	3.6	V
IOVDD	I/O supply voltage		1.65		3.6	V
PLLVDD	PLL supply voltage		3	3.3	3.6	V
I_{AVDD}	Analog supply current	Single (quad) DAC mode; including output current through load resistor, mode 7		30		mA
		Dual DAC mode; including output current through load resistor, mode 11			55	
I_{DVDD}	Digital supply current	f_{DATA} = 125 MSPS, SSB mode, F_{update} = 500 MSPS, 40-MHz IF		242		mA
I_{CLKVDD}	Clock supply current			10		mA
I_{PLLVDD}	PLL supply current			28		mA
I_{IOVDD}	IO supply current			< 3		mA

(3) Nominal full-scale current, $IOUT_{FS}$, equals 16× the IBIAS current.
(4) The upper limit of the output compliance is determined by the CMOS process. Exceeding this limit may result in transistor breakdown, resulting in reduced reliability of the DAC5686 device. The lower limit of the output compliance is determined by the load resistors and full-scale output current. Exceeding the upper limit adversely affects distortion performance and integral nonlinearity.
(5) Use an external buffer amplifier with high-impedance input to drive any external load.

ELECTRICAL CHARACTERISTICS (DC SPECIFICATIONS) (continued)

over operating free-air temperature range, AVDD = 3.3 V, CLKVDD = 3.3 V, PLLVDD = 3.3 V, IOVDD = 3.3 V, DVDD = 1.8 V, $IOUT_{FS}$ = 20 mA (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
I_{AVDD}	Sleep mode, AVDD supply current	Sleep mode		1		mA
I_{DVDD}	Sleep mode, DVDD supply current			4		mA
I_{CLKVDD}	Sleep mode, CLKVDD supply current			2		mA
I_{PLLVDD}	Sleep mode, PLLVDD supply current			0.5		mA
I_{IOVDD}	Sleep mode, IOVDD supply current			0.25		mA
P_D	Power dissipation	Mode 1(6) AVDD = 3.3 V, DVDD = 1.8 V		215		mW
		Mode 2(7) AVDD = 3.3 V, DVDD = 1.8 V		495		
		Mode 5(8) AVDD = 3.3 V, DVDD = 1.8 V		445		
		Mode 7(9) AVDD = 3.3 V, DVDD = 1.8 V		754		
		Mode 9(10) AVDD = 3.3 V, DVDD = 1.8 V		547		
		Mode 11(11) AVDD = 3.3 V, DVDD = 1.8 V		855	950	
APSRR	Power supply rejection ratio		–0.2		0.2	%FSR/V
DPSRR	Power supply rejection ratio		–0.2		0.2	%FSR/V

(6) Mode 1: Dual DAC mode, fully bypassed, F_{DAC} = 160 MSPS, f_{OUT} = 20 MHz
(7) Mode 2: Dual DAC mode, 2× interpolation, F_{DAC} = 320 MSPS, f_{OUT} = 20 MHz
(8) Mode 5: Quadrature modulation mode, 4× interpolation, fs/4 mixing, F_{DAC} = 320 MSPS, f_{OUT} = 100 MHz
(9) Mode 7: Quadrature modulation mode, 4× interpolation, NCO running at 320 MHz, F_{DAC} = 320 MSPS, f_{OUT} = 100 MHz
(10) Mode 9: SSB modulation mode, 4× interpolation, fs/4 mixing, F_{DAC} = 320 MSPS, f_{OUT} = 100 MHz
(11) Mode 11: SSB modulation mode, 4× interpolation, NCO running at 320 MHz, f_{OUT} = 100 MHz, maximum operating condition

ELECTRICAL CHARACTERISTICS (AC SPECIFICATIONS)(1)

over operating free-air temperature range, AVDD = 3.3 V, CLKVDD = 3.3 V, PLLVDD = 0 V, IOVDD = 3.3 V, DVDD = 1.8 V, $IOUT_{FS}$ = 20 mA, external clock mode, differential transformer-coupled output, 50-Ω doubly terminated load (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
Analog Output						
f_{CLK}	Maximum output update rate		500			MSPS
$t_{s(DAC)}$	Output settling time to 0.1%	Mid-scale transition		12		ns
t_{pd}	Output propagation delay			2.5		ns
$t_{r(IOUT)}$ (2)	Output rise time 10% to 90%			2.5		ns
$t_{f(IOUT)}$ (2)	Output fall time 90% to 10%			2.5		ns
AC Performance—1:1 Impedance-Ratio Transformer						
SFDR	Spurious free dynamic range	First Nyquist zone < f_{DATA}/2, 4× interpolation, dual DAC mode, f_{DATA} = 52 MSPS, f_{OUT} = 14 MHz, T_A = 25°C		89		dBc
		First Nyquist zone < f_{DATA}/2, 4× interpolation, dual DAC mode, f_{DATA} = 160 MSPS, f_{OUT} = 20 MHz, full bypass, T_A = T_{MIN} to T_{MAX} for MIN, 25°C for TYP, IOVDD = 1.8 V for TYP	68	79		
		2× interpolation, dual DAC mode, f_{DATA} = 160 MSPS, f_{OUT} = 41 MHz, T_A = 25°C, IOVDD = 1.8 V		72		
		2× interpolation, dual DAC mode, f_{DATA} = 160 MSPS, f_{OUT} = 61 MHz, T_A = 25°C, IOVDD = 1.8 V		68		

(1) Specifications subject to change without notice
(2) Measured single-ended into 50-Ω load

ELECTRICAL CHARACTERISTICS (AC SPECIFICATIONS) (continued)

over operating free-air temperature range, AVDD = 3.3 V, CLKVDD = 3.3 V, PLLVDD = 0 V, IOVDD = 3.3 V, DVDD = 1.8 V, $IOUT_{FS}$ = 20 mA, external clock mode, differential transformer-coupled output, 50-Ω doubly terminated load (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
SNR	Signal-to-noise ratio	First Nyquist zone < f_{DATA}/2, f_{DATA} = 100 MSPS, f_{OUT} = 5 MHz, IOVDD = 1.8 V, f_{DAC} = 400 MSPS		80		dB
		First Nyquist zone < f_{DATA}/2, f_{DATA} = 78 MSPS, f_{OUT} = 15.6 MHz, 15.8 MHz, 16.2 MHz, 16.4 MHz, IOVDD = 1.8 V, f_{DAC} = 314 MSPS		72		
ACLR	Adjacent channel power ratio	Single carrier W-CDMA with 3.84-MHz BW, 5-MHz spacing, centered at IF, TESTMODEL 1, 10 ms, f_{DATA} = 122.88 MSPS, baseband, dual DAC, 2× interpolation, f_{OUT} = 245 MSPS		72		dB
		Single carrier W-CDMA with 3.84-MHz BW, 5-MHz spacing, centered at IF, TESTMODEL 1, 10 ms, f_{DATA} = 76.8 MSPS, IF = 19.2 MHz, dual DAC, 2× interpolation, f_{OUT} = 153.6 MSPS		77		
		Single carrier W-CDMA with 3.84-MHz BW, 5-MHz spacing, centered at IF, TESTMODEL 1, 10 ms, f_{DATA} = 122.88 MSPS, IF = 30.72 MHz, dual DAC, 2× interpolation, f_{DAC} = 245 MSPS		76		
		Single carrier W-CDMA with 3.84-MHz BW, 5-MHz spacing, centered at IF, TESTMODEL 1, 10 ms, f_{DATA} = 61.44 MSPS, IF = 61.44 MHz, quad mode, fs/4, 4× interpolation, f_{DAC} = 245 MSPS		73		
		Two-carrier W-CDMA with 3.84-MHz BW, 5-MHz spacing, centered at IF, TESTMODEL 1, 10 ms, f_{DATA} = 122.88 MSPS, IF = 30.72 MHz, dual DAC, 2× interpolation, f_{DAC} = 245 MSPS		72		
		Four-carrier W-CDMA with 3.84-MHz BW, 5-MHz spacing, centered at IF, TESTMODEL 1, 10 ms, f_{DATA} = 121.88 MSPS, complex IF - 30.72 MHz, quad mode, fs/4, 4× interpolation, IF = 92.16 MHz		64		
IMD3	Third-order two-tone intermodulation	f_{DATA} = 160 MSPS, f_{OUT} = 60.1 and 61.1 MHz, 2× interp-olation, 320 MSPS, IOVDD = 1.8 V, each tone at –6 dBFS		74		dBc
		f_{DATA} = 100 MSPS, f_{OUT} = 15.1 and 16.1 MHz, 2× interp-olation, 200 MSPS, IOVDD = 1.8 V, each tone at –6 dBFS		84		
IMD	Four-tone intermodulation	f_{DATA} = 100 MSPS, f_{OUT} = 15.6 MHz, 15.8 MHz, 16.2 MHz, 16.4 MHz, 4× interpolation, 400 MSPS, IOVDD = 1.8 V, each tone at –12 dBFS		85		dBc

ELECTRICAL CHARACTERISTICS (DIGITAL SPECIFICATIONS)(1)

over operating free-air temperature range, AVDD = 3.3 V, CLKVDD = 3.3 V, PLLVDD = 3.3 V, IOVDD = 3.3 V, DVDD = 1.8 V, $IOUT_{FS}$ = 20 mA (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
CMOS Interface						
V_{IH}	High-level input voltage		2	3		V
V_{IL}	Low-level input voltage		0	0	0.8	V
I_{IH}	High-level input current		–40		40	µA
I_{IL}	Low-level input current		–40		40	µA
	Input capacitance			5		pF
V_{OH}	High-level output voltage, PLLLOCK, SDO, SDIO (I/O)	I_L = –100 µA	IOVDD – 0.2			V
		I_L = –8 mA	0.8 × IOVDD			

(1) Specifications subject to change without notice.

ELECTRICAL CHARACTERISTICS (DIGITAL SPECIFICATIONS) (continued)

over operating free-air temperature range, AVDD = 3.3 V, CLKVDD = 3.3 V, PLLVDD = 3.3 V, IOVDD = 3.3 V, DVDD = 1.8 V, $IOUT_{FS}$ = 20 mA (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{OL}	Low-level output voltage, PLLLOCK, SDO, SDIO (I/O)	I_L = 100 µA			0.2	V
		I_L = 8 mA			0.22 × IOVDD	
PLL						
	Input data rate supported		1		160	MSPS
	Phase noise	At 600-kHz offset, measured at DAC output, 25-MHz 0-dBFS tone, f_{DATA} = 125 MSPS, 4× interpolation		128		dBc/Hz
		At 6-MHz offset, measured at DAC output, 25-MHz 0-dBFS tone, f_{DATA} = 125 MSPS, 4× interpolation		151		
	VCO minimum frequency	PLL_rng = 00 (nominal)			120	MHz
	VCO maximum frequency	PLL_rng = 00 (nominal)	500			MHz
NCO						
	NCO clock (DAC update rate)				320	MHz
Serial Port Timing						
$t_{su(SDENB)}$	Setup time, SDENB to rising edge of SCLK		20			ns
$t_{su(SDIO)}$	Setup time, SDIO valid to rising edge of SCLK		10			ns
$t_{h(SDIO)}$	Hold time, SDIO valid to rising edge of SCLK		5			ns
t_{SCLK}	Period of SCLK		100			ns
t_{SCLKH}	High time of SCLK		40			ns
t_{SCLKL}	Low time of SCLK		40			ns
$t_{d(Data)}$	Data output delay after falling edge of SCLK			10		ns
Parallel Data Input Timing (PLL Mode, CLK1 Input)						
$t_{su(DATA)}$	Setup time, data valid to rising edge of CLK1		0.3	–0.4		ns
$t_{h(DATA)}$	Hold time, data valid after rising edge of CLK1		1.2	0.6		ns
Parallel Data Input Timing (Dual Clock Mode, CLK1 and CLK2 Input)						
$t_{su(DATA)}$	Setup time, data valid to rising edge of CLK1			–0.4		ns
$t_{h(DATA)}$	Hold time, data valid after rising edge of CLK1			0.6		ns
Timing Parallel Data Input (External Clock Mode, CLK2 Input)						
$t_{su(DATA)}$	Setup time, DATA valid to rising edge of PLLLOCK	High-impedance load on PLLLOCK. Note that t_{su} increases with a lower-impedance load.	4.6	3		ns
$t_{h(DATA)}$	Hold time, DATA valid after rising edge of PLLLOCK	High-impedance load on PLLLOCK. Note that t_h decreases (becomes more negative) with a lower-impedance load.	–0.8	–2.4		ns
$t_{d(PLLLock)}$	Delay from CLK2 rising edge to PLLLOCK rising edge	High-impedance load on PLLLOCK. Note that PLLLOCK delay increases with a lower-impedance load.	2.5	4.2	6.5	ns

TYPICAL CHARACTERISTICS

INTEGRAL NONLINEARITY
vs
INPUT CODE

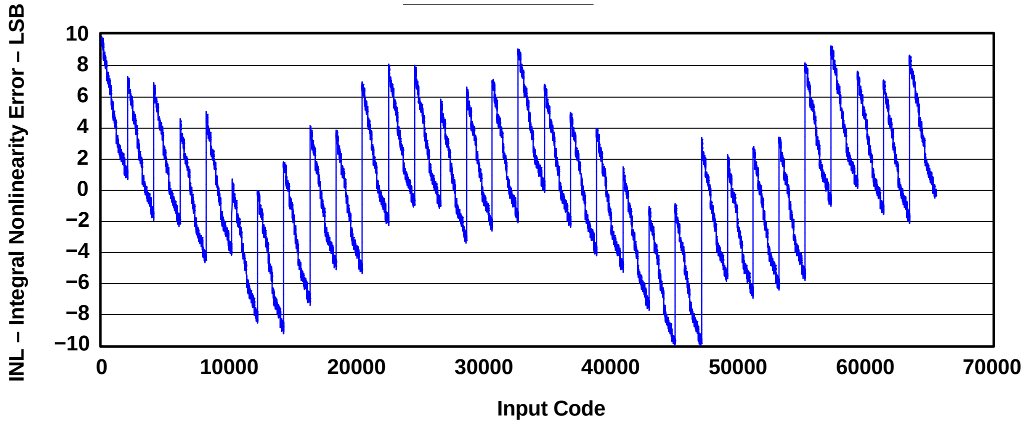


Figure 1.

DIFFERENTIAL NONLINEARITY
vs
INPUT CODE

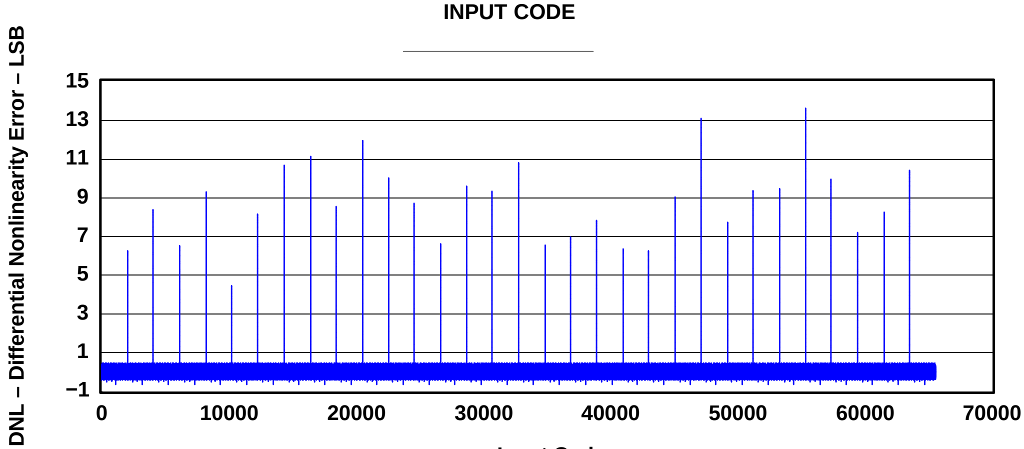


Figure 2.

TYPICAL CHARACTERISTICS (continued)

SINGLE-TONE SPECTRUM

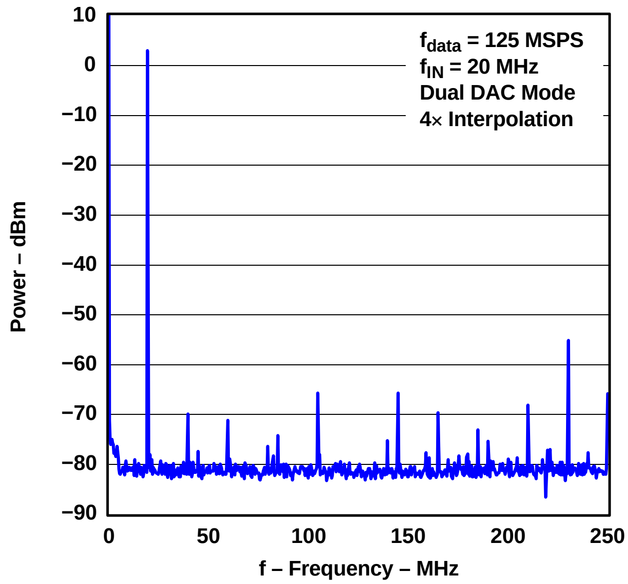


Figure 3.

IN-BAND SPURIOUS-FREE DYNAMIC RANGE
vs
OUTPUT FREQUENCY

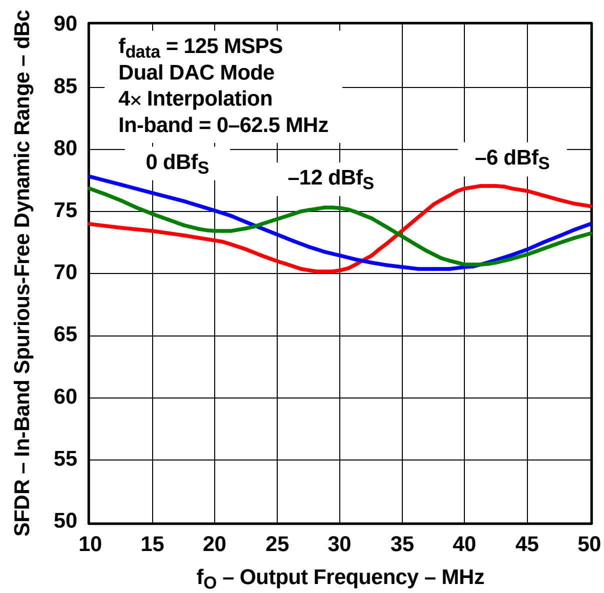


Figure 4.

OUT-OF-BAND SPURIOUS-FREE DYNAMIC RANGE
vs
OUTPUT FREQUENCY

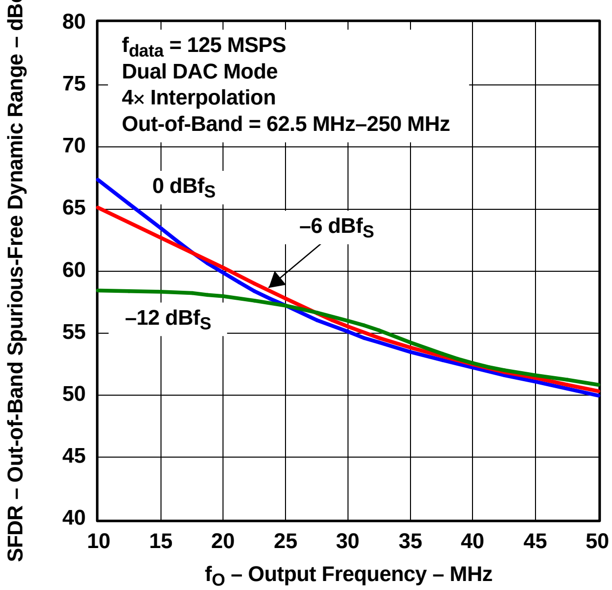


Figure 5.

SINGLE-TONE SPECTRUM

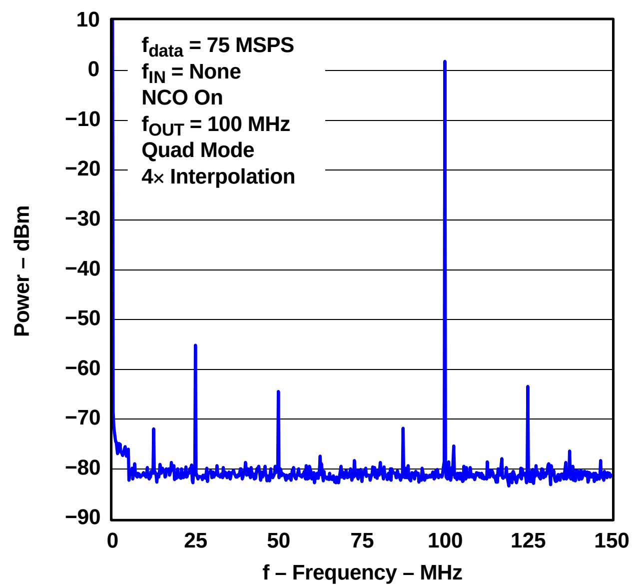


Figure 6.

TYPICAL CHARACTERISTICS (continued)

TWO-TONE IMD3 vs OUTPUT FREQUENCY

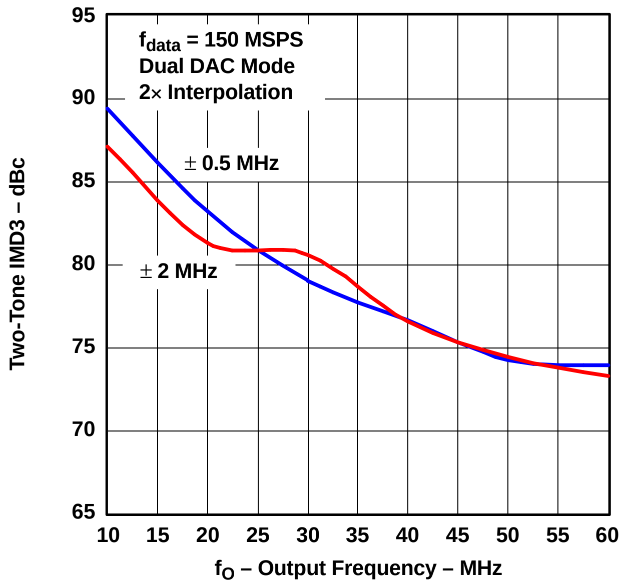


Figure 7.

TWO-TONE IMD PERFORMANCE

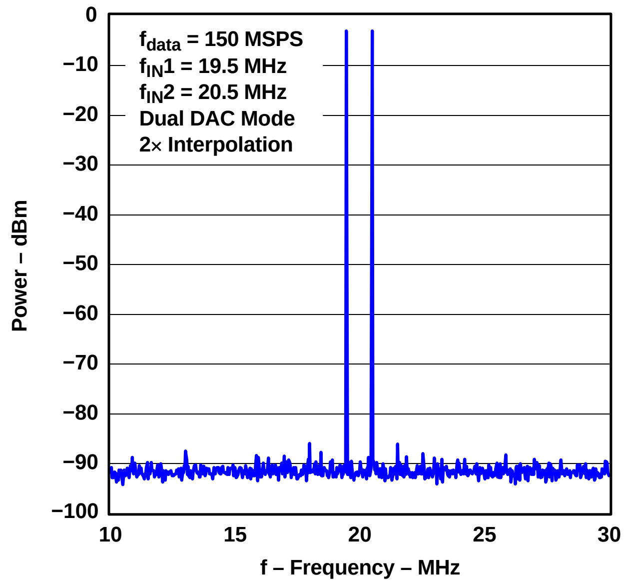


Figure 8.

TWO-TONE IMD3 vs OUTPUT FREQUENCY

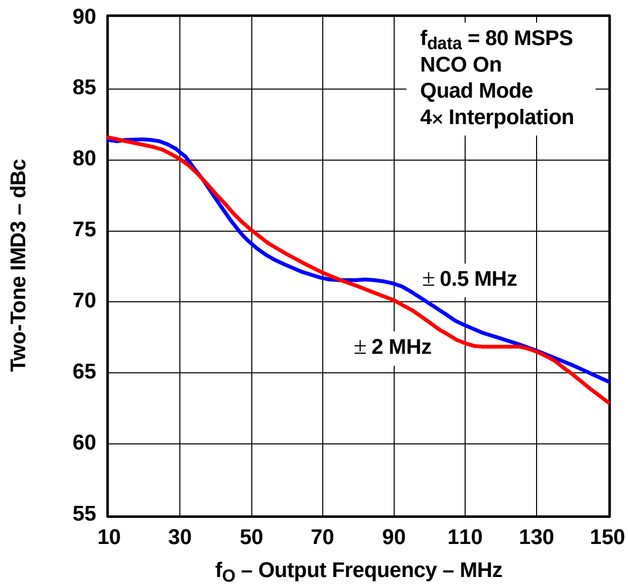


Figure 9.

TWO-TONE IMD PERFORMANCE

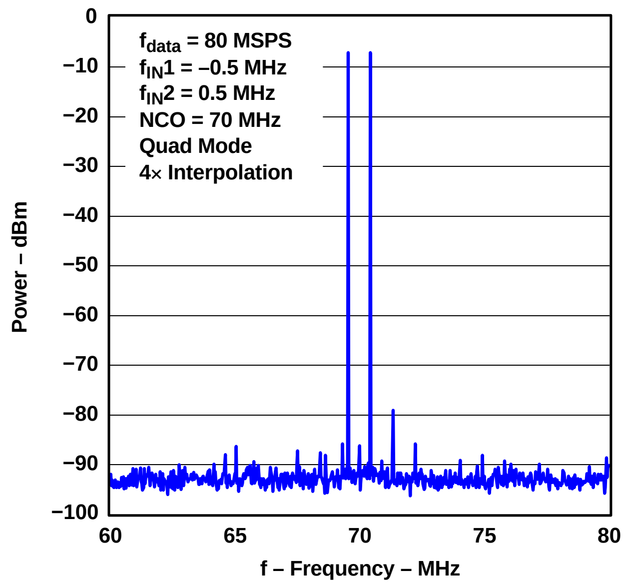


Figure 10.

TYPICAL CHARACTERISTICS (continued)

TWO-TONE IMD PERFORMANCE

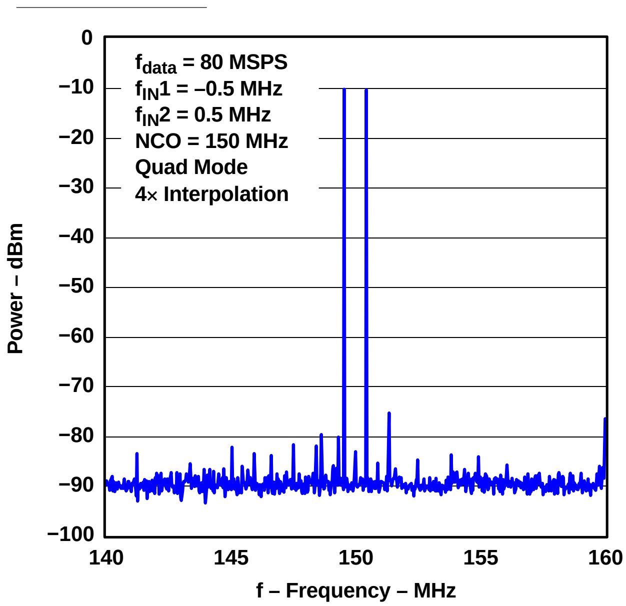


Figure 11.

WCDMA TEST MODEL 1: SINGLE CARRIER

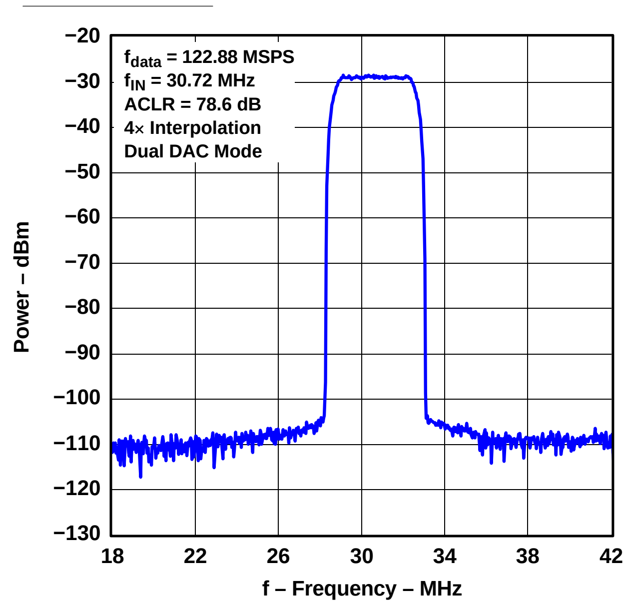


Figure 12.

WCDMA TEST MODEL 1: DUAL CARRIER

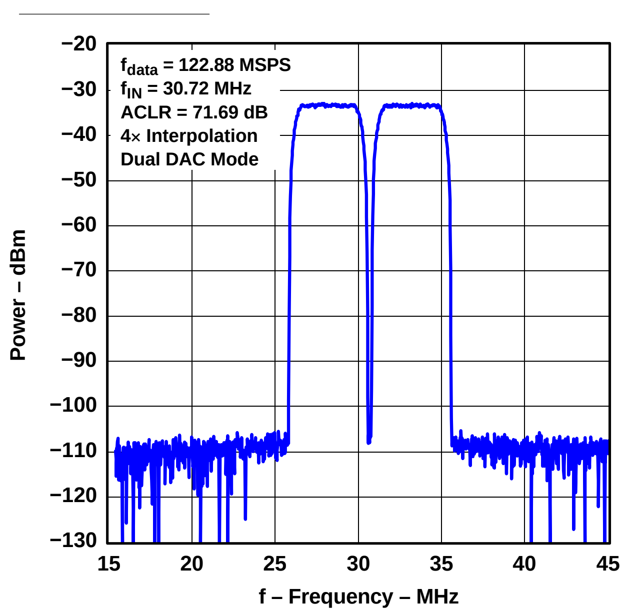


Figure 13.

WCDMA TEST MODEL 1: DUAL CARRIER

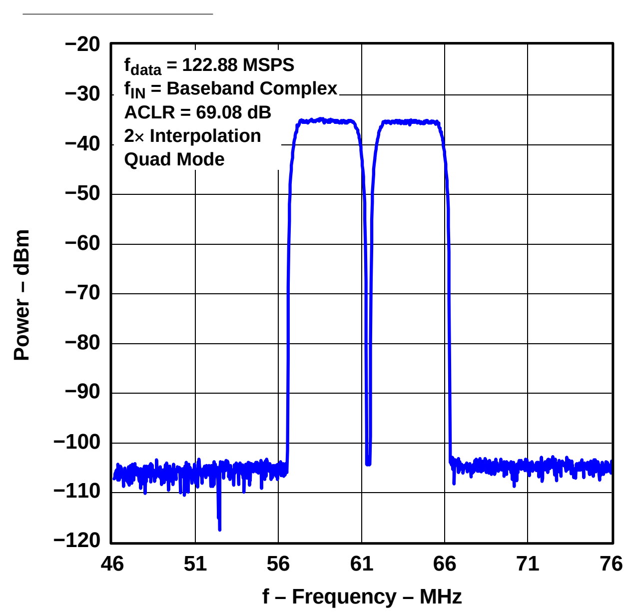


Figure 14.

TYPICAL CHARACTERISTICS (continued)

WCDMA TEST MODEL 1: FOUR CARRIER

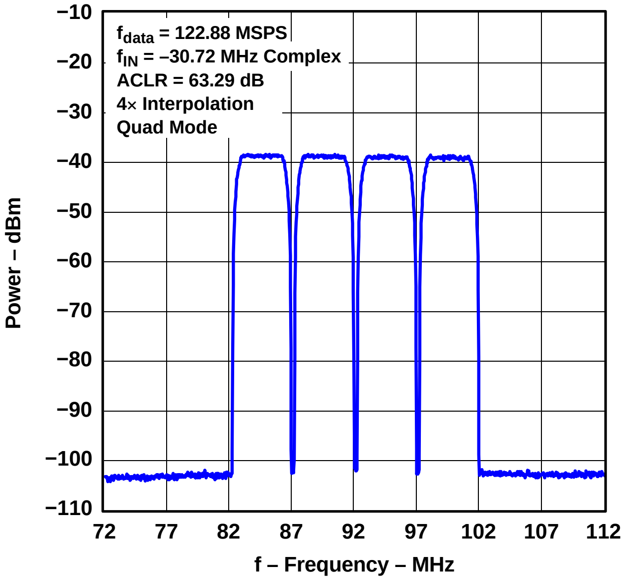


Figure 15.

WCDMA TEST MODEL 1: DUAL CARRIER

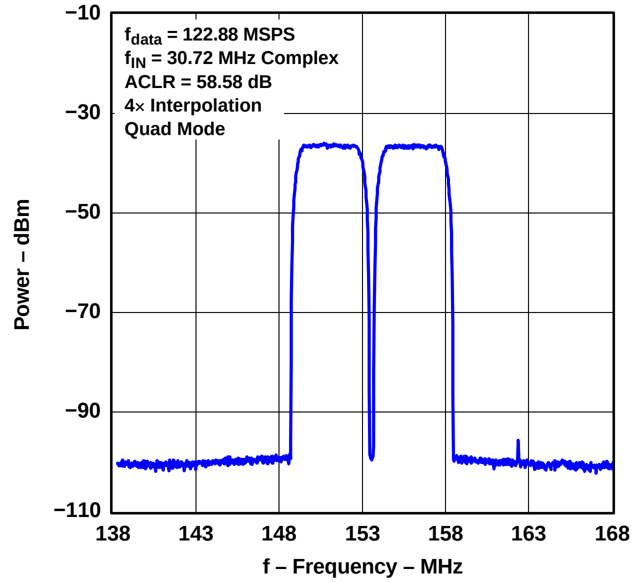


Figure 16.

VCO GAIN vs VCO FREQUENCY

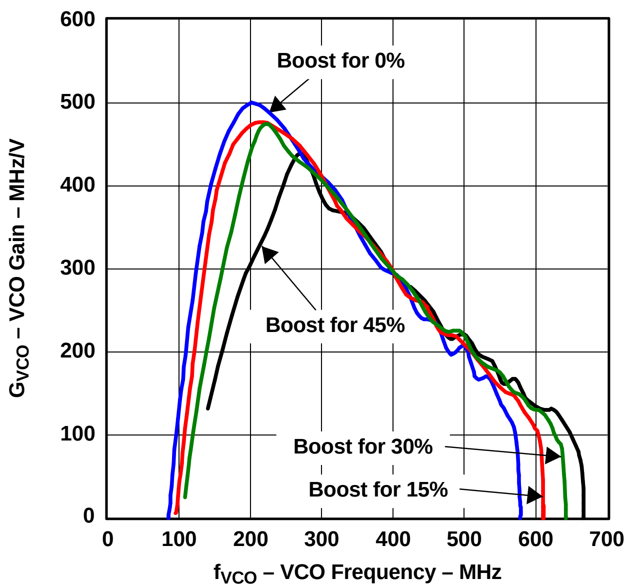


Figure 17.

DETAILED DESCRIPTION

Dual-Channel Mode

In dual-channel mode, interpolation filtering increases the DAC update rate, thereby reducing sinx/x rolloff and enabling relaxed analog post-filtering, and is useful for baseband I and Q modulation or two-channel low-IF signals. The dual-channel mode is set by **mode[1:0]** = 00 in the config_lsb register. Figure 18 shows the data path architecture in dual-channel mode. The A- and B-data paths, which are independent, consist of four cascaded half-band interpolation filters, followed by an optional inverse sinc filter. Interpolation filtering is selected as 2×, 4×, 8×, or 16× by **sel[1:0]** in the config_lsb register. Magnitude spectral responses of each filter are presented following in the section on digital filtering. Full bypass of all the interpolation filters is selected by **fbypass** in the config_lsb register. The inverse sinc filter is intended for use in single-sideband and quadrature modulation modes and is of limited benefit in dual-channel mode.

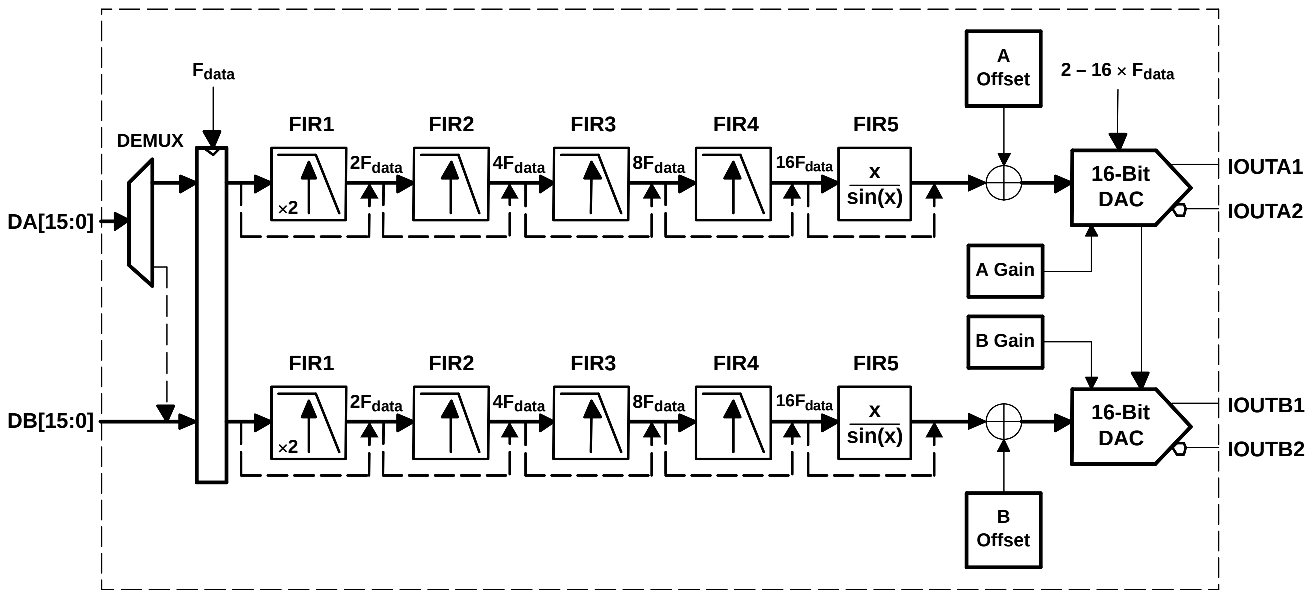


Figure 18. Data Path in Dual-Channel Mode

Single-Sideband Mode

Single-sideband (SSB) mode provides optimum interfacing to analog quadrature modulators. The SSB mode is selected by **mode[1:0]** = 01 in the config_lsb register. Figure 19 shows the data path architecture in single-sideband mode. Complex baseband I and Q are input to the DAC5686, which in turn performs a complex mix, resulting in Hilbert transform pairs at the outputs of the DAC5686's two DACs. NCO mixing frequencies are programmed through 32-bit **freq** (4 registers); 16-bit phase adjustments are programmed through **phase** (2 registers). The NCO operates at the DAC update rate; thus, increased amounts of interpolation allow for higher IFs. More details for the NCO are provided as follows. For mixing to $F_{dac}/4$, DAC5686 provides a specific architecture that exploits the {… –1 0 1 0 …} resultant streams from sin and cos; the NCO is shut off in this mode to conserve power. $F_{dac}/4$ mix mode is implemented by deasserting **nco** in register config_msb while in single-sideband or quadrature modulation mode.

DETAILED DESCRIPTION (continued)

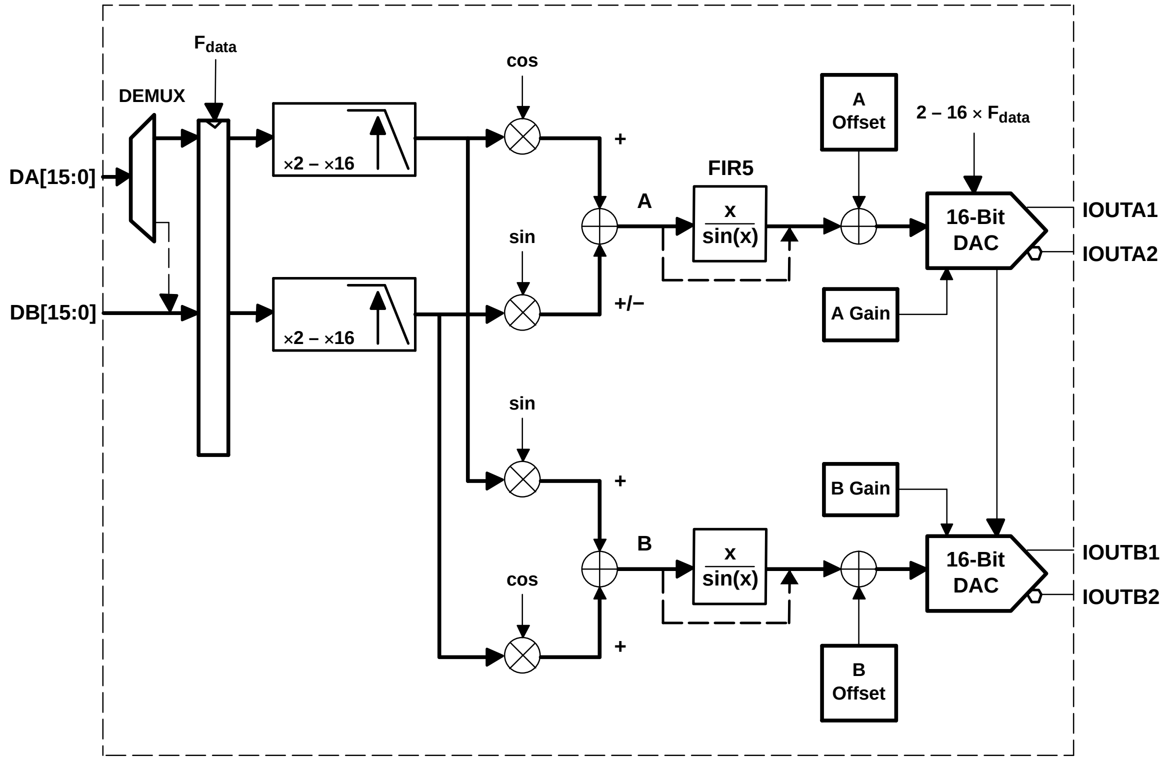


Figure 19. Data Path in SSB Mode

Figure 20 shows the DAC5686 interfaced to an RF quadrature modulator. The outputs of the complex mixer stage can be expressed as:

$$A(t) = I(t)\cos(\omega_c t) - Q(t)\sin(\omega_c t) = m(t)$$

$$B(t) = I(t)\sin(\omega_c t) + Q(t)\cos(\omega_c t) = m_h(t)$$

where m(t) and $m_h(t)$ connote a Hilbert transform pair. Upper single-sideband up-conversion is achieved at the output of the analog quadrature modulator, whose output is expressed as:

$$IF(t) = A(t)\cos(\omega_c + \omega_1)t - B(t)\sin(\omega_c + \omega_1)t$$

Flexibility is provided to the user by allowing for the selection of –B(t) out, which results in lower-sideband up-conversion. This option is selected by **ssb** in the config_msb register. Figure 21 depicts the magnitude spectrum along the signal path during single-sideband up-conversion for real input. Further flexibility is provided to the user by allowing for the inverse of sin to be used in the complex mixer by programming **rspect** in the config_usb register. The four combinations of rspect and ssb allow the user to select one of four complex spectral bands to input to a quadrature modulator (see Figure 22).

DETAILED DESCRIPTION (continued)

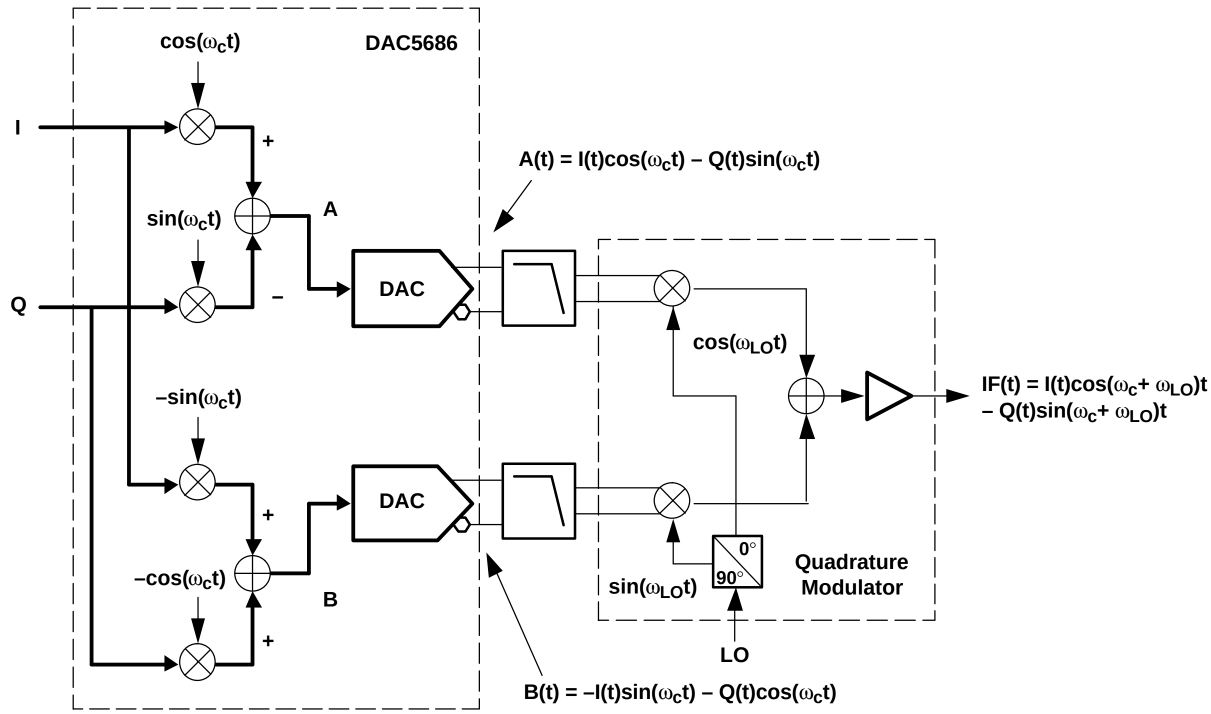


Figure 20. DAC5686 in SSB Mode With Quadrature Modulator

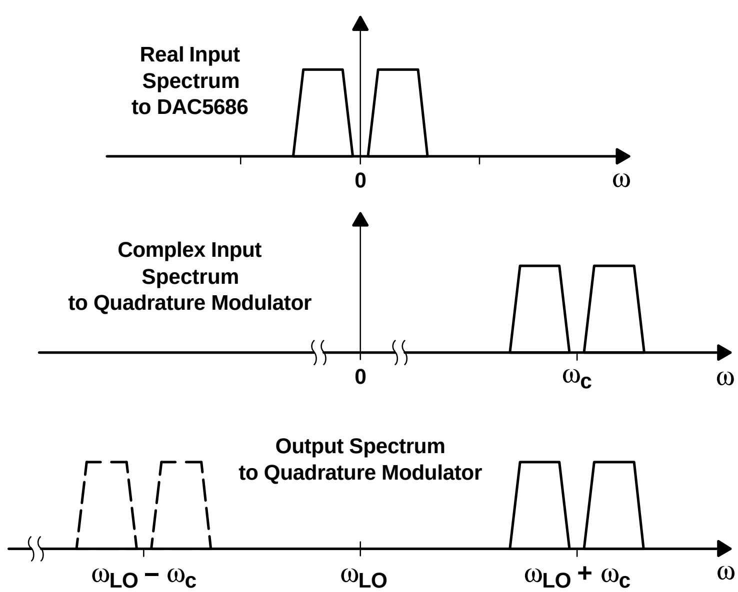


Figure 21. Spectrum After First and Second Up-Converson for Real Input

DETAILED DESCRIPTION (continued)

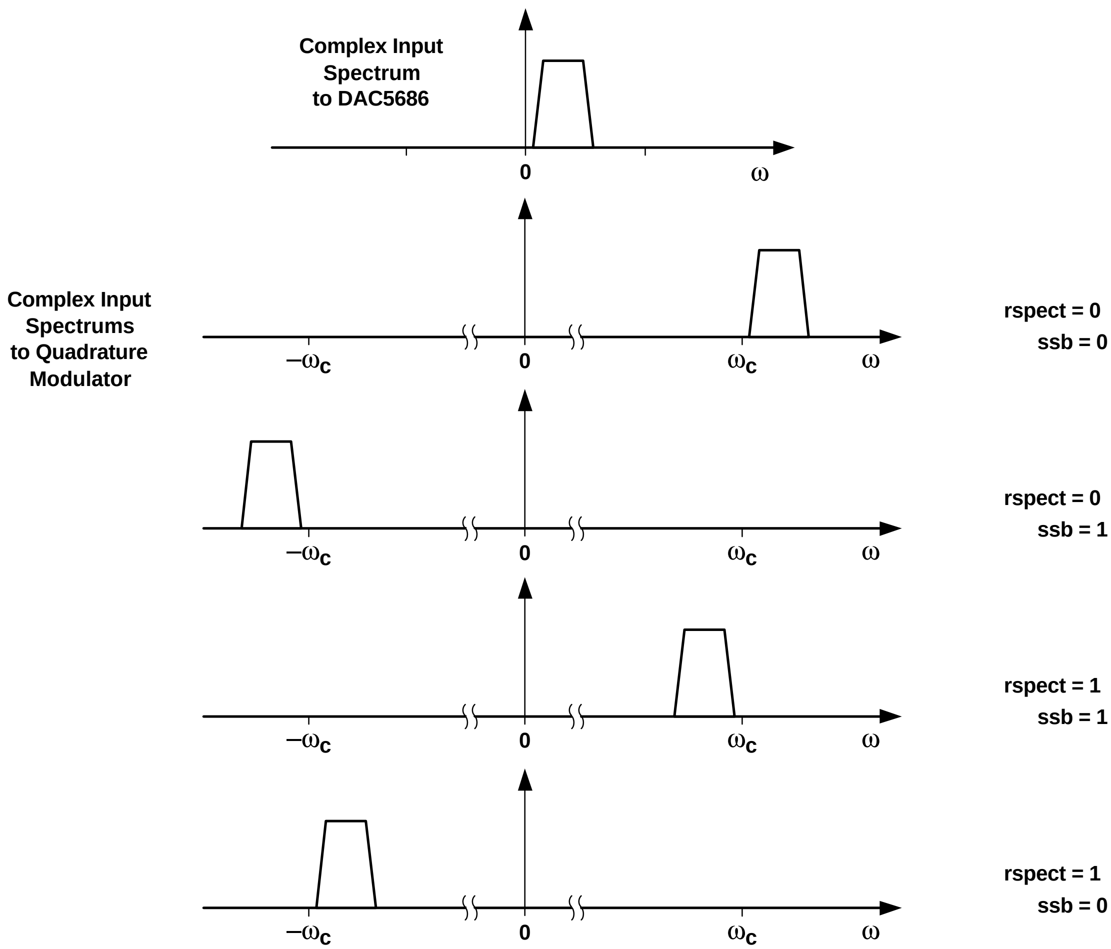


Figure 22. Spectrum After First and Second Up-Converson for Complex Input

To compensate for the sinx/x rolloff of the zero-order hold of the DACs, the DAC5686 provides an inverse sinc FIR, which provides high-frequency boost. The magnitude spectral response of this filter is presented in the *Digital Filters* section.

DAC Gain and Offset Control

Unmatched gains and offsets at the RF quadrature modulator result in unwanted sideband and local-oscillator feedthrough. Gain and offset imbalances between the two DACs are compensated for by programming **daca_gain**, **dacb_gain**, **daca_offset**, and **dacb_offset** in registers 0x0A through 0x0F (see the following register descriptions). The DAC gain value controls the full-scale output current. The DAC offset value adds a digital offset to the digital data before digital-to-analog conversion. Care must be taken when using the offset by restricting the dynamic range of the digital signal to prevent saturation when the offset value is added to the digital signal.

Quadrature Modulation Mode

In quadrature modulation mode, on-chip mixing of complex I and Q inputs provides the final baseband-to-IF up-conversion. Quadrature modulation mode is selected by **mode[1:0]** = 10 in the config_lsb register. Figure 23 shows the data path architecture in quadrature modulation mode. Complex baseband I and Q from the ASIC/FPGA are input to the DAC5686, which in turn quadrature modulates I and Q to produce the final IF single-sideband spectrum. DAC A is held constant, while DAC B presents the DAC5686 quadrature modulator mode output.

DETAILED DESCRIPTION (continued)

NCO mixing frequencies are programmed through 32-bit **freq** (4 registers); 16-bit phase adjustments are programmed through **phase** (2 registers). The NCO operates at the DAC update rate; thus, increased amounts of interpolation allow for higher IFs. More details for the NCO are provided in the NCO section. For mixing to $F_{dac}/4$, the DAC5686 provides a specific architecture that exploits the {… –1 0 1 0 …} resultant streams from sin and cos; the NCO is shut off in this mode to conserve power. $F_{dac}/4$ mix mode is implemented by deasserting **nco** in register config_msb while in single-sideband or quadrature modulation mode.

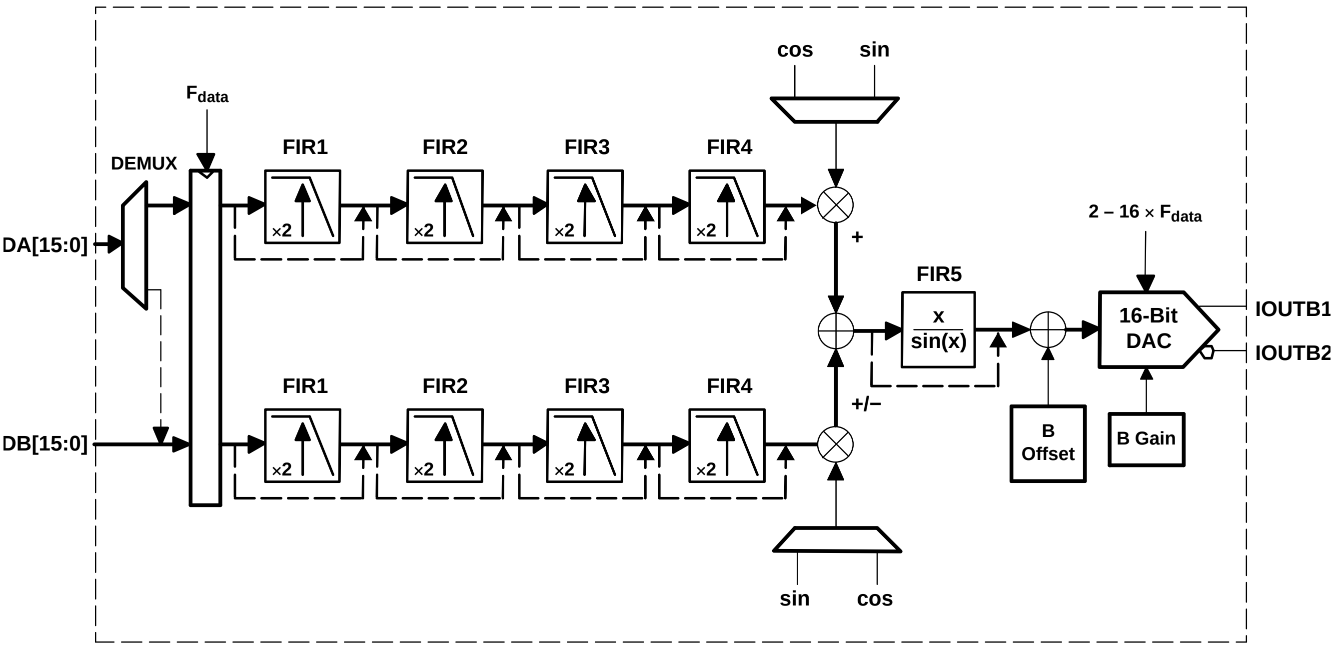


Figure 23. Data Path in Quadrature Modulation Mode

In quadrature modulation mode, only one output from the complex mixer stage is routed to the B DAC. The output can be expressed as:

$$B(t) = I(t)\sin(\omega_c t) + Q(t)\cos(\omega_c t)$$

or

$$B(t) = I(t)\cos(\omega_c t) - Q(t)\sin(\omega_c t)$$

Single-sideband up-conversion is achieved when I and Q are Hilbert transform pairs. Upper- or lower-sideband up-conversion is selected by **ssb** in the **config_msb** register, which selects the output from the mixer stage that is routed out.

The offset and gain features for the B DAC, as previously described, are functional in the quadrature mode.

Serial Interface

The serial port of the DAC5686 is a flexible serial interface that communicates with industry-standard microprocessors and microcontrollers. The interface provides read/write access to all registers used to define the operating modes of the DAC5686. It is compatible with most synchronous transfer formats and can be configured as a 3- or 4-pin interface by **sif4** in register **config_msb**. In both configurations, **SCLK** is the serial-interface input clock and **SDENB** is the serial-interface enable. For the 3-pin configuration, **SDIO** is a bidirectional pin for both data-in and data-out. For the 4-pin configuration, **SDIO** is data-in only and **SDO** is data-out only.

DETAILED DESCRIPTION (continued)

Each read/write operation is framed by signal **SDENB** (serial data enable bar) asserted low for 2 to 5 bytes, depending on the data length to be transferred (1–4 bytes). The first frame byte is the instruction cycle, which identifies the following data transfer cycle as read or write, how many bytes to transfer, and the address to/from which to transfer the data. Table 1 indicates the function of each bit in the instruction cycle and is followed by a detailed description of each bit. Frame bytes 2 through 5 comprise the data to be transferred.

Table 1. Instruction Byte of the Serial Interface

	MSB							LSB
Bit	7	6	5	4	3	2	1	0
Description	R/$\overline{W}$	N1	N0	–	A3	A2	A1	A0

R/$\overline{W}$: Identifies the following data transfer cycle as a read or write operation. A high indicates a read operation from the DAC5686 and a low indicates a write operation to the DAC5686.

N[1:0]: Identifies the number of data bytes to be transferred per Table 2. Data is transferred MSB-first.

Table 2. Number of Transferred Bytes Within One Communication Frame

N1	N0	DESCRIPTION
0	0	Transfer 1 byte
0	1	Transfer 2 bytes
1	0	Transfer 3 bytes
1	1	Transfer 4 bytes

A4: Unused

A[3:0]: Identifies the address of the register to be accessed during the read or write operation. For multibyte transfers, this address is the starting address and the address decrements. Note that the address is written to the DAC5686 MSB-first.

Serial-Port Timing Diagrams

Figure 24 shows the serial-interface timing diagram for a DAC5686 write operation. **SCLK** is the serial-interface clock input to the DAC5686. Serial data enable **SDENB** is an active-low input to the DAC5686. **SDIO** is serial data-in. Input data to the DAC5686 is clocked on the rising edges of **SCLK**.

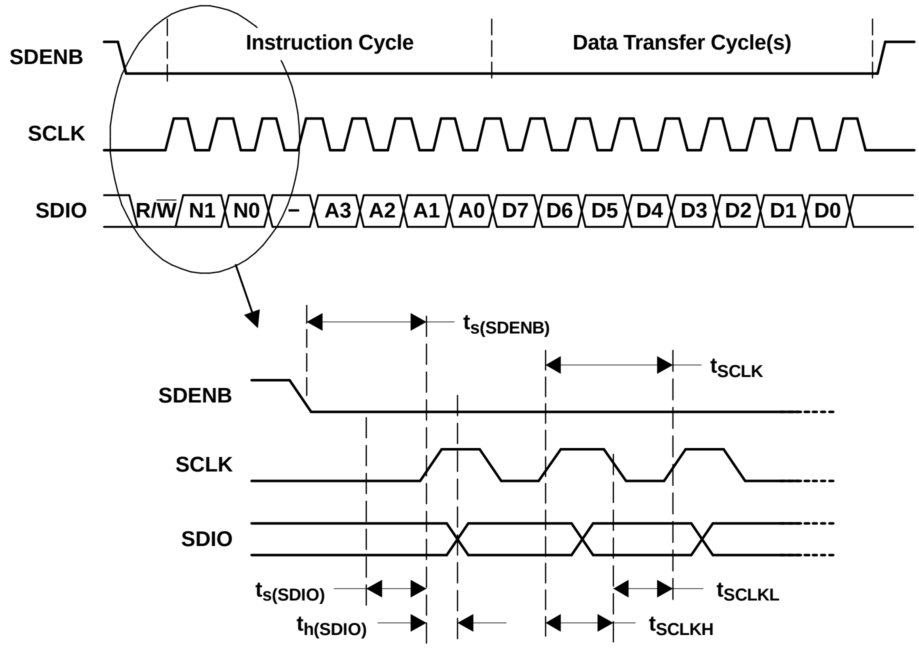


Figure 24. Serial-Interface Write Timing Diagram

Figure 25 shows the serial-interface timing diagram for a DAC5686 read operation. **SCLK** is the serial-interface clock input to the DAC5686. Serial data enable **SDENB** is an active-low input to the DAC5686. **SDIO** is serial data-in during the instruction cycle. In the 3-pin configuration, **SDIO** is data-out from the DAC5686 during the data transfer cycle(s), while **SDO** is in a high-impedance state. In the 4-pin configuration, **SDO** is data-out from the DAC5686 during the data transfer cycle(s). SDO is never placed in the high-impedance state in the four-pin configuration.

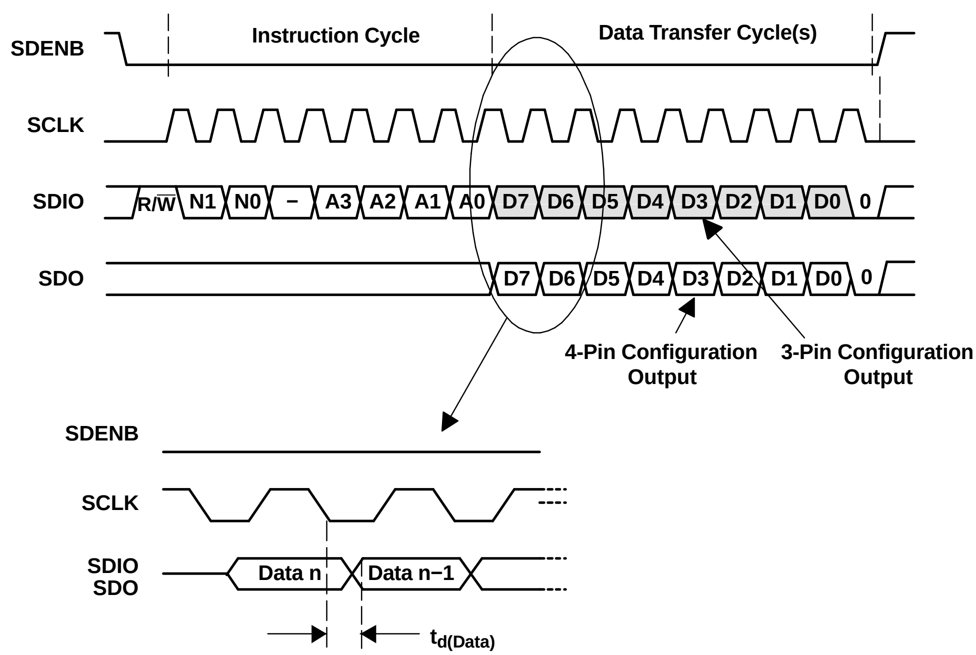


Figure 25. Serial-Interface Read Timing Diagram

Clock Generation

In the DAC5686, the internal clocks (1×, 2×, 4×, 8×, and 16×, as needed) for the logic, FIR interpolation filters, and DAC are derived from a clock at either the input data rate using an internal PLL (PLL clock mode) or the DAC output sample rate (external clock mode). Power for the internal PLL blocks (PLLVDD and PLLGND) is separate from power for the other clock generation blocks (CLKVDD and CLKGND), thus minimizing phase noise within the PLL.

The DAC5686 has three clock modes for generating the internal clocks (1×, 2×, 4×, 8×, and 16×, as needed) for the logic, FIR interpolation filters, and DACs. The clock mode is set using the PLLVDD pin and **dual_clk** in register **config_usb**. A block diagram for the clock generation circuit is shown in Figure 27.

1. PLLVDD = 0V and **dual_clk** = 0: EXTERNAL CLOCK MODE

   In EXTERNAL CLOCK MODE, the user provides a clock signal at the DAC output sample rate through CLK2/CLK2C. CLK1/CLK1C and the internal PLL are not used, so the LPF circuit is not applicable. The input data rate clock and interpolation rate are selected by the registers **sel[1:0]**, and are output through the PLLLOCK pin. It is common to use the PLLLOCK clock to drive the chip that sends the data to the DAC; otherwise, there is phase ambiguity regarding how the DAC divides down to the input sample rate clock and an external clock divider divides down. (For a divide by N, there are N possible phases.) The phase ambiguity can also be solved by using PHSTR pin with a synchronization signal.

2. PLLVDD = 3.3V (**dual_clk** can be 0 or 1 and is ignored): PLL CLOCK MODE

   Power for the internal PLL blocks (PLLVDD and PLLGND) is separate from power for the other clock generation blocks (CLKVDD and CLKGND), thus minimizing PLL phase noise.

   In PLL CLOCK MODE, the DAC is driven at the input sample rate (unless the data is multiplexed) through CLK1/CLK1C. CLK2/CLK2C is not used. In this case, there is no phase ambiguity on the clock. The DAC generates the higher speed DAC sample rate clock using an internal PLL/VCO. In PLL clock mode, the user provides a differential external reference clock on CLK1/CLK1C.

   A type-4 phase-frequency detector (PFD) in the internal PLL compares this reference clock to a feedback clock and drives the PLL to maintain synchronization between the two clocks. The feedback clock is generated by dividing the VCO output by 1×, 2×, 4×, or 8× as selected by the prescaler (**div[1:0]**). The output of the prescaler is the DAC sample rate clock and is divided down to generate clocks at ÷2, ÷4, ÷8, and ÷16. The feedback clock is selected by the registers **sel[1:0]**, an then is fed back to the PFD for synchronization to the input clock. The feedback clock is also used for the data input rate, so the ratio of DAC output clock to feedback clock sets the interpolation rate of the DAC5686. The PLLLOCK pin is an output that indicates when the PLL has achieved lock. An external RC low-pass PLL filter is provided by the user at pin LPF. See the low-pass filter section for filter setting calculations. This is the only mode where the LPF filter applies.

3. PLLVDD = 0V and **dual_clk** = 1: DUAL CLOCK MODE

   In DUAL CLOCK MODE, the DAC is driven at the DAC sample rate through CLK2/CLK2C and at the input data rate through CLK1/CLK1C. The DUAL CLOCK MODE has the advantage of a clean external clock for the DAC sampling without the phase ambiguity. The edges of CLK1 and CLK2 must be aligned to within $\pm t_{\_align}$ (See Figure 26), defined as

   $$t_{\_align} = \frac{1}{2F_{CLK2}} - 0.5\ \text{ns}$$

   where F_{CLK2} is the clock frequency of CLK2. For example, $t_{\_align}$ = 0.5 ns at F_{CLK2} = 500 MHz and 1.5 ns at F_{CLK2} = 250 MHz.

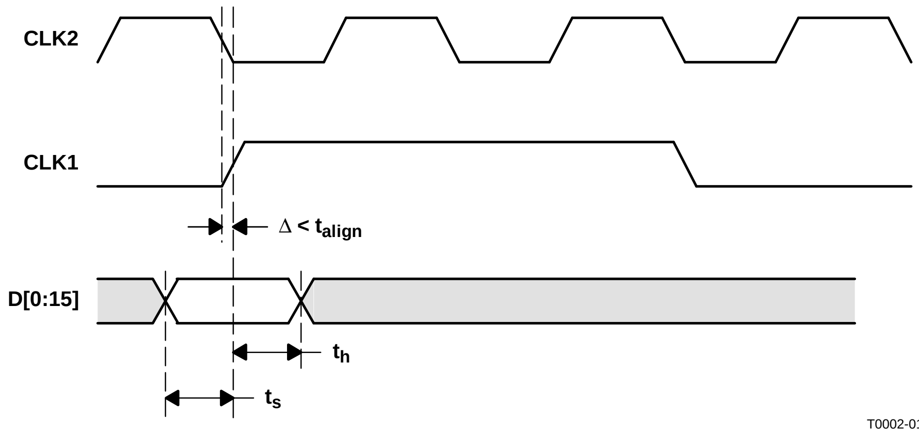


Figure 26. DAC and Data Clock Mode

The CDC7005 from Texas Instruments is recommended for providing phase-aligned clocks at different frequencies for this application.

Table 3 provides a summary of the clock configurations with corresponding data rate ranges.

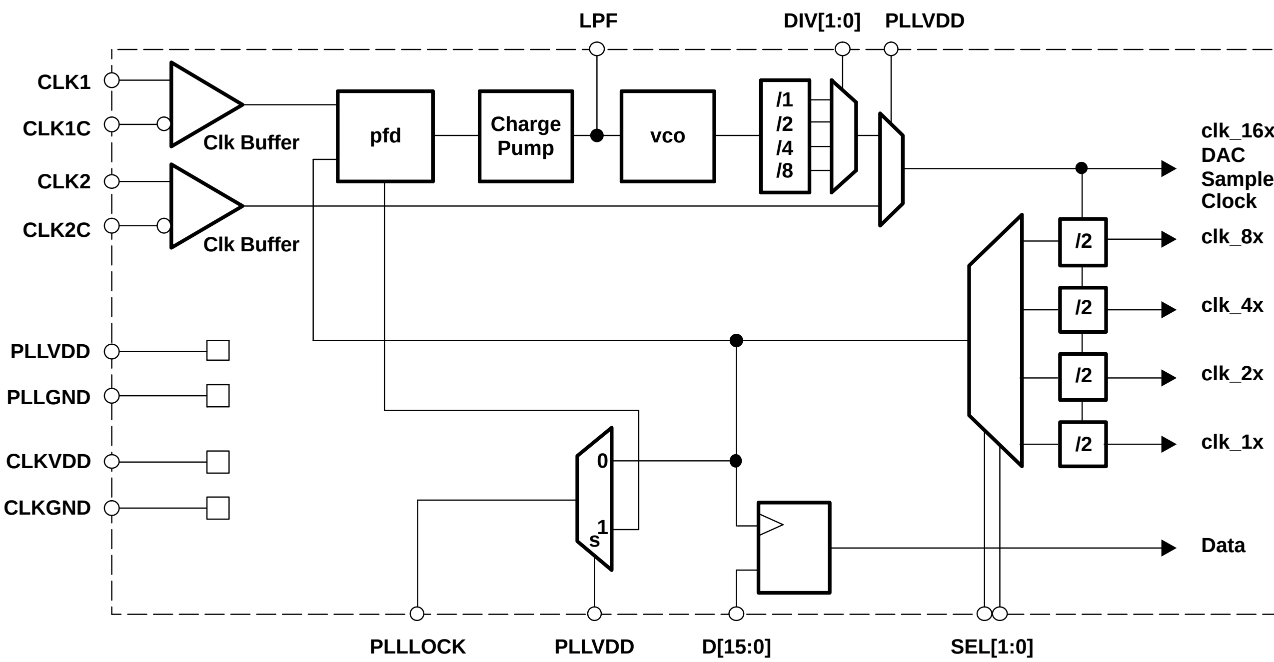


Figure 27. Clock-Generation Architecture

Table 3. Clock-Mode Configuration

CLOCK MODE	PLLVDD	DIV[1:0]	SEL[1:0]	DATA RATE (MSPS)	PLLLOCK PIN FUNCTION
Non-interleaved input data; internal PLL off; DA[15:0] data rate matches DB[15:0] data rate.					
External 2×	0 V	XX	00	DC to 160	External clk2/clk2c clock ÷ 2
External 4×	0 V	XX	01	DC to 125	External clk2/clk2c clock ÷ 4
External 8×	0 V	XX	10	DC to 62.5	External clk2/clk2c clock ÷ 8
External 16×	0 V	XX	11	DC to 31.25	External clk2/clk2c clock ÷ 16
External dual clock 2×	0 V	XX	00	DC to 160	None - held low
External dual clock 4×	0 V	XX	01	DC to 125	None - held low

Table 3. Clock-Mode Configuration (continued)

CLOCK MODE	PLLVDD	DIV[1:0]	SEL[1:0]	DATA RATE (MSPS)	PLLLOCK PIN FUNCTION
External dual clock 8×	0 V	XX	10	DC to 62.5	None - held low
External dual clock 16×	0 V	XX	11	DC to 31.25	None - held low
Interleaved input data on the DA[15:0] input pins; internal PLL off					
External 2×	0 V	XX	00	DC to 80	External clk2/clk2c clock ÷ 2
External 4×	0 V	XX	01	DC to 80	External clk2/clk2c clock ÷ 4
External 8×	0 V	XX	10	DC to 62.5	External clk2/clk2c clock ÷ 8
External 16×	0 V	XX	11	DC to 31.25	External clk2/clk2c clock ÷ 16
External dual clock 2×	0 V	XX	00	DC to 80	None - held low
External dual clock 4×	0 V	XX	01	DC to 62.5	None - held low
External dual clock 8×	0 V	XX	10	DC to 31.25	None - held low
External dual clock 16×	0 V	XX	11	DC to 15.625	None - held low
Non-interleaved input data; internal PLL on; DA[15:0] data rate matches DB[15:0] data rate.					
Internal 2×	3.3 V	00	00	125 to 160	Internal PLL lock indicator
Internal 2×	3.3 V	01	00	62.5 to 125	Internal PLL lock indicator
Internal 2×	3.3 V	10	00	31.25 to 62.5	Internal PLL lock indicator
Internal 2×	3.3 V	11	00	15.63 to 31.25	Internal PLL lock indicator
Internal 4×	3.3 V	00	01	62.5 to 125	Internal PLL lock indicator
Internal 4×	3.3 V	01	01	31.25 to 62.5	Internal PLL lock indicator
Internal 4×	3.3 V	10	01	15.63 to 31.25	Internal PLL lock indicator
Internal 4×	3.3 V	11	01	7.8125 to 15.625	Internal PLL lock indicator
Internal 8×	3.3 V	00	10	31.25 to 62.5	Internal PLL lock indicator
Internal 8×	3.3 V	01	10	15.63 to 31.25	Internal PLL lock indicator
Internal 8×	3.3 V	10	10	7.8125 to 15.625	Internal PLL lock indicator
Internal 8×	3.3 V	11	10	3.9 to 7.8125	Internal PLL lock indicator
Internal 16×	3.3 V	00	11	15.625 to 31.25	Internal PLL lock indicator
Internal 16×	3.3 V	01	11	7.8125 to 15.625	Internal PLL lock indicator
Internal 16×	3.3 V	10	11	3.9062 to 7.8125	Internal PLL lock indicator
Interleaved input data on the DA[15:0] input pins; internal PLL on					
Internal 2×	3.3 V	00	00	Not recommended	Internal PLL lock indicator
Internal 2×	3.3 V	01	00	62.5 to 80	Internal PLL lock indicator
Internal 2×	3.3 V	10	00	31.25 to 62.5	Internal PLL lock indicator
Internal 2×	3.3 V	11	00	15.625 to 31.25	Internal PLL lock indicator
Internal 4×	3.3 V	00	01	62.5 to 80	Internal PLL lock indicator
Internal 4×	3.3 V	01	01	31.25 to 62.5	Internal PLL lock indicator
Internal 4×	3.3 V	10	01	15.625 to 31.25	Internal PLL lock indicator
Internal 4×	3.3 V	11	01	7.8125 to 15.625	Internal PLL lock indicator
Internal 8×	3.3 V	00	10	31.25 to 62.5	Internal PLL lock indicator
Internal 8×	3.3 V	01	10	15.625 to 31.25	Internal PLL lock indicator
Internal 8×	3.3 V	10	10	7.8125 to 15.625	Internal PLL lock indicator
Internal 8×	3.3 V	11	10	3.9062 to 7.8125	Internal PLL lock indicator
Internal 16×	3.3 V	00	11	15.625 to 31.25	Internal PLL lock indicator
Internal 16×	3.3 V	01	11	7.8125 to 15.625	Internal PLL lock indicator
Internal 16×	3.3 V	10	11	3.9062 to 7.8125	Internal PLL lock indicator
Internal 16×	3.3 V	11	11	1.9531 to 3.9062	Internal PLL lock indicator

Dual-Bus Mode

In dual-bus mode, two separate parallel data streams (I and Q) are input to the DAC5686 on data bus **DA** and data bus **DB**. Dual-bus mode is selected by setting **INTERL** to 0 in the **config_msb** register. Figure 28 shows the DAC5686 data path in dual-bus mode. The dual-bus mode timing diagram is shown in Figure 29 for the PLL clock mode and in Figure 30 for the external clock mode.

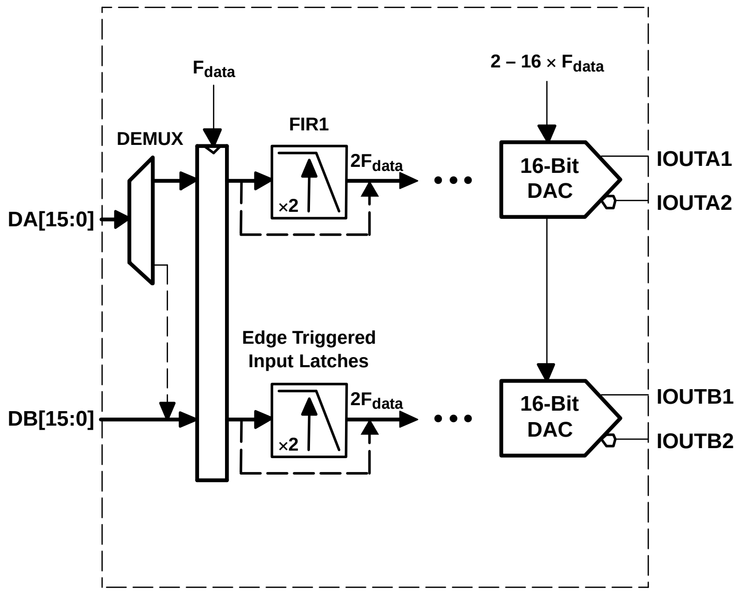


Figure 28. Dual-Bus Mode Data Path

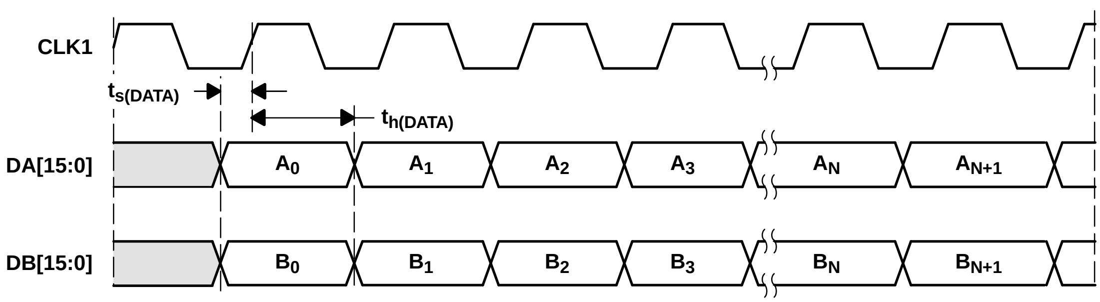


Figure 29. Dual-Bus Mode Timing Diagram (PLL Mode)

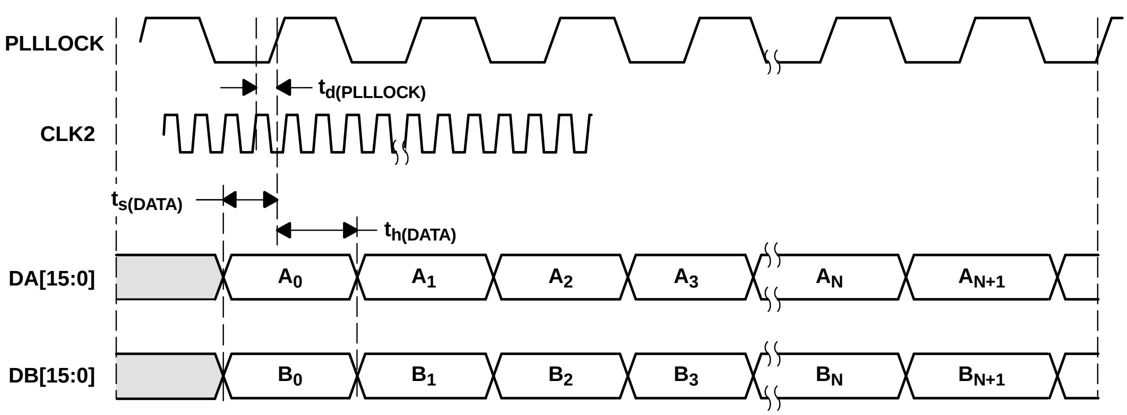


Figure 30. Dual-Bus Mode Timing Diagram (External Clock Mode)

Interleave Bus Mode

In interleave bus mode, one parallel data stream with interleaved data (I and Q) is input to the DAC5686 on data bus **DA**. Interleave bus mode is selected by setting **INTERL** to 1 in the **config_msb** register. Figure 31 shows the DAC5686 data path in interleave bus mode. The interleave bus mode timing diagram is shown in Figure 32.

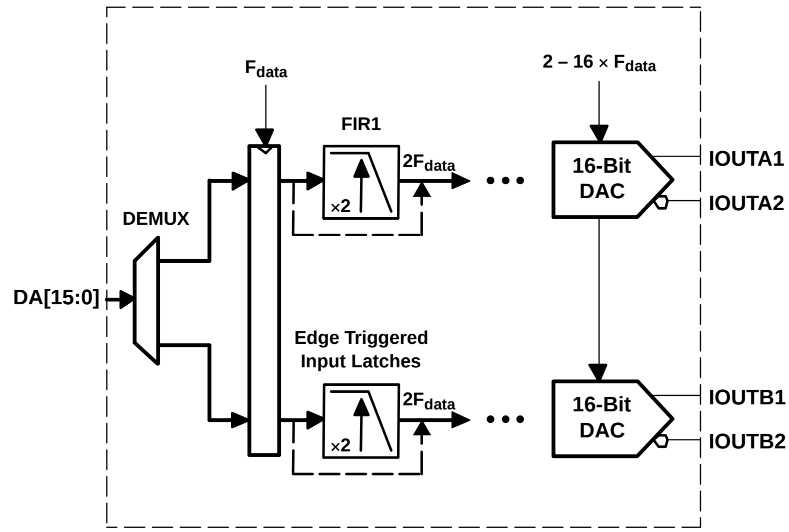


Figure 31. Interleave Bus Mode Data Path

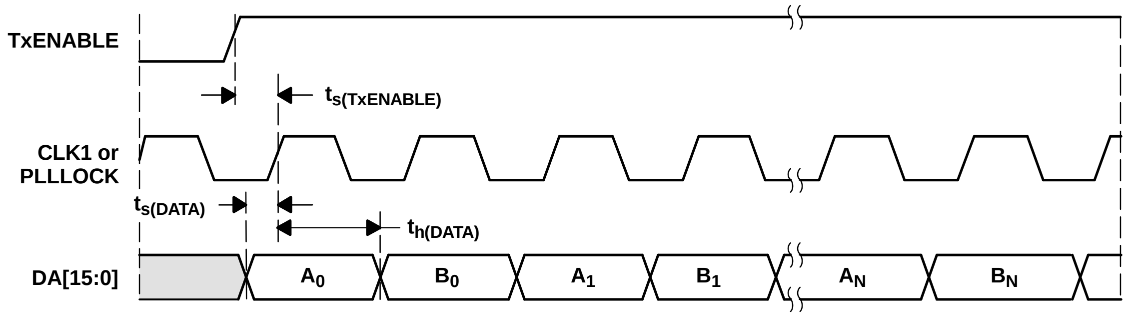


Figure 32. Interleave Bus Mode Timing Diagram Using TxENABLE

Interleaved user data on data bus **DA** is alternately multiplexed to internal data channels A and B. Data channels A and B can be synchronized using either the **QFLAG** pin or the **TxENABLE** pin. When **qflag** in register **config_usb** is 0, transitions on **TxENABLE** identify the interleaved data sequence. The first data after the rising edge of **TxENABLE** is latched with the rising edge of **CLK** as channel-A data. Data is then alternately distributed to B and A channels with successive rising edges of **CLK**. When **qflag** is 1, the **QFLAG** pin is used as an output to identify the interleaved data sequence. **QFLAG** high identifies data as channel B (see Figure 33).

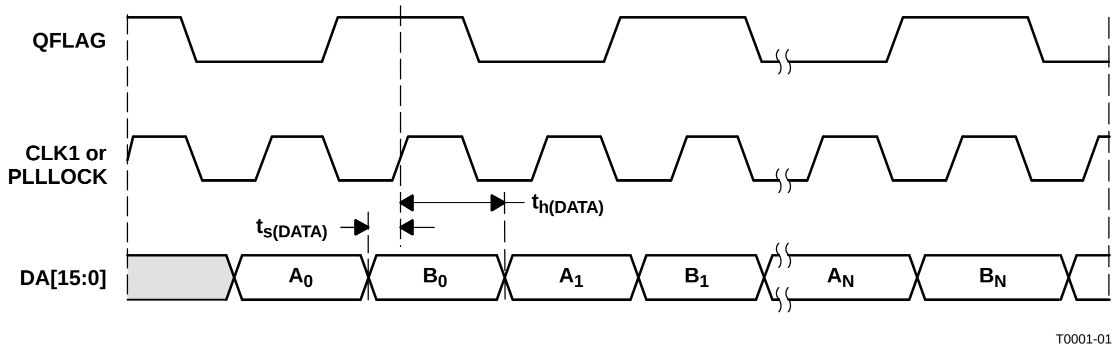


Figure 33. Interleave Bus Mode Timing Diagram Using QFLAG

The dual-clock mode is selected by setting **dualclk** high in the **config_usb** register. In this mode, the DAC5686 uses both clock inputs; **CLK1/CLK1C** is the input data clock, and **CLK2/CLK2C** is the external clock. The edges of the two input clocks must be phase-aligned within ±500 ps to function properly.

Clock Synchronization Using the PHSTR Pin in External Clock Mode

In external clock mode, the DAC5686 is clocked at the DAC output sample frequency (CLK2 and CLK2C). For an interpolation rate N, there are N possible phases for the DAC input clock on the PLLLOCK pin (see Figure 34 for N = 4).

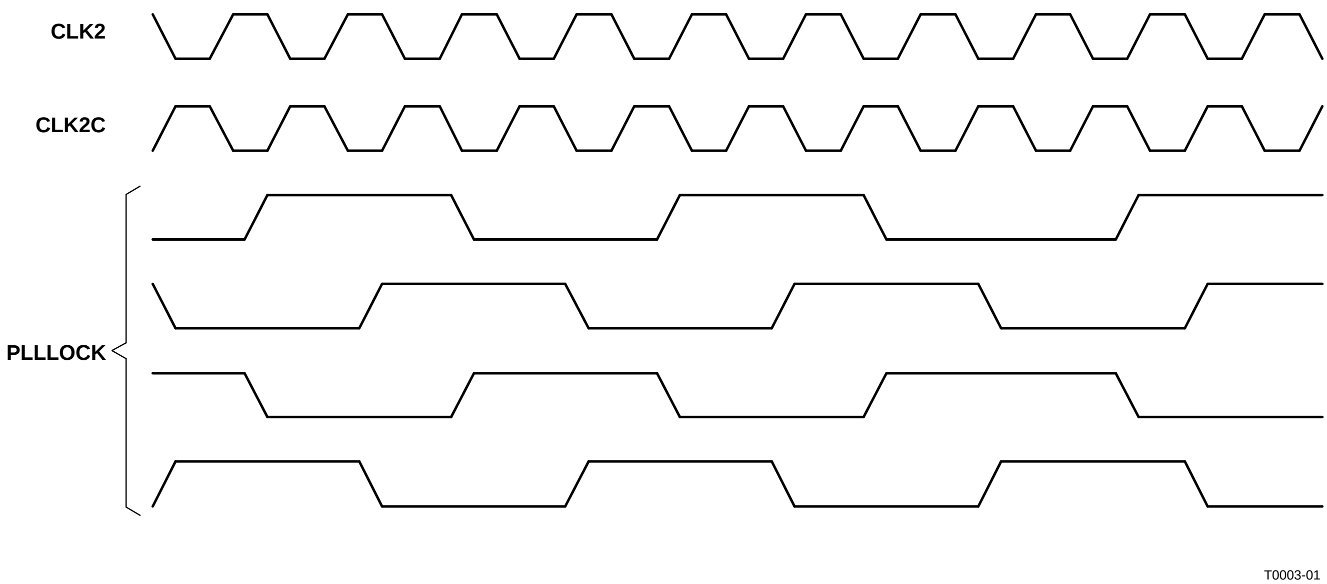


Figure 34. Four Possible PLLLOCK Phases for N = 4 in External Clock Mode

To synchronize PLLLOCK input clocks across multiple DAC5686 chips, a sync signal on the PHSTR pin is used. During configuration of the DAC5686 chips, address **sync_phstr** in **config_msb** is set high to enable the PHSTR input pin as a sync input to the clock dividers generating the input clock. A simultaneous low-to-high transition on the PHSTR pin for each DAC5686 then forces the input clock on PLLLOCK to start in phase on each DAC. See Figure 35.

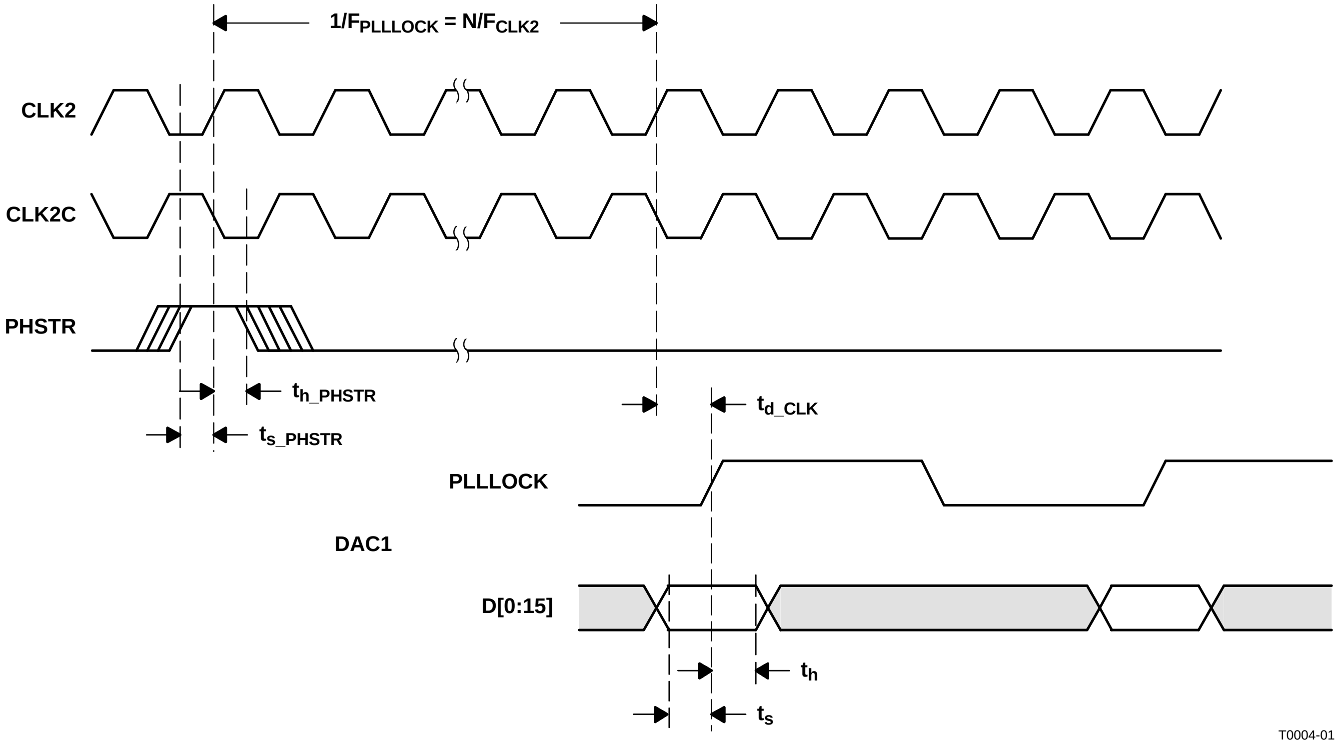


Figure 35. Using PHSTR to Synchronize PLLLOCK Input Clock for Multiple DACs in External Clock Mode

The PHSTR transition has a setup and hold time relative to the DAC output sample clock (t_{s_PHSTR} and t_{h_PHSTR}) equal to 50% of the DAC output sample clock period up to a maximum of 1 ns. At 500 MHz, the setup and hold times are therefore 0.5 ns. The PHSTR signal can remain high after synchronization, or can return low. A new low-to-high transition resynchronizes the input clock. Note that the PHSTR transition also resets the NCO accumulator.

Digital Filters

Figure 36 through Figure 39 show magnitude spectrum responses for 2×, 4×, 8×, and 16× FIR interpolation filtering. The transition band is from 0.4 to 0.6 f_{DATA} with < 0.002-dB pass-band ripple and > 80-dB stop-band attenuation for all four configurations. The filters are linear phase. The **sel** field in register **config_lsb** selects the interpolation filtering rate as 2×, 4×, 8×, or 16×; interpolation filtering can be completely bypassed by setting **fullbypass** in register **config_lsb**.

Figure 40 shows the spectral correction of the DAC sinx/x rolloff achieved with use of inverse sinc filtering. Pass-band ripple from 0 to 0.4 f_{DATA} is < 0.03 dB. Inverse sinc filtering is enabled by **sinc** in register **config_msb**.

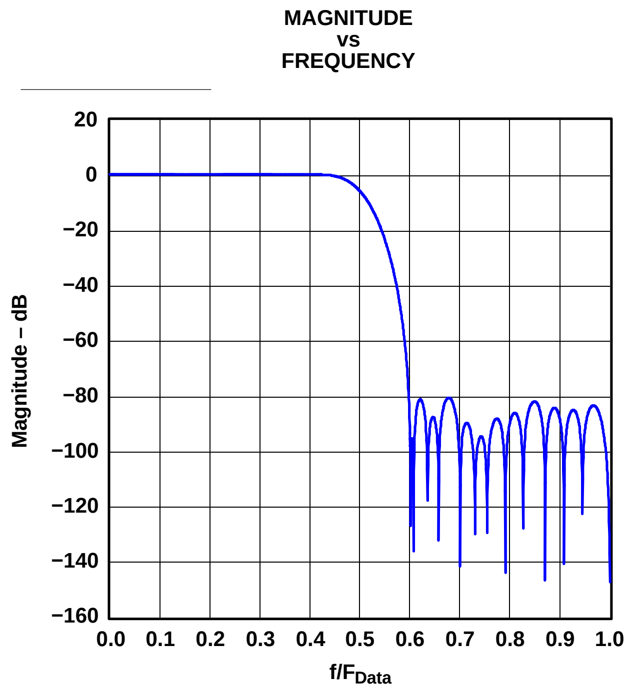


Figure 36. Magnitude Spectrum for 2× Interpolation (dB)

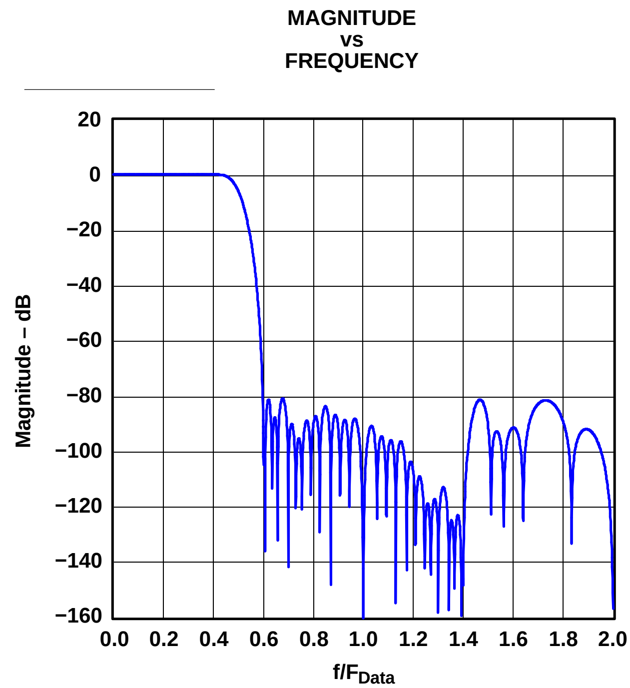


Figure 37. Magnitude Spectrum for 4× Interpolation (dB)

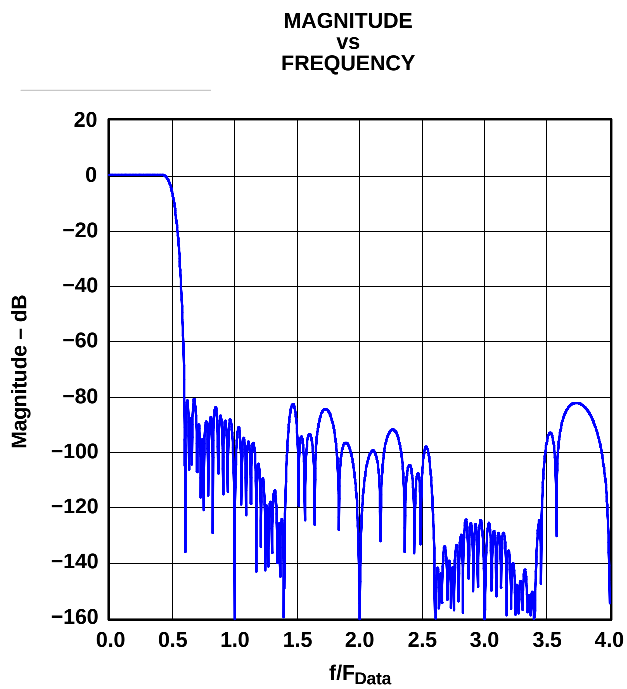


Figure 38. Magnitude Spectrum for 8× Interpolation (dB)

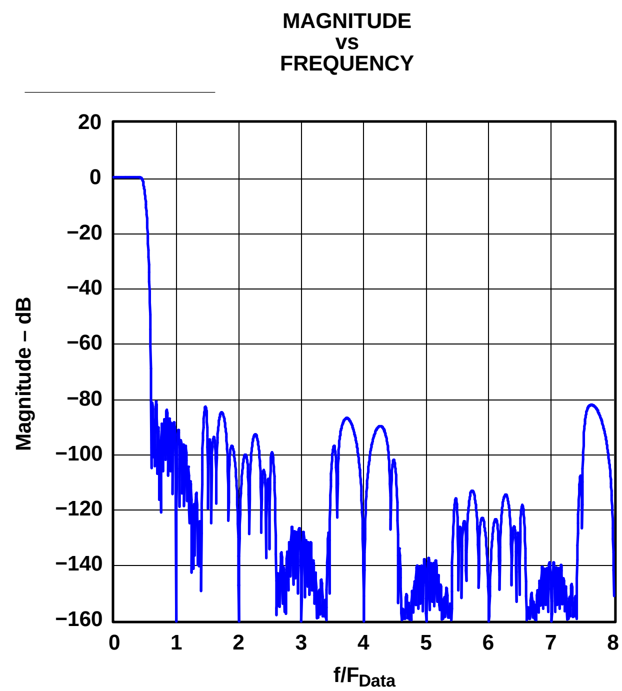


Figure 39. Magnitude Spectrum for 16× Interpolation (dB)

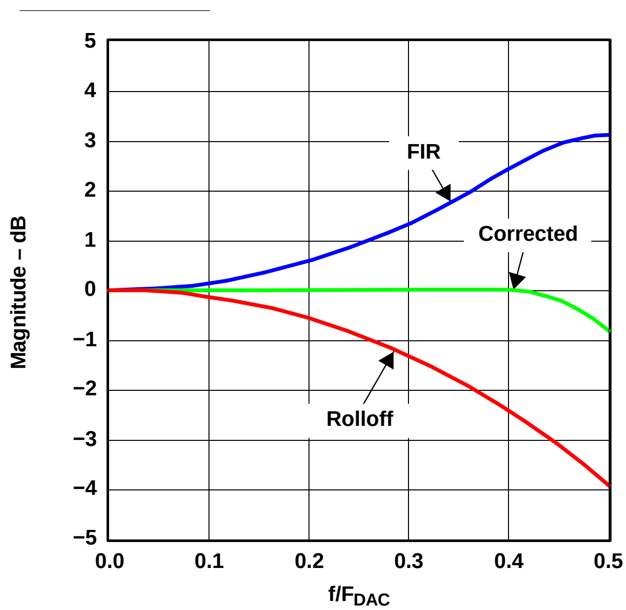


Figure 40. Magnitude Spectrum for Inverse Sinc Filtering

The filter taps for interpolation filters FIR1 - FIR4 and inverse sinc filter FIR5 are listed in Table 4.

Table 4. Filter Taps for FIR1–FIR5

FIR1	FIR2	FIR3	FIR4	FIR5 (INVSINC)
8	9	31	-33	1
0	0	0	0	–3
–24	–58	–219	289	9
0	0	0	512	–34
58	214	1212	289	400
0	0	2048	0	–34
–120	–638	1212	–33	9
0	0	0		–3
221	2521	–219		1
0	4096	0		
–380	2521	31		
0	0			
619	–638			
0	0			
-971	214			
0	0			
1490	–58			
0	0			
–2288	9			
0				
3649				
0				
–6628				
0				

Table 4. Filter Taps for FIR1–FIR5 (continued)

FIR1	FIR2	FIR3	FIR4	FIR5 (INVSINC)
20750				
32768				
20750				
0				
–6628				
0				
3649				
0				
–2288				
0				
1490				
0				
–971				
0				
619				
0				
–380				
0				
221				
0				
–120				
0				
58				
0				
–24				
0				
8				

NCO

The DAC5686 uses a numerically controlled oscillator (NCO) with a 32-bit frequency register and a 16-bit phase register. The NCO is used in quadrature-modulation and single-sideband modes to provide sin and cos for mixing. The NCO tuning frequency is programmed in registers 0x1 through 0x4. Phase offset is programmed is registers 0x5 and 0x6. A block diagram of the NCO is shown in Figure 41.

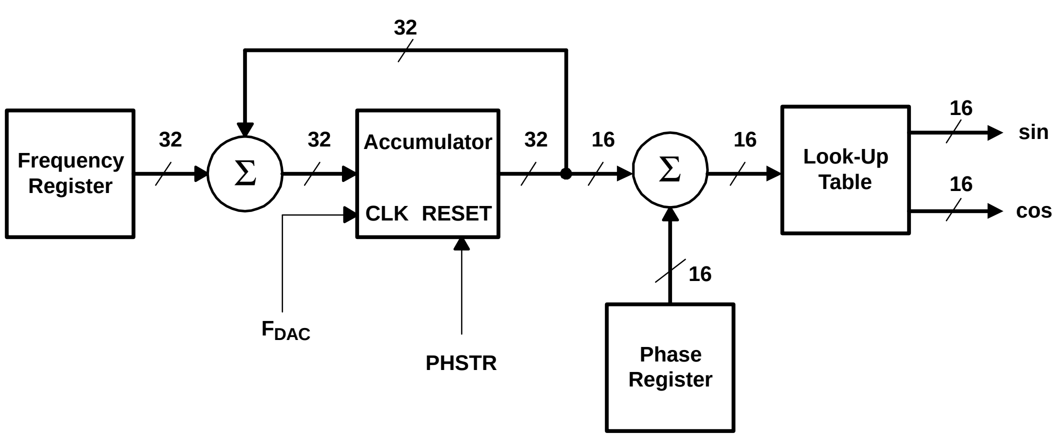


Figure 41. Block Diagram of the NCO

The NCO accumulator is reset to zero when the **PHSTR** pin is high and remains at zero until **PHSTR** is set low. Frequency word **freq** in the frequency register is added to the accumulator every clock cycle. The output frequency of the NCO is:

$$f_{NCO} = \frac{freq \times F_{DAC}}{2^{32}}$$

While the maximum clock frequency of the DACs is 500 MSPS, the maximum clock frequency the NCO can operate at is 320 MHz; mixing at DAC rates higher than 320 MSPS requires using the fs/4 mixing option.

Register Bit Allocation Map

NAME	R/W	AD-DRESS	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
chip_ver	R/W	0x00	atest[4:0]					version[2:0] *read only*		
freq_lsb	R/W	0x01	freq_int[7:0]							
freq_lmidsb	R/W	0x02	freq_int[15:8]							
freq_umidsb	R/W	0x03	freq_int[23:16]							
freq_msb	R/W	0x04	freq_int[31:24]							
phase_lsb	R/W	0x05	phase_int[7:0]							
phase_msb	R/W	0x06	phase_int[15:8]							
config_lsb	R/W	0x07	mode[1:0]		div[1:0]		sel[1:0]		counter	fbypass
config_msb	R/W	0x08	ssb	interl	sinc	dith	sync_phstr	nco	sif4	twos
config_usb	R/W	0x09	dual clk	dds_gain[1:0]		rspect	qflag	pll_rng[1:0]		rev_bbus
daca_offset_lsb	R/W	0x0A	daca_offset[7:0]							
daca_gain_lsb	R/W	0x0B	daca_gain[7:0]							
daca_offset_gain_msb	R/W	0x0C	daca_offset[10:8]			sleepA	daca_gain[11:8]			
dacb_offset_lsb	R/W	0x0D	dacb_offset[7:0]							
dacb_gain_lsb	R/W	0x0E	dacb_gain[7:0]							
dacb_offset_gain_msb	R/W	0x0F	dacb_offset[10:8]			sleepB	dacb_gain[11:8]			

REGISTER DESCRIPTIONS

Register Name: chip_ver

MSB LSB

atest[4:0]					chip_ver[2:0] *read only*		
0	0	0	0	0	1	0	1

chip_ver[3:0]: chip_ver [3:0] stores the device version, initially 0x5. The user can find out which version of the DAC5686 is in the system by reading this byte.

a_test[4:0]: must be 0 for proper operation.

Register Name: freq_lsb

MSB LSB

freq_int[7:0]							
0	0	0	0	0	0	0	0

freq_int[7:0]: The lower 8 bits of the frequency register in the DDS block

Register Name: freq_lmidsb

MSB LSB

freq_int[15:8]							
0	0	0	0	0	0	0	0

freq_int[15:8]: The lower mid 8 bits of the frequency register in the DDS block

Register Name: freq_umidsb

MSB LSB

freq_int[23:16]							
0	0	0	0	0	0	0	0

freq_int[23:16]: The upper mid 8 bits of the frequency register in the DDS block

Register Name: freq_msb

MSB LSB

freq_int[31:24]							
0	0	1	0	0	0	0	0

freq_int[31:24]: The most significant 8 bits of the frequency register in the DDS block

Register Name: phase_lsb

MSB LSB

phase_int[7:0]							
0	0	0	0	0	0	0	0

phase_int[7:0]: The lower 8 bits of the phase register in the DDS block

Register Name: phase_msb

MSB LSB

phase_int[15:8]							
0	0	0	0	0	0	0	0

phase_int[15:8]: The most significant 8 bits of the phase register in the DDS block

Register Name: config_lsb

MSB LSB

mode[1:0]		div[1:0]		sel[1:0]		counter	Full_bypass
0	0	0	0	0	0	0	1

mode[1:0]: Controls the mode of the DAC5686; summarized in Table 5.

Table 5. DAC5686 Modes

mode[1:0]	DAC5686 MODE
00	Dual-DAC
01	Single-sideband
10	Quadrature
11	Dual-DAC

div[1:0]: Controls the PLL divider value; summarized in Table 6.

Table 6. PLL Divide Ratios

div[1:0]	PLL DIVIDE RATIO
00	1× divider
01	2× divider
10	4× divider
11	8× divider

sel[1:0]: Controls the selection of interpolating filters used; summarized in Table 7.

Table 7. DAC5686 Filter Configuration

sel[1:0]	INTERP. FIR SETTING
00	×2
01	× 4
10	× 8
11	× 16

counter: When asserted, the DAC5686 goes into counter mode and uses an internal counter as a ramp input to the DAC. The count range is determined by the A-side input data DA[2:0], as summarized in Table 8.

Table 8. DAC5686 Counter Mode Count Range

DA[2:0]	COUNT RANGE
000	All bits D[15:0]
001	Lower 7 bits D[6:0]
010	Mid 4 bits D[10:7]
100	Upper 5 bits D[15:11]

Full_bypass: When asserted, the interpolation filters and mixer logic are bypassed and the data inputs DA[15:0] and DB[15:0] go straight to the DAC inputs.

Register Name: config_msb

MSB							LSB
ssb	interl	sinc	dith	sync_phstr	nco	sif4	twos
0	0	0	0	0	0	0	0

ssb: In single-sideband mode, assertion inverts the B data; in quadrature modulation mode, assertion routes the A data path to DACB instead of the B data path.

interl: When asserted, data input to the DAC5686 on channel DA[15:0] is interpreted as a single interleaved stream (I/Q); channel DB[15:0] is unused.

sinc: Assertion enables the INVSINC filter.

dith: Assertion enables dithering in the PLL.

sync_phstr: Assertion enables the PHSTR input as a sync input to the clock dividers in external single-clock mode.

nco: Assertion enables the NCO.

sif4: When asserted, the sif interface becomes a 4-pin interface instead of a 3-pin interface. The SDIO pin becomes an input only and the SDO is the output.

twos: When asserted, the chip interprets the input data as 2s complement form instead of binary offset.

Register Name: config_usb

MSB							LSB
dualclk	DDS_gain[1:0]		rspect	qflag	pll_rng[1:0]		rev_bbus
0	0	0	0	0	0	0	0

dualclk: When asserted, the DAC5686 uses both clock inputs; CLK1/CLK1C is the input data clock and CLK2/CLK2C is the DAC output clock. These two clocks must be phase-aligned within ±500 ps to function properly. When deasserted, CLK2/CLK2C is the DAC output clock and is divided down to generate the input data clock, which is output on PLLLOCK. Dual clock mode is only available when PLLVDD = 0.

DDS_gain[1:0]: Controls the gain of the DDS so that the overall gain of the DDS is unity. It is important to ensure that $\max(\text{abs}(\cos(\omega t) + \sin(\omega t))) < 1$. At different frequencies, the summation produces different maximum outputs and must be reduced. The simplest is fs/4 mode where the maximum is 1 and the gain multiply should be 1 to maintain unity. However, due to the fact that the digital logic does a divide-by-two in this summation, the gain necessary to achieve unity must be double (DDS_gain[1:0] = 01). Table 9 shows the digital gain necessary and the actual signal gain needed to make the above equation have a maximum value of 1.

Table 9. Digital Gain for DDS

DDS_gain [1:0]	DIGITAL GAIN	SIGNAL GAIN FOR UNITY
00	1.40625	0.703125
01	2	1
10	1.59375	0.7936
11	1.40625	0.703125

rspect: When asserted, the sin term is negated before being used in mixing. This gives the reverse spectrum in single-sideband mode.

qflag: When asserted, the QFLAG pin is used during interleaved data input mode to identify the Q sample. When deasserted, the TXENABLE pin transition is used to start an internal toggling signal, which is used to interpret the interleaved data sequence; the first sample clocked into the DAC5686 after TXENABLE goes high is routed through the A data path.

PLL_rng[1:0]: Increases the PLL VCO VtoI current, summarized in Table 10. See Figure 17 for the effect on VCO gain and range.

Table 10. PLL VCO VtoI Current Increase

PLL_rng[1:0]	VtoI CURRENT INCREASE
00	nominal
01	15%
10	30%
11	45%

rev_bbus[1:0]: When asserted, pin 92 changes from DB15 to DB0, pin 91 changes from DB14 to DB1, etc., reversing the order of the DB[15:0] pins.

Register Name: daca_offset_lsb (2s complement)

MSB							LSB
daca_offset[7:0]							
0	0	0	0	0	0	0	0

daca_offset[7:0]: The lower 8 bits of the DACA offset

Register Name: daca_gain_lsb (2s complement)

MSB							LSB
daca_gain[7:0]							
0	0	0	0	0	0	0	0

daca_gain[7:0]: The lower 8 bits of the DACA gain control register. These lower 8 bits are for fine gain control. This word is a 2s complement value that adjusts the full-scale output current over an approximate 4% to –4% range.

Register Name: daca_offset_gain_msb (2s complement)

MSB							LSB
daca_offset[10:8]			sleepa	daca_gain[11:8]			
0	0	0	0	0	0	0	0

daca_offset[10:8]: The upper 3 bits of the DACA _offset

sleepa: When asserted, DACA is put into the sleep mode.

daca_gain[11:8]: Coarse gain control for DACA; the full-scale output current is:

$$I_{fullscale} = \left[\frac{16\left(V_{extio}\right)}{R_{biasj}} \times \frac{(GAINCODE + 1)}{16} \div \left(1 - \frac{FINEGAIN}{3072}\right) \right]$$

where GAINCODE is the decimal equivalent of daca_gain [11:8] {0…15} and the FINEGAIN is daca_gain [1:0] as 2s complement [–127…128].

Register Name: dacb_offset_lsb (2s complement)

MSB							LSB
dacb_offset[7:0]							
0	0	0	0	0	0	0	0

dacb_offset[7:0]: The lower 8 bits of the DACB offset

Register Name: dacb_gain_lsb (2s complement)

MSB							LSB
dacb_gain[7:0]							
0	0	0	0	0	0	0	0

dacb_gain[7:0]: The lower 8 bits of the DACB gain control register. These lower 8 bits are for fine gain control. This word is a 2s complement value that adjusts the full-scale output current over an approximate 4% to –4% range.

Register Name: dacb_offset_gain_msb (2s complement)

MSB							LSB
dacb_offset[10:8]			sleepb	dacb_gain[11:8]			
0	0	0	0	0	0	0	0

dacb_offset[10:8]: The upper 3 bits of the DACA _offset

sleepb: When asserted, DACB is put into the sleep mode.

dacb_gain[11:8]: Coarse gain control for DACB; the full-scale output current is:

$$I_{fullscale} = \left[\frac{16(V_{extio})}{R_{biasj}} \times \frac{(GAINCODE + 1)}{16} \div \left(1 - \frac{FINEGAIN}{3072} \right) \right]$$

where GAINCODE is the decimal equivalent of dacb_gain [11:8] {0…15} and the FINEGAIN is dacb_gain [1:0] as 2s complement [–127…128].

DIGITAL INPUTS

Figure 42 shows a schematic of the equivalent CMOS digital inputs of the DAC5686. DA[0:15], DB[0:15], SLEEP, PHSTR, TxENABLE, QFLAG, SDIO, SCLK, and SDENB have pulldown resistors and RESETB has a pullup resistor internal to the DAC5686. See the specification table for logic thresholds.

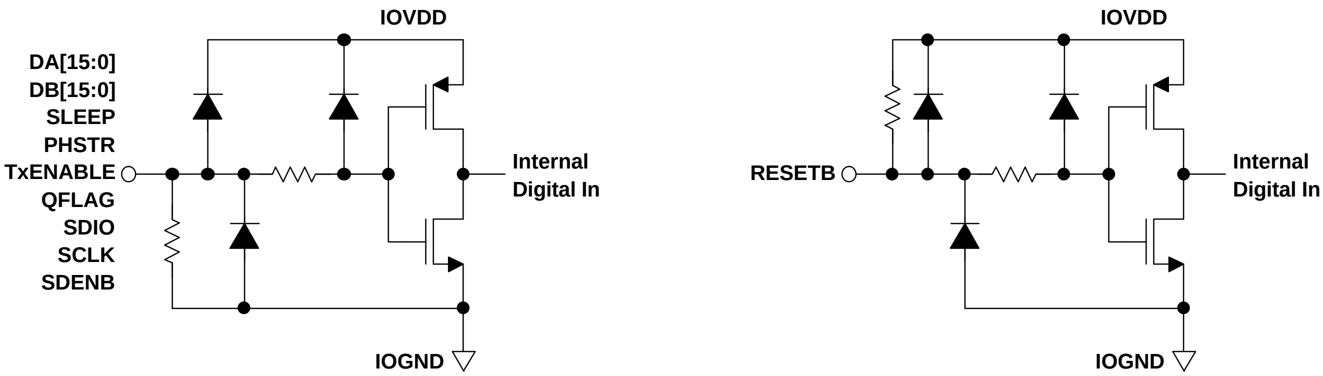


Figure 42. CMOS/TTL Digital Equivalent Input

CLOCK INPUT AND TIMING

Figure 43 shows an equivalent circuit for the clock input.

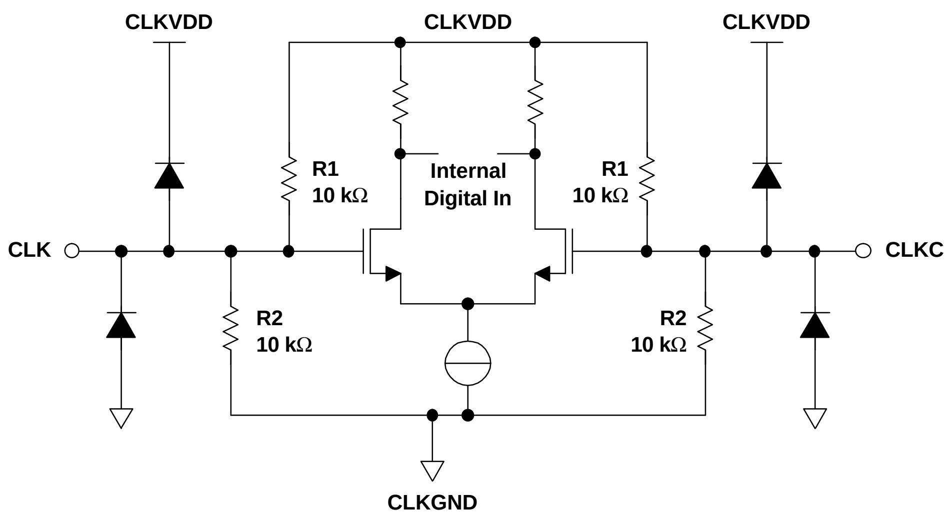


Figure 43. Clock Input Equivalent Circuit

CLOCK INPUT AND TIMING (continued)

Figure 44, Figure 45, and Figure 46 show various input configurations for driving the differential clock input (CLK/CLKC).

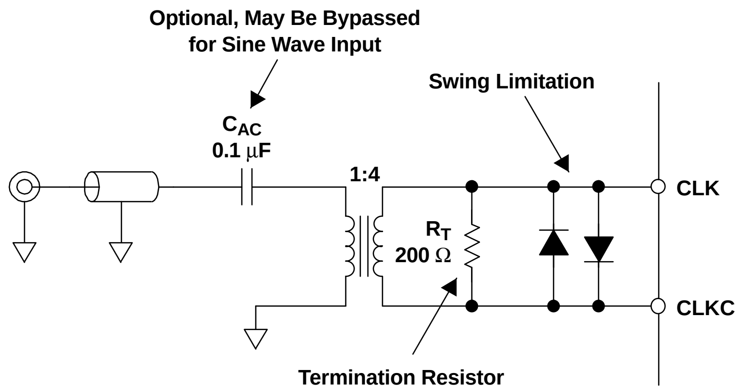


Figure 44. Preferred Clock Input Configuration

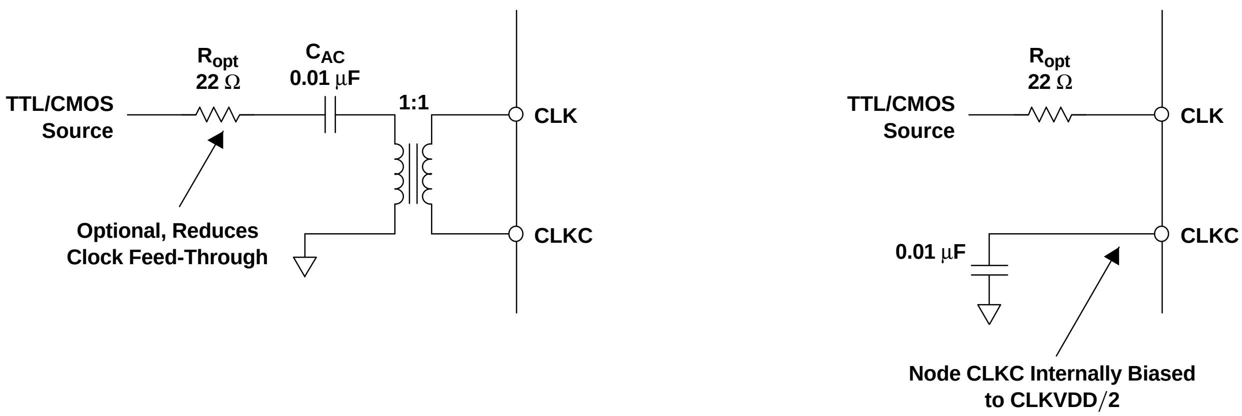


Figure 45. Driving the DAC5686 With a Single-Ended TTL/CMOS Clock Source

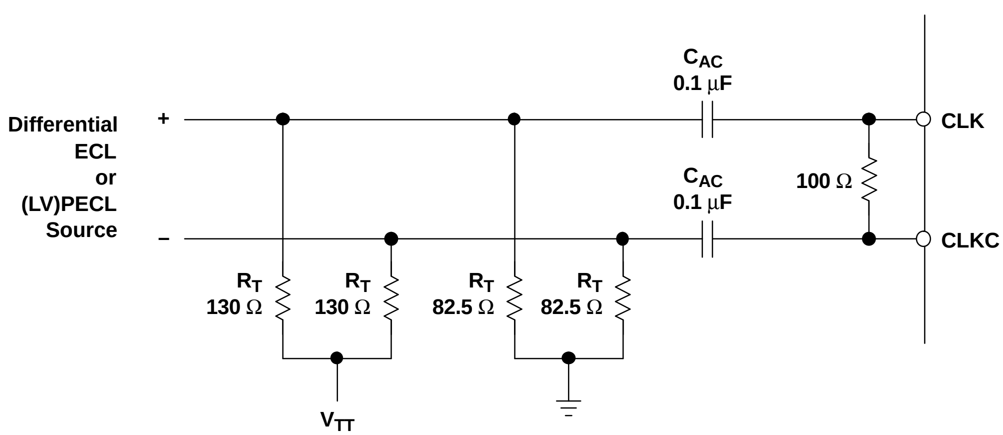


Figure 46. Driving the DAC5686 With a Differential ECL/PECL Clock Source

CLOCK INPUT AND TIMING (continued)

DAC Transfer Function

The CMOS DACs consist of a segmented array of NMOS current sources, capable of delivering a full-scale output current up to 20 mA. Differential current switches direct the current of each current source to either one of the complementary output nodes IOUT1 or IOUT2. Complementary output currents enable differential operation, thus canceling out common-mode noise sources (digital feed-through, on-chip, and PCB noise), dc offsets, even-order distortion components, and increasing signal output power by a factor of two.

The full-scale output current is set using external resistor R_{BIAS} in combination with an on-chip band-gap voltage reference source (1.2 V) and control amplifier. Current I_{BIAS} through resistor R_{BIAS} is mirrored internally to provide a full-scale output current equal to 16 times I_{BIAS}. The full-scale current can be adjusted from 20 mA down to 2 mA.

The DAC5686 delivers complementary output currents IOUT1 and IOUT2. Output current IOUT1 equals the approximate full-scale output current when all bits (after the digital processing) are high. Full-scale output current flows through terminal IOUT2 when all input bits are low. The relation between IOUT1 and IOUT2 can thus be expressed as:

$$IOUT1 = IOUT_{FS} - IOUT2$$

where $IOUT_{FS}$ is the full-scale output current. The output currents can be expressed as:

$$IOUT1 = IOUT_{FS} \times \frac{CODE}{65536}$$

$$IOUT2 = IOUT_{FS} \times \frac{(65536 - CODE)}{65536}$$

where CODE is the decimal representation of the DAC data input word. Output currents IOUT1 and IOUT2 drive resistor loads R_L or a transformer with equivalent input load resistance (R_L). This translates into single-ended voltages VOUT1 and VOUT2 at terminals IOUT1 and IOUT2, respectively, of:

$$VOUT1 = IOUT1 \times R_L = \frac{CODE}{65536 \times IOUT_{FS} \times R_L}$$

$$VOUT2 = IOUT2 \times R_L = \frac{(65536 - CODE)}{65536 \times IOUT_{FS} \times R_L}$$

The differential output voltage $VOUT_{DIFF}$ can thus be expressed as:

$$VOUT_{DIFF} = IOUT1 - VOUT2 = \frac{(2CODE - 65536)}{65536 \times IOUT_{FS} \times R_L}$$

The latter equation shows that applying the differential output results in doubling of the signal power delivered to the load. Because the output currents IOUT1 and IOUT2 are complementary, they become additive when processed differentially. Note that care should be taken not to exceed the compliance voltages at nodes IOUT1 and IOUT2, which would lead to increased signal distortion.

Reference Operation

The DAC5686 comprises a band-gap reference and control amplifier for biasing the full-scale output current. The full-scale output current is set by applying an external resistor R_{BIAS}. The bias current I_{BIAS} through resistor R_{BIAS} is defined by the on-chip band-gap reference voltage and control amplifier. The full-scale output current equals 16 times this bias current. The full-scale output current $IOUT_{FS}$ can thus be expressed as (coarse gain = 15, fine gain = 0):

$$IOUT_{FS} = \frac{16 \times V_{EXTIO}}{R_{BIAS}}$$

,

where V_{EXTIO} is the voltage at terminal EXTIO. The band-gap reference voltage delivers an accurate voltage of 1.2 V. This reference is active when terminal EXTLO is connected to AGND. An external decoupling capacitor

CLOCK INPUT AND TIMING (continued)

C_{EXT} of 0.1 μF should be connected externally to terminal EXTIO for compensation. The band-gap reference additionally can be used for external reference operation. In that case, an external buffer with a high-impedance input should be used in order to limit the band-gap load current to a maximum of 100 nA. The internal reference can be disabled and overridden by an external reference by connecting EXTLO to AVDD. Capacitor C_{EXT} may hence be omitted. Terminal EXTIO serves as either input or output node.

The full-scale output current can be adjusted from 20 mA down to 2 mA by varying resistor R_{BIAS} or changing the externally applied reference voltage. The internal control amplifier has a wide input range supporting the full-scale output current range of 20 dB.

Analog Current Outputs

Figure 47 shows a simplified schematic of the current source array with corresponding switches. Differential switches direct the current of each individual NMOS current source to either the positive output node IOUT1 or its complementary negative output node IOUT2. The output impedance is determined by the stack of the current sources and differential switches, and is typically >300 kΩ in parallel with an output capacitance of 5 pF.

The external output resistors are terminated to AVDD. The maximum output compliance at nodes IOUT1 and IOUT2 is limited to AVDD + 0.5 V, determined by the CMOS process. Beyond this value, transistor breakdown can occur, resulting in reduced reliability of the DAC5686 device. The minimum output compliance voltage at nodes IOUT1 and IOUT2 equals AVDD – 0.5 V. Exceeding the minimum output compliance voltage adversely affects distortion performance and integral nonlinearity. The optimum distortion performance for a single-ended or differential output is achieved when the maximum full-scale signal at IOUT1 and IOUT2 does not exceed 0.5 V.

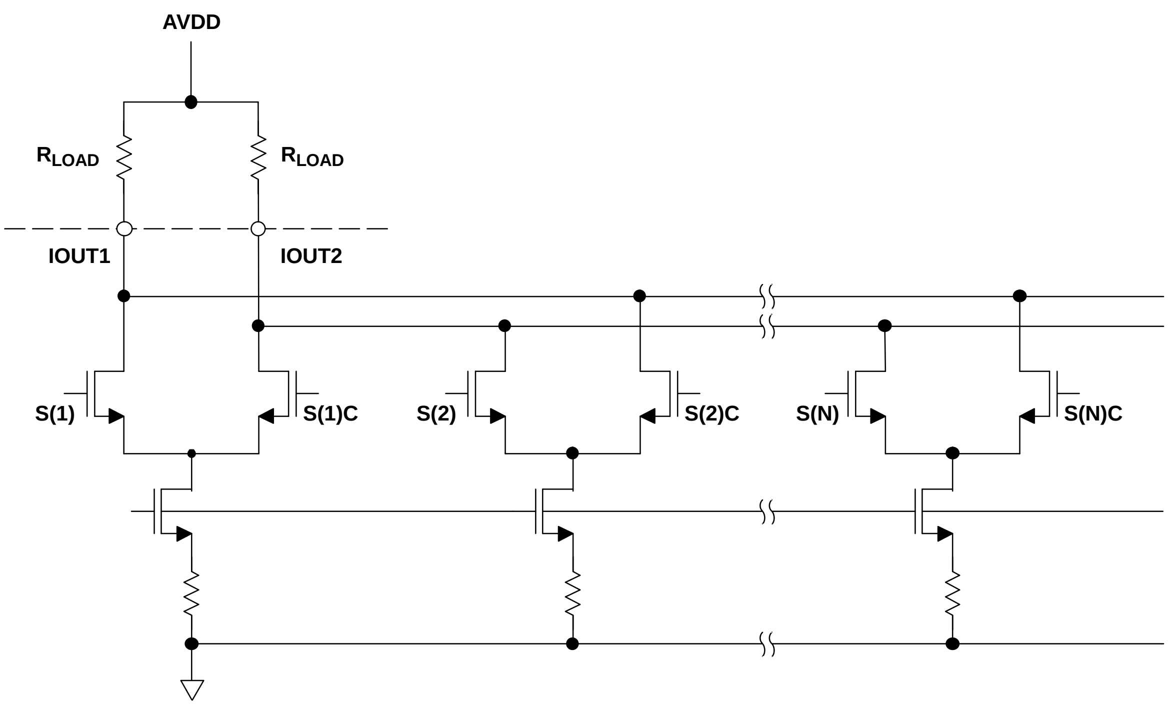


Figure 47. Equivalent Analog Current Output

The DAC5686 can be easily configured to drive a doubly terminated 50-Ω cable using a properly selected RF transformer. Figure 48 and Figure 49 show the 50-Ω doubly terminated transformer configuration with 1:1 and 4:1 impedance ratios, respectively. Note that the center tap of the primary input of the transformer must be connected to AVDD to enable a dc current flow. Applying a 20-mA full-scale output current would lead to a 0.5-Vpp output for a 1:1 transformer and a 1-Vpp output for a 4:1 transformer.

CLOCK INPUT AND TIMING (continued)

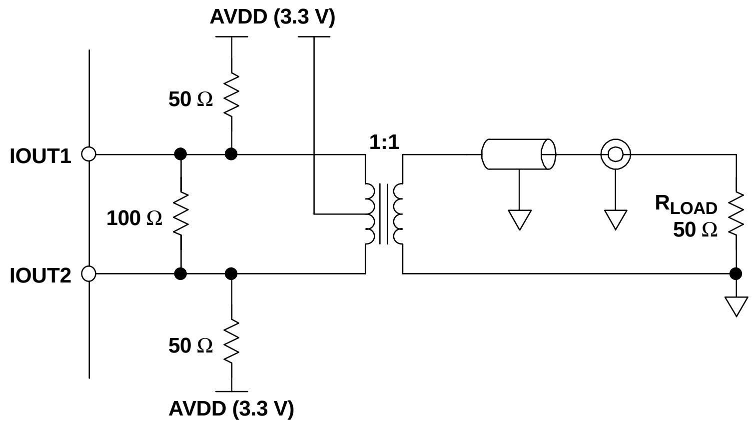


Figure 48. Driving a Doubly Terminated 50-Ω Cable Using a 1:1 Impedance-Ratio Transformer

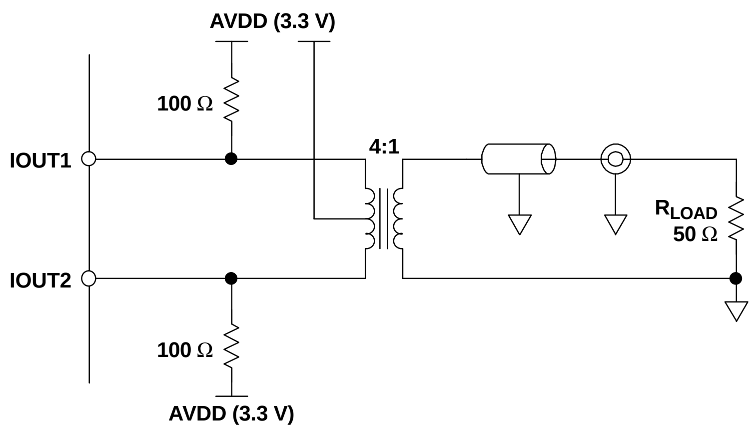


Figure 49. Driving a Doubly Terminated 50-Ω Cable Using a 4:1 Impedance-Ratio Transformer

SLEEP MODE

The DAC5686 features a power-down mode that turns off the output current and reduces the supply current to less than 5 mA over the supply range of 3 V to 3.6 V and temperature range of –40°C to 85°C. The power-down mode is activated by applying a logic level 1 to the SLEEP pin (e.g., by connecting pin SLEEP to IOVDD). An internal pulldown circuit at node SLEEP ensures that the DAC5686 is enabled if the input is left disconnected. Power-up and power-down activation times depend on the value of the external capacitor at node SLEEP. For a nominal capacitor value of 0.1 mF, it takes less than 5 ms to power down and approximately 3 ms to power up.

POWER-UP SEQUENCE

In all conditions, bring up DVDD first. If PLLVDD is powered (PLL on), CLKVDD should be powered before or simultaneously with PLLVDD. AVDD, CLKVDD and IOVDD can be powered simultaneously or in any order. Within AVDD, the multiple AVDD pins should be powered simultaneously.

DAC5686 EVALUATION BOARD

There is a combination EVM board for the DAC5686 digital-to-analog converter for evaluation. This board allows the user the flexibility to operate the DAC5686 in various configurations. Possible output configurations include transformer-coupled, resistor-terminated, inverting/non-inverting and differential amplifier outputs. The digital inputs are designed to be driven directly from various pattern generators with the onboard option to add a resistor network for proper load termination.

Appendix A. PLL LOOP FILTER COMPONENTS

For the external second-order filter shown in Figure 50, the components R, C1, and C2 are calculated for a desired phase margin and loop bandwidth. Resistor R3 = 200 Ω and capacitor C3 = 8 pF are internal to the DAC5686.

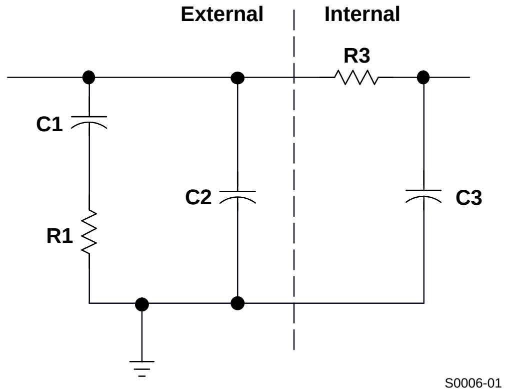


Figure 50. DAC5686 Loop Filter

The VCO gain (Gvco) as a function of VCO frequency for the DAC5686 is shown in Figure 17. For a desired VCO frequency, the loop filter values can be calculated using the following equations. Nominal PLL design parameters include:

Charge pump current:	iqp = 1 mA
VCO gain:	$K_{VCO} = 2\pi \times G_{VCO}$ rad/A
PLL divide ratio × interpolation:	N = {2, 4, 8, 16, 32}
Phase detector gain:	$K_d = iqp \times (2\pi N)^{-1}$ A/rad

Let

Desired loop bandwidth = ω_d

Desired phase margin = ϕ_d

DAC5686 EVALUATION BOARD (continued)

Then

$$C1 = \tau 1\left(1 - \frac{\tau 2}{\tau 3}\right)$$

$$C2 = \frac{\tau 1 - \tau 2}{\tau 3}$$

$$R = \frac{\tau 3^2}{\tau 1(\tau 3 - \tau 2)}$$

where

$$\tau 1 = \frac{K_d K_{VCO}}{\omega_d^2}(\tan\phi_d + \sec\phi_d)$$

$$\tau 2 = \frac{1}{\omega_d(\tan\phi_d + \sec\phi_d)}$$

$$\tau 3 = \frac{\tan\phi_d + \sec\phi_d}{\omega_d}$$

Example: $\phi_d = 70°$, $\omega_d = 1$ MHz, $G_{VCO} = 300e6$ MHz/A

N	R (Ω)	C1 (μF)	C2 (pF)
2	43	0.02	670
4	86	0.01	335
8	173	0.005	167
16	346	0.002	84
32	692	0.001	42

The calculated phase margin and loop bandwidth can be verified by plotting the gain and phase of the open-loop transfer function given by

$$H(s) = \frac{K_{VCO}K_d(1 + sRC1)}{s^3RC1C2 + s^2(C1 + C2)}$$

Figure 51 shows the open-loop gain and phase for the DAC5686 evaluation-board loop filter.

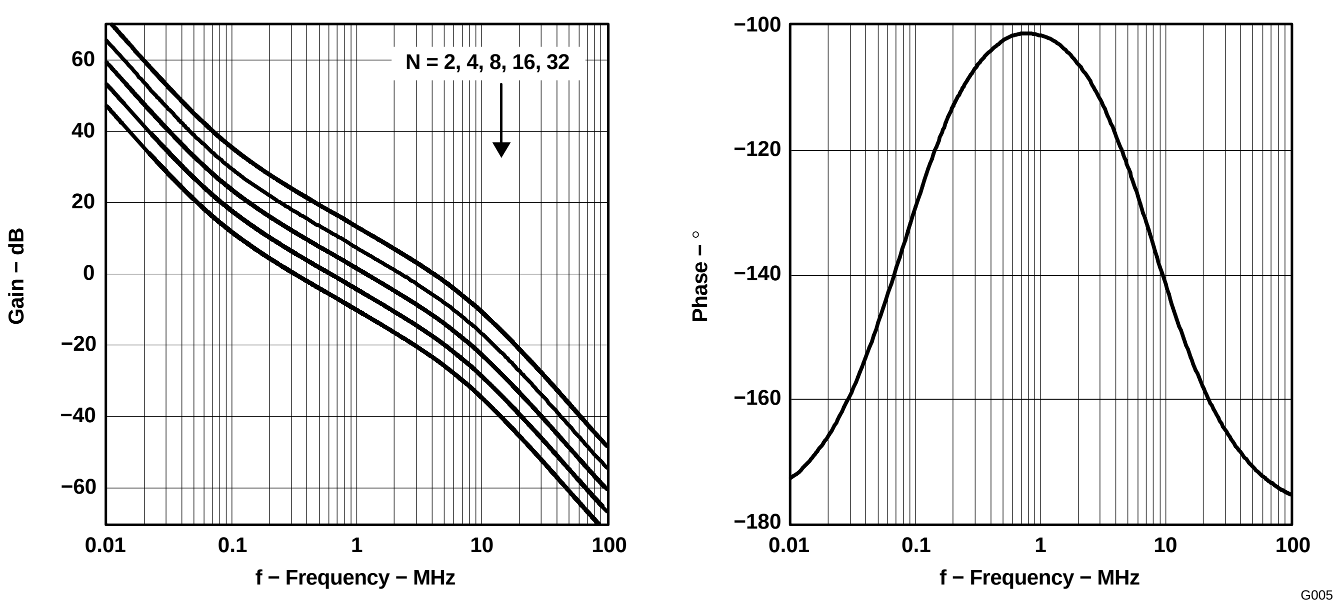


Figure 51. Open-Loop Phase and Gain Plots for DAC5686 Evaluation Board

The phase error (ϕ_{err}) phase and frequency step responses are given by the following equations and are plotted in Figure 52 for the DAC5686 evaluation-board loop filter.

$$\phi_{err} = \Delta\phi \times [1 + \omega_n t - (\omega_n t)^2] \times e^{-\omega_n t} \qquad \text{phase step response}$$

$$\phi_{err} = \frac{\Delta\omega}{\omega_n} \times [\omega_n t - (\omega_n t)^2] \times e^{-\omega_n t} \qquad \text{frequency step response}$$

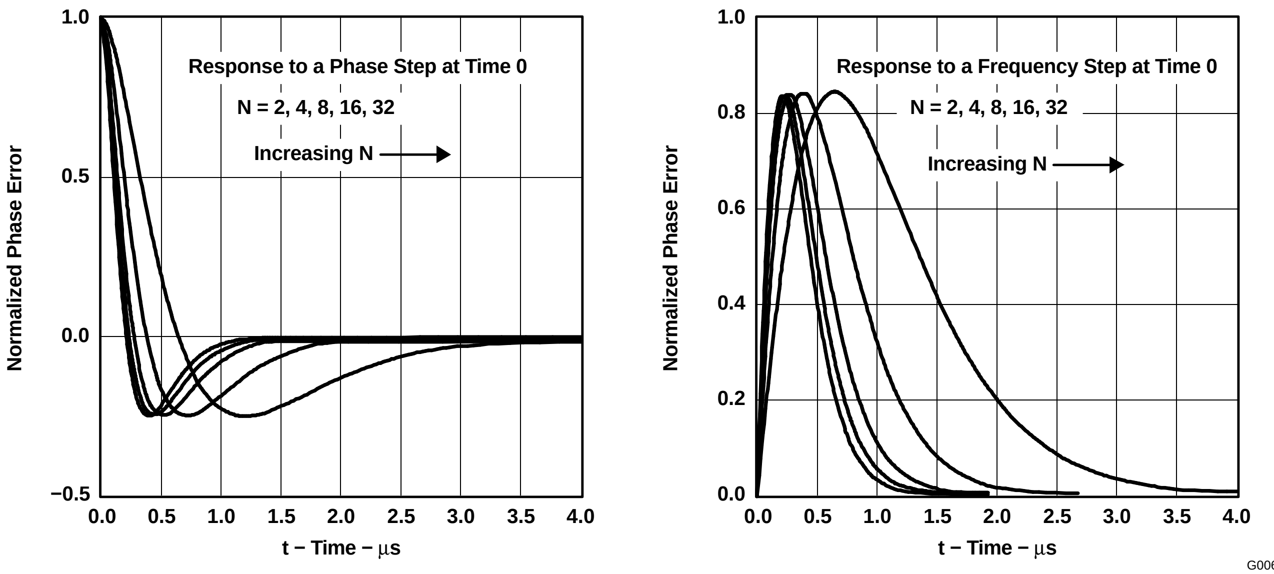


Figure 52. Phase and Frequency Step Responses for DAC5686 Evaluation Board

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