

Features

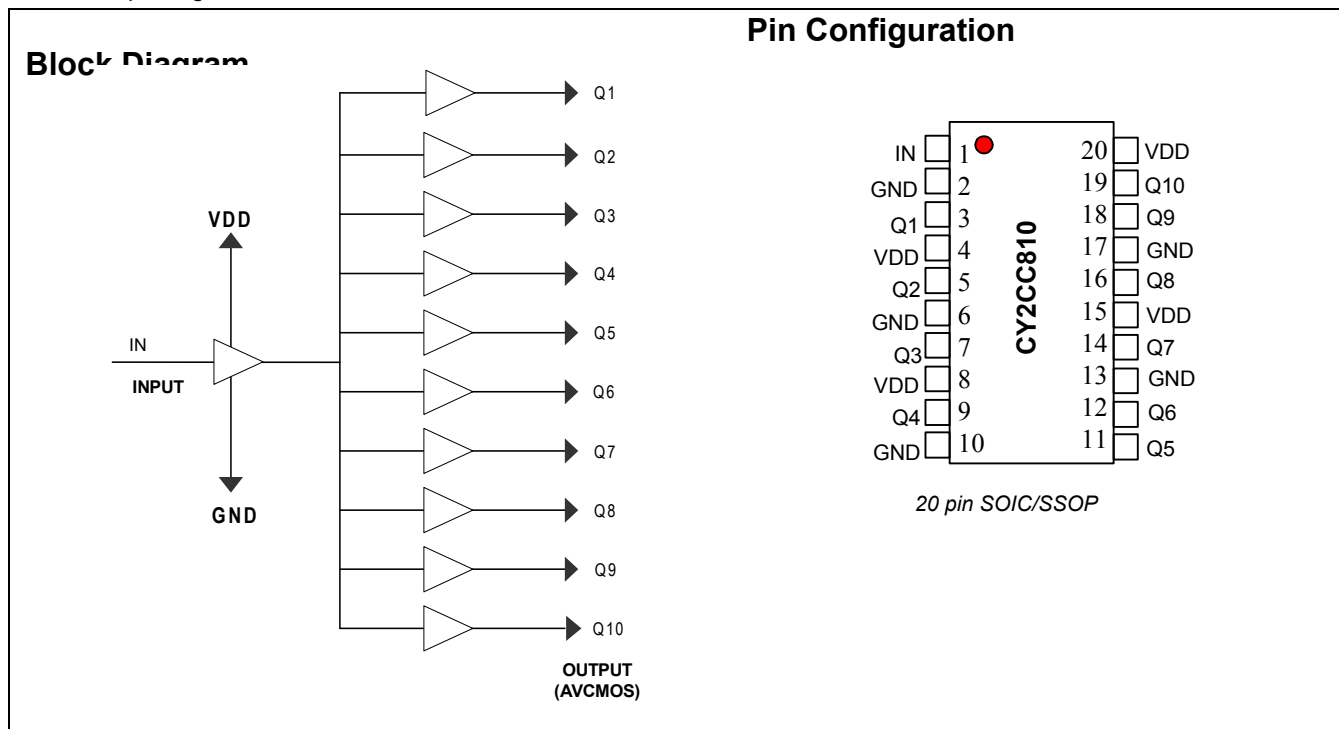
- Low-voltage operation
- V_{DD} range from 2.5V to 3.3V
- 1:10 fanout
- Over voltage tolerant input hot swappable
- Drives either a 50-Ohm or 75-Ohm transmission line
- Low-input capacitance
- 250 ps typical output-to-output skew
- 19 ps typical DJ jitter
- Typical propagation delay < 3.5 ns
- High-speed operation > 500 MHz
- Industrial temperature range
- Available packages include: SSOP

Description

The Cypress series of network circuits are produced using advanced 0.35-micron CMOS technology, achieving the industry's fastest logic and buffers.

The Cypress CY2CC810 fanout buffer features one input and ten outputs. Designed for data communications clock management applications, the large fanout from a single input reduces loading on the input clock.

AVCMOS-type outputs dynamically adjust for variable impedance matching and reduce noise overall.



Pin Description

Pin Number	Pin Name	Description	
1	IN	Input	LVC MOS
2, 6, 10, 13, 17	GND	Ground	Power
4, 8, 15, 20	V _{DD}	Power Supply	Power
3, 5, 7, 9, 11, 12, 14, 16, 18, 19	Q1... Q10	Output	AVCMOS

Absolute Maximum Conditions^[1, 2]

Parameter	Description	Min.	Max.	Unit
V _{DD}	V _{DD} Ground Supply voltage	-0.5	4.6	V
V _{IN}	Input Supply Voltage to Ground Potential	-0.5	5.8	V
V _{OUT}	Output Supply Voltage to Ground Potential	-0.5	V _{DD} + 1	V
T _S	Temperature, Storage	-65	150	°C
T _A	Temperature, Operating Ambient	-40	85	°C
	Power Dissipation	0.75		W

DC Electrical Characteristics @ 3.3V (see Figure 5)

Parameter	Description	Conditions		Min.	Typ.	Max.	Unit
V _{OH}	Output High Voltage	V _{DD} = Min., V _{IN} = V _{IH} or V _{IL}	I _{OH} = -12 mA	2.3	3.3		V
V _{OL}	Output Low Voltage	V _{DD} = Min., V _{IN} = V _{IH} or V _{IL}	I _{OL} = 12 mA		0.2	0.5	V
V _{IH}	Input High Voltage	Guaranteed Logic High Level		2		5.8	V
V _{IL}	Input Low Voltage	Guaranteed Logic Low Level				0.8	V
I _{IH}	Input High Current	V _{DD} = Max.	V _{IN} = 2.7V			1	μA
I _{IL}	Input Low Current	V _{DD} = Max.	V _{IN} = 0.5V			-1	μA
I _I	Input High Current	V _{DD} = Max., V _{IN} = V _{DD} (Max.)				20	μA
V _{IK}	Clamp Diode Voltage	V _{DD} = Min., I _{IN} = -18 mA			-0.7	-1.2	V
I _{OK}	Continuous Clamp Current	V _{DD} = Max., V _{OUT} = GND				-50	mA
O _{OFF}	Power down Disable	V _{DD} = GND, V _{OUT} = < 4.5V				100	μA
V _H	Input Hysteresis	V _{DD} = Min., V _{IN} = V _{IH} or V _{IL}			80		mV

DC Electrical Characteristics @ 2.5V (see Figure 1)

Parameter	Description	Conditions		Min.	Typ.	Max.	Unit
V _{OH}	Output High Voltage	V _{DD} = Min., V _{IN} = V _{IH} or V _{IL}	I _{OH} = -7 mA	1.8			V
			I _{OH} = 12 mA	1.6			V
V _{OL}	Output Low Voltage	V _{DD} = Min., V _{IN} = V _{IH} or V _{IL}	I _{OL} = 12 mA			0.65	V
V _{IH}	Input High Voltage	Guaranteed Logic High Level		1.6		5.0	V
V _{IL}	Input Low Voltage	Guaranteed Logic Low Level				0.8	V
I _{IH}	Input High Current	V _{DD} = Max.	V _{IN} = 2.4V			1	μA
I _{IL}	Input Low Current	V _{DD} = Max.	V _{IN} = 0.5V			-1	μA
I _I	Input High Current	V _{DD} = Max., V _{IN} = V _{DD} (Max.)				20	μA
V _{IK}	Clamp Diode Voltage	V _{DD} = Min., I _{IN} = -18 mA			-0.7	-1.2	V
I _{OK}	Continuous Clamp Current	V _{DD} = Max., V _{OUT} = GND				-50	mA
O _{OFF}	Power-down Disable	V _{DD} = GND, V _{OUT} = < 4.5V				100	μA
V _H	Input Hysteresis				80		mV

Capacitance

Parameter	Description	Test Conditions	Min.	Typ.	Max.	Unit
C _{in}	Input Capacitance	V _{IN} = 0V		2.5		pF
C _{out}	Output Capacitance	V _{OUT} = 0V		6.5		pF

Power Supply Characteristics (see Figure 5)

Parameter	Description	Test Conditions	Min.	Typ.	Max.	Unit
ΔI _{CC}	Delta I _{CC} Quiescent Power Supply Current	(I _{DD} @ V _{DD} = Max. and V _{IN} = V _{DD}) – (I _{DD} @ V _{DD} = Max. and V _{IN} = V _{DD} – 0.6V)			50	μA
I _{CCD}	Dynamic Power Supply Current	V _{DD} = Max. Input toggling 50% Duty Cycle, Outputs Open			0.63	mA/MHz
I _C	Total Power Supply Current	V _{DD} = Max. Input toggling 50% Duty Cycle, Outputs Open f _L = 40 MHz			25	mA
t _{PU}	Power-up time for all V _{DD} S	Power-up to reach minimum specified voltage (power ramp must be monotonic)	0.05		500	ms

High-frequency Parametrics

Parameter	Description	Test Conditions	Min.	Typ.	Max.	Unit	
D _J	Jitter, Deterministic	50% duty cycle t _W (50–50) The “point to point load circuit” Output Jitter – Input Jitter	2.5V		23	35	ps
			3.3V		19	30	ps
F _{max(3.3V)}	Maximum frequency V _{DD} = 3.3V	50% duty cycle t _W (50–50) Standard Load Circuit.	See Figure 5			160	MHz
		50% duty cycle t _W (50–50) The “point to point load circuit”	See Figure 7			650	
F _{max(2.5V)}	Maximum frequency V _{DD} = 2.5V	The “point to point load circuit” V _{IN} = 2.4V/0.0V V _{OUT} = 1.7V/0.7V	See Figure 7			200	MHz
F _{max(20)}	Maximum frequency V _{DD} = 3.3V	20% duty cycle t _W (20–80) The “point to point load circuit” V _{IN} = 3.0V/0.0V V _{OUT} = 2.3V/0.4V	See Figure 7			250	MHz
		Maximum frequency V _{DD} = 2.5V	See Figure 3			200	
t _W	Minimum pulse V _{DD} = 3.3V	The “point to point load circuit” V _{IN} = 3.0V/0.0V F = 100 MHz V _{OUT} = 2.0V/0.8V	See Figure 7	1			ns
		The “point to point load circuit” V _{IN} = 2.4V/0.0V F = 100 MHz V _{OUT} = 1.7V/0.7V	See Figure 3	1			

Note

- Stresses greater than those listed under absolute maximum ratings may cause permanent damage to the device. This is intended to be a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operation sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.
- Multiple Supplies: The voltage on any input or I/O pin cannot exceed the power pin during power-up. Power supply sequencing is NOT required.

AC Switching Characteristics @ 3.3V, $V_{DD} = 3.3V \pm 5\%$, Temperature = $-40^{\circ}C$ to $+85^{\circ}C$

Parameter	Description	Min.	Typ.	Max.	Unit
t_{PLH}	Propagation Delay – Low to High	1.5	2.7	3.5	ns
t_{PHL}	Propagation Delay – High to Low				
t_R	Output Rise Time		0.8		V/ns
t_F	Output Fall Time		0.8		V/ns
$t_{SK(0)}$	Output Skew: Skew between outputs of the same package (in phase)	See Figure 10	0.25	0.38	ns
$t_{SK(p)}$	Pulse Skew: Skew between opposite transitions of the same output ($t_{PHL} - t_{PLH}$)	See Figure 9		0.2	ns
$t_{SK(t)}$	Package Skew: Skew between outputs of different packages at the same power supply voltage, temperature and package type.	See Figure 11		0.42	ns

AC Switching Characteristics @ 2.5V, $V_{DD} = 2.5V \pm 5\%$, Temperature = $-40^{\circ}C$ to $+85^{\circ}C$

Parameter	Description	Min.	Typ.	Max.	Unit
t_{PLH}	Propagation Delay – Low to High	1.5	2.0	3.5	ns
t_{PHL}	Propagation Delay – High to Low				
t_R	Output Rise Time		0.8		V/ns
t_F	Output Fall Time		0.8		V/ns
$t_{SK(0)}$	Output Skew: Skew between outputs of the same package (in phase)	See Figure 10	0.25	0.38	ns
$t_{SK(p)}$	Pulse Skew: Skew between opposite transitions of the same output ($t_{PHL} - t_{PLH}$)	See Figure 9		0.4	ns
$t_{SK(t)}$	Package Skew: Skew between outputs of different packages at the same power supply voltage, temperature and package type.	See Figure 11		0.65	ns

Parameter Measurement Information: V_{DD} @ 2.5V

Figure 1. Load Circuit [3,4,5]
f

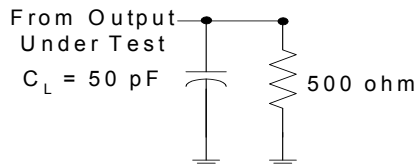
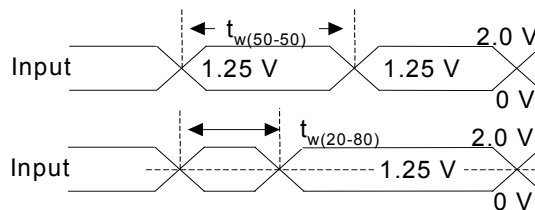


Figure 2. Voltage Waveforms Pulse Duration [6]



Notes

- C_L includes probe and jig capacitance.
- All input pulses are supplied by generators having the following characteristics: PRR < 100 MHz, $Z_0 = 50\Omega$, $t_R < 2.5$ ns, $t_F < 2.5$ ns.
- The outputs are measured one at a time with one transition per measurement.
- t_{PLH} and t_{PHL} are the same as t_{pd} .

Figure 3. Point to Point Load Circuit^[3,4,5]

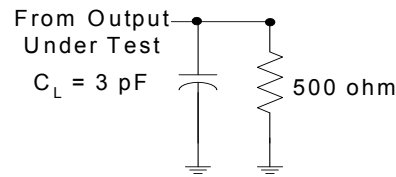
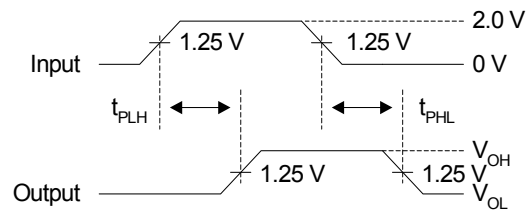


Figure 4. Voltage Waveforms Propagation Delay Times^[4]



Parameter Measurement Information: V_{DD} @ 3.3V

Figure 5. Load Circuit [3,4,5]

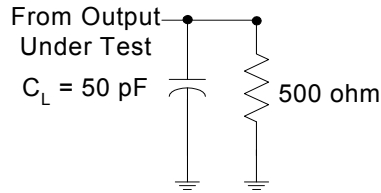


Figure 6. Voltage Waveforms—Pulse Duration [6]

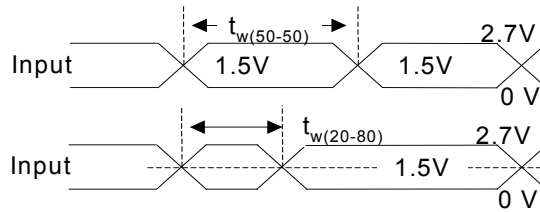


Figure 7. Point to Point Load Circuit [3,4,5]

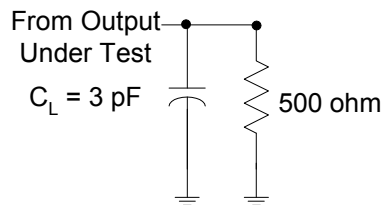


Figure 8. Voltage Waveforms Propagation Delay Times [4]

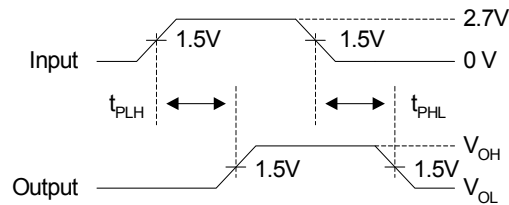


Figure 9. Pulse Skew- $tsk_{(p)}$

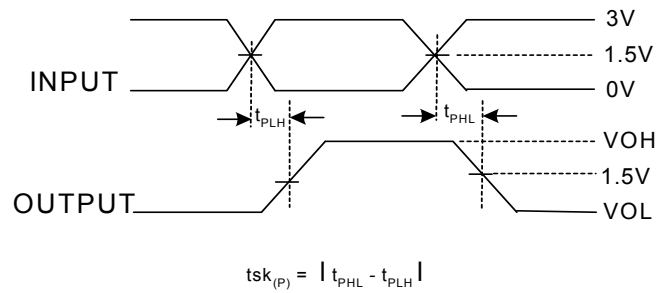


Figure 10. Output Skew- $tsk_{(o)}$

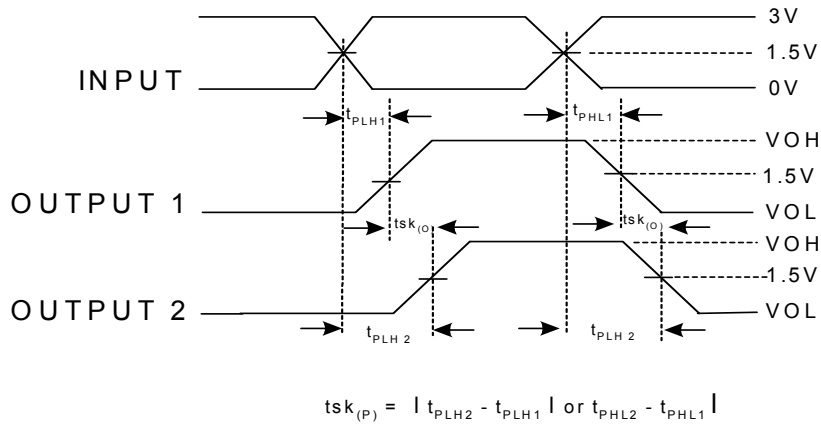
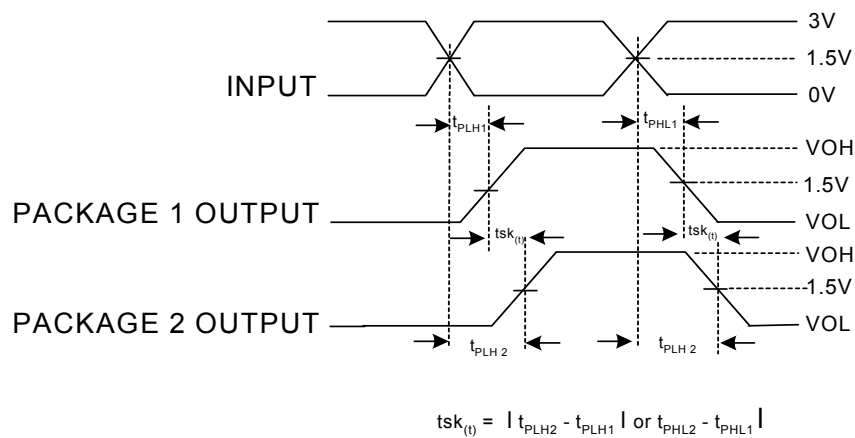


Figure 11. Package Skew- $tsk_{(t)}$

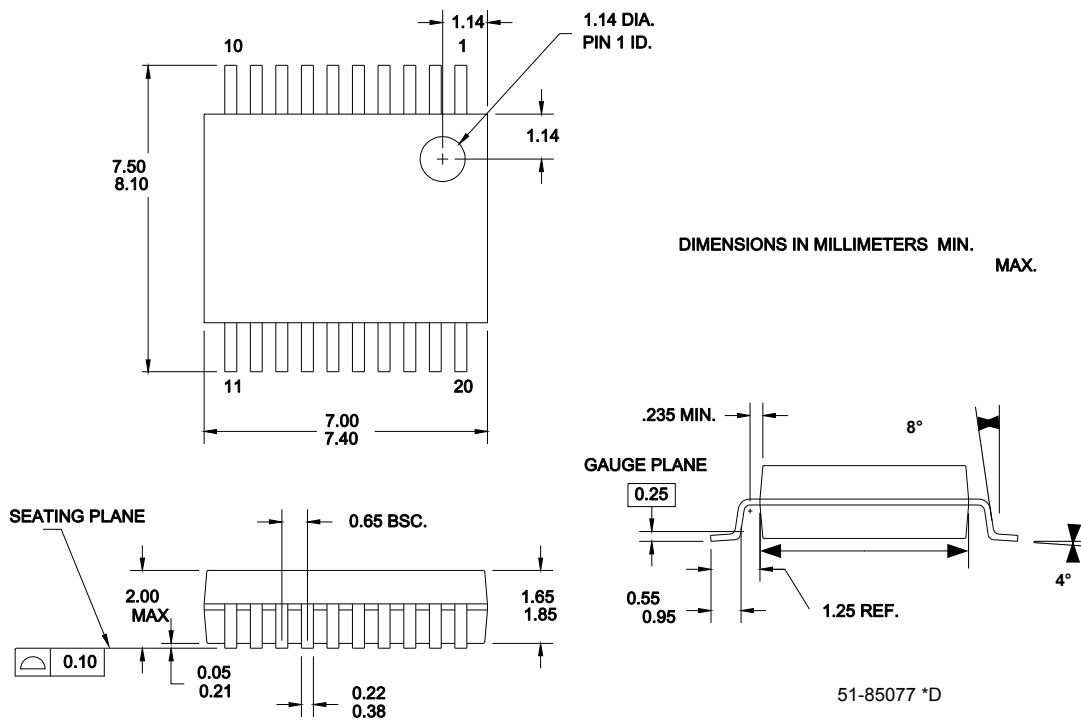


Ordering Information

Part Number ^[7]	Package Type	Product Flow
Pb-free		
CY2CC8100XI	20-pin SSOP	Industrial, -40°C to 85°C
CY2CC8100XIT	20-pin SSOP–Tape and Reel	Industrial, -40°C to 85°C
CY2CC8100XI-1	20-pin SSOP	Industrial, -40°C to 85°C
CY2CC8100XI-1T	20-pin SSOP–Tape and Reel	Industrial, -40°C to 85°C

Package Drawing and Dimensions

Figure 12. 20-Pin (5.3-mm) Shrunken Small Outline Package O20



Note

7. Devices with part numbers ending with -1 are identical to devices without the -1 suffix. There are no differences in specification.

Document History Page

Document Title: CY2CC810 1:10 Clock Fanout Buffer Document #: 38-07056				
Rev.	ECN No.	Submission Date	Orig. of Change	Description of Change
**	107081	06/07/01	IKA	Convert from IMI to Cypress
*A	114315	05/09/02	TSM	ΔI_{DD} Validation
*B	119117	10/07/02	RGL	Added 5.8 as the Max. value of V_{IH} in the DC Electrical Characteristics @3.3V table. Changed the Max. value of V_{IH} from 1.8 to 5.0 in the DC Electrical Characteristics @2.5V table.
*C	122743	12/14/02	RBI	Added power up requirements to maximum ratings information.
*D	387761	See ECN	RGL	Added typical values Updated jitter and skew specs. Removed devices with SOIC package Added Lead-free SSOP package
*E	499991	See ECN	RGL	Added tpu parameter in the Power Supply Characteristics table
*F	2896073	03/19/10	CXQ	Updated package diagram Removed obsolete parts from ordering information table and added CY2CC810OXI-1, CY2CC810OXI-1T Removed reference to SOIC packages
*G	3056154	10/08/2010	CXQ	Removed CY2CC810OXC and CY2CC810OXCT parts from Ordering Information .

Sales, Solutions, and Legal Information

Worldwide Sales and Design Support

Cypress maintains a worldwide network of offices, solution centers, manufacturer's representatives, and distributors. To find the office closest to you, visit us at [Cypress Locations](#).

Products

Automotive	cypress.com/go/automotive
Clocks & Buffers	cypress.com/go/clocks
Interface	cypress.com/go/interface
Lighting & Power Control	cypress.com/go/powerpsoc cypress.com/go/plc
Memory	cypress.com/go/memory
Optical & Image Sensing	cypress.com/go/image
PSoC	cypress.com/go/psoc
Touch Sensing	cypress.com/go/touch
USB Controllers	cypress.com/go/USB
Wireless/RF	cypress.com/go/wireless

PSoC Solutions

psoc.cypress.com/solutions
PSoC 1 | PSoC 3 | PSoC 5

© Cypress Semiconductor Corporation, 2006-2010. The information contained herein is subject to change without notice. Cypress Semiconductor Corporation assumes no responsibility for the use of any circuitry other than circuitry embodied in a Cypress product. Nor does it convey or imply any license under patent or other rights. Cypress products are not warranted nor intended to be used for medical, life support, life saving, critical control or safety applications, unless pursuant to an express written agreement with Cypress. Furthermore, Cypress does not authorize its products for use as critical components in life-support systems where a malfunction or failure may reasonably be expected to result in significant injury to the user. The inclusion of Cypress products in life-support systems application implies that the manufacturer assumes all risk of such use and in doing so indemnifies Cypress against all charges.

Any Source Code (software and/or firmware) is owned by Cypress Semiconductor Corporation (Cypress) and is protected by and subject to worldwide patent protection (United States and foreign), United States copyright laws and international treaty provisions. Cypress hereby grants to licensee a personal, non-exclusive, non-transferable license to copy, use, modify, create derivative works of, and compile the Cypress Source Code and derivative works for the sole purpose of creating custom software and or firmware in support of licensee product to be used only in conjunction with a Cypress integrated circuit as specified in the applicable agreement. Any reproduction, modification, translation, compilation, or representation of this Source Code except as specified above is prohibited without the express written permission of Cypress.

Disclaimer: CYPRESS MAKES NO WARRANTY OF ANY KIND, EXPRESS OR IMPLIED, WITH REGARD TO THIS MATERIAL, INCLUDING, BUT NOT LIMITED TO, THE IMPLIED WARRANTIES OF MERCHANTABILITY AND FITNESS FOR A PARTICULAR PURPOSE. Cypress reserves the right to make changes without further notice to the materials described herein. Cypress does not assume any liability arising out of the application or use of any product or circuit described herein. Cypress does not authorize its products for use as critical components in life-support systems where a malfunction or failure may reasonably be expected to result in significant injury to the user. The inclusion of Cypress' product in a life-support systems application implies that the manufacturer assumes all risk of such use and in doing so indemnifies Cypress against all charges.

Use may be limited by and subject to the applicable Cypress software license agreement.