TIP35A, TIP35B, TIP35C (NPN); TIP36A, TIP36B, TIP36C (PNP)

TIP35B, TIP35C, TIP36B, and TIP36C are Preferred Devices

Complementary Silicon High-Power Transistors

Designed for general−purpose power amplifier and switching applications.

Features

- 25 A Collector Current
- Low Leakage Current −
  I_{CEO} = 1.0 mA @ 30 and 60 V
- Excellent DC Gain −
  h_{FE} = 40 Typ @ 15 A
- High Current Gain Bandwidth Product −
  $|h_{fe}|$ = 3.0 min @ I_C
  = 1.0 A, f = 1.0 MHz
- Pb−Free Packages are Available*

MAXIMUM RATINGS

Rating	Symbol	TIP35A TIP36A	TIP35B TIP36B	TIP35C TIP36C	Unit
Collector − Emitter Voltage	V_{CEO}	60	80	100	Vdc
Collector − Base Voltage	V_{CB}	60	80	100	Vdc
Emitter − Base Voltage	V_{EB}	5.0			Vdc
Collector Current − Continuous − Peak (Note 1)	I_C	25 40			Adc
Base Current − Continuous	I_B	5.0			Adc
Total Power Dissipation @ T_C = 25°C Derate above 25°C	P_D	125			W W/°C
Operating and Storage Junction Temperature Range	T_J, T_{stg}	−65 to +150			°C
Unclamped Inductive Load	E_{SB}	90			mJ

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction−to−Case	$R_{\theta JC}$	1.0	°C/W
Junction−To−Free−Air Thermal Resistance	$R_{\theta JA}$	35.7	°C/W

Maximum ratings are those values beyond which device damage can occur. Maximum ratings applied to the device are individual stress limit values (not normal operating conditions) and are not valid simultaneously. If these limits are exceeded, device functional operation is not implied, damage may occur and reliability may be affected.

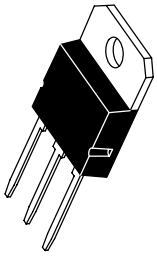
1. Pulse Test: Pulse Width = 10 ms, Duty Cycle ≤ 10%.

*For additional information on our Pb−Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

ON Semiconductor®

http://onsemi.com

25 AMPERE COMPLEMENTARY SILICON POWER TRANSISTORS 60−100 VOLTS, 125 WATTS



SOT−93 (TO−218)
CASE 340D
STYLE 1

MARKING DIAGRAM

A	=	Assembly Location
Y	=	Year
WW	=	Work Week
TIP3xx	=	Device Code
xx	=	5A, 5B, 5C 6A, 6B, 6C
G	=	Pb−Free Package

ORDERING INFORMATION

See detailed ordering and shipping information in the package dimensions section on page 2 of this data sheet.

Preferred devices are recommended choices for future use and best overall value.

ORDERING INFORMATION

Device	Package	Shipping
TIP35A	SOT−93 (TO−218)	30 Units / Rail
TIP35AG	SOT−93 (TO−218) (Pb−Free)	30 Units / Rail
TIP35B	SOT−93 (TO−218)	30 Units / Rail
TIP35BG	SOT−93 (TO−218) (Pb−Free)	30 Units / Rail
TIP35C	SOT−93 (TO−218)	30 Units / Rail
TIP35CG	SOT−93 (TO−218) (Pb−Free)	30 Units / Rail
TIP36A	SOT−93 (TO−218)	30 Units / Rail
TIP36AG	SOT−93 (TO−218) (Pb−Free)	30 Units / Rail
TIP36B	SOT−93 (TO−218)	30 Units / Rail
TIP36BG	SOT−93 (TO−218) (Pb−Free)	30 Units / Rail
TIP36C	SOT−93 (TO−218)	30 Units / Rail
TIP36CG	SOT−93 (TO−218) (Pb−Free)	30 Units / Rail

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic		Symbol	Min	Max	Unit
OFF CHARACTERISTICS					
Collector−Emitter Sustaining Voltage (Note 2)		$V_{CEO(sus)}$			Vdc
(I_C = 30 mA, I_B = 0)	TIP35A, TIP36A		60	−	
	TIP35B, TIP36B		80	−	
	TIP35C, TIP36C		100	−	
Collector−Emitter Cutoff Current		I_{CEO}			mA
(V_{CE} = 30 V, I_B = 0)	TIP35A, TIP36A		−	1.0	
(V_{CE} = 60 V, I_B = 0)	TIP35B, TIP35C, TIP36B, TIP36C		−	1.0	
Collector−Emitter Cutoff Current (V_{CE} = Rated V_{CEO}, V_{EB} = 0)		I_{CES}	−	0.7	mA
Emitter−Base Cutoff Current (V_{EB} = 5.0 V, I_C = 0)		I_{EBO}	−	1.0	mA
ON CHARACTERISTICS (Note 2)					
DC Current Gain		h_{FE}			−
(I_C = 1.5 A, V_{CE} = 4.0 V)			25	−	
(I_C = 15 A, V_{CE} = 4.0 V)			15	75	
Collector−Emitter Saturation Voltage		$V_{CE(sat)}$			Vdc
(I_C = 15 A, I_B = 1.5 A)			−	1.8	
(I_C = 25 A, I_B = 5.0 A)			−	4.0	
Base−Emitter On Voltage		$V_{BE(on)}$			Vdc
(I_C = 15 A, V_{CE} = 4.0 V)			−	2.0	
(I_C = 25 A, V_{CE} = 4.0 V)			−	4.0	
DYNAMIC CHARACTERISTICS					
Small−Signal Current Gain (I_C = 1.0 A, V_{CE} = 10 V, f = 1.0 kHz)		h_{fe}	25	−	−
Current−Gain — Bandwidth Product (I_C = 1.0 A, V_{CE} = 10 V, f = 1.0 MHz)		f_T	3.0	−	MHz

2. Pulse Test: Pulse Width = 300 μs, Duty Cycle ≤ 2.0%.

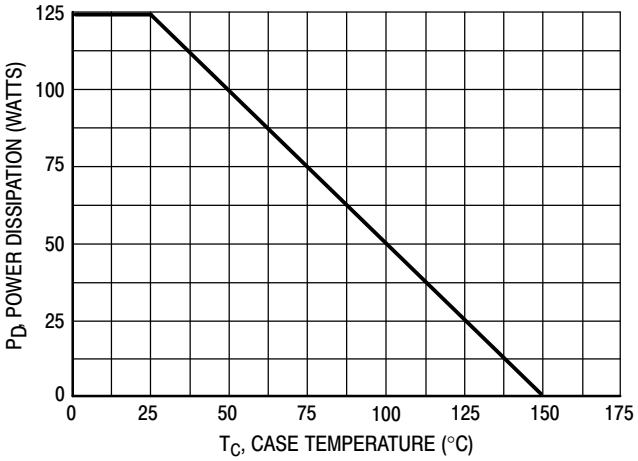
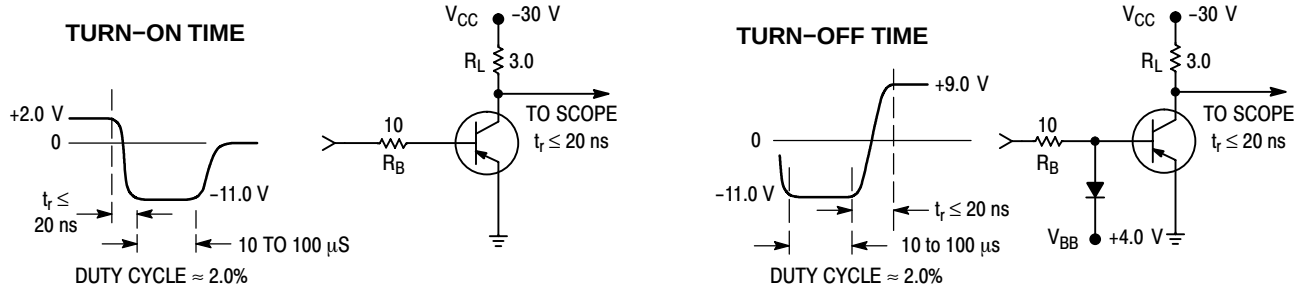


Figure 1. Power Derating



FOR CURVES OF FIGURES 3 & 4, R_B & R_L ARE VARIED.
INPUT LEVELS ARE APPROXIMATELY AS SHOWN.
FOR NPN, REVERSE ALL POLARITIES.

Figure 2. Switching Time Equivalent Test Circuits

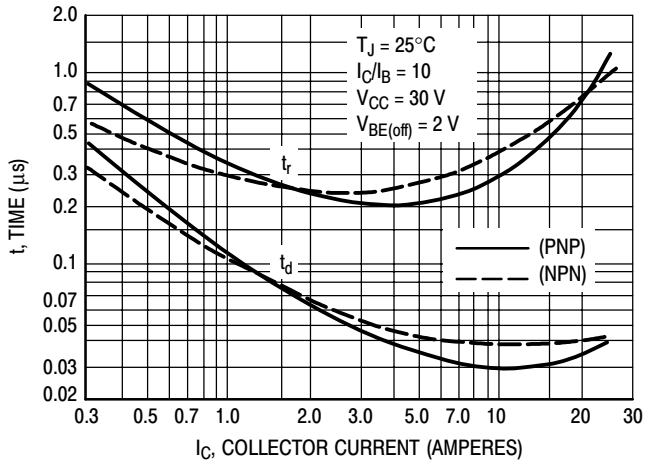


Figure 3. Turn−On Time

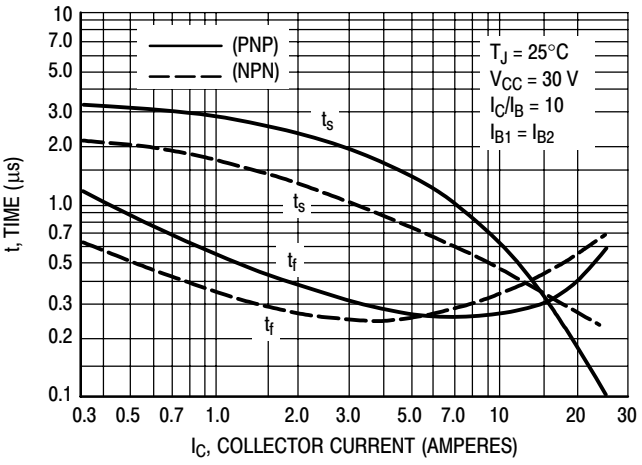


Figure 4. Turn−Off Time

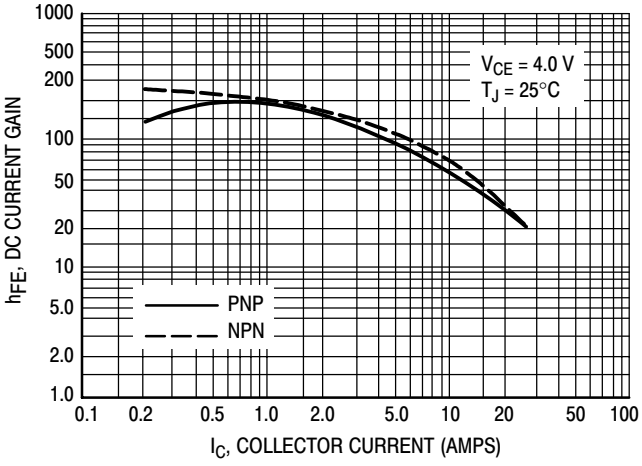


Figure 5. DC Current Gain

FORWARD BIAS

There are two limitations on the power handling ability of a transistor: average junction temperature and second breakdown. Safe operating area curves indicate $I_C - V_{CE}$ limits of the transistor that must be observed for reliable operation; i.e., the transistor must not be subjected to greater dissipation than the curves indicate.

The data of Figure 6 is based on T_C = 25°C; $T_{J(pk)}$ is variable depending on power level. Second breakdown pulse limits are valid for duty cycles to 10% but must be derated when $T_C \geq$ 25°C. Second breakdown limitations do not derate the same as thermal limitations.

REVERSE BIAS

For inductive loads, high voltage and high current must be sustained simultaneously during turn−off, in most cases, with the base to emitter junction reverse biased. Under these conditions the collector voltage must be held to a safe level at or below a specific value of collector current. This can be accomplished by several means such as active clamping, RC snubbing, load line shaping, etc. The safe level for these devices is specified as Reverse Bias Safe Operating Area and represents the voltage−current conditions during reverse biased turn−off. This rating is verified under clamped conditions so that the device is never subjected to an avalanche mode. Figure 7 gives RBSOA characteristics.

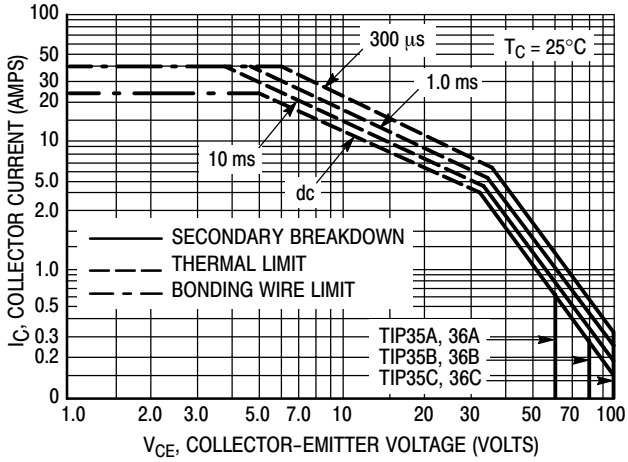


Figure 6. Maximum Rated Forward Bias Safe Operating Area

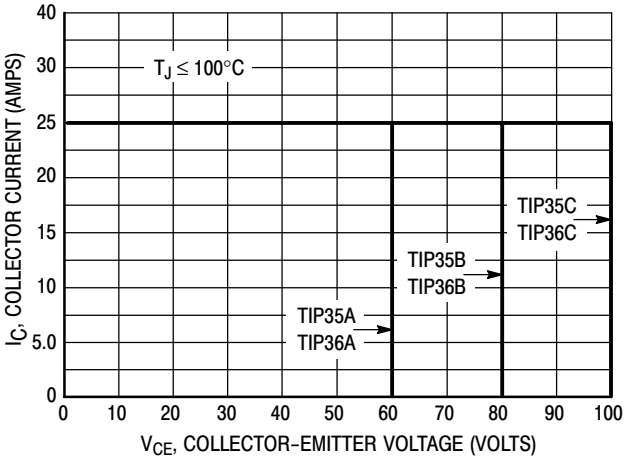
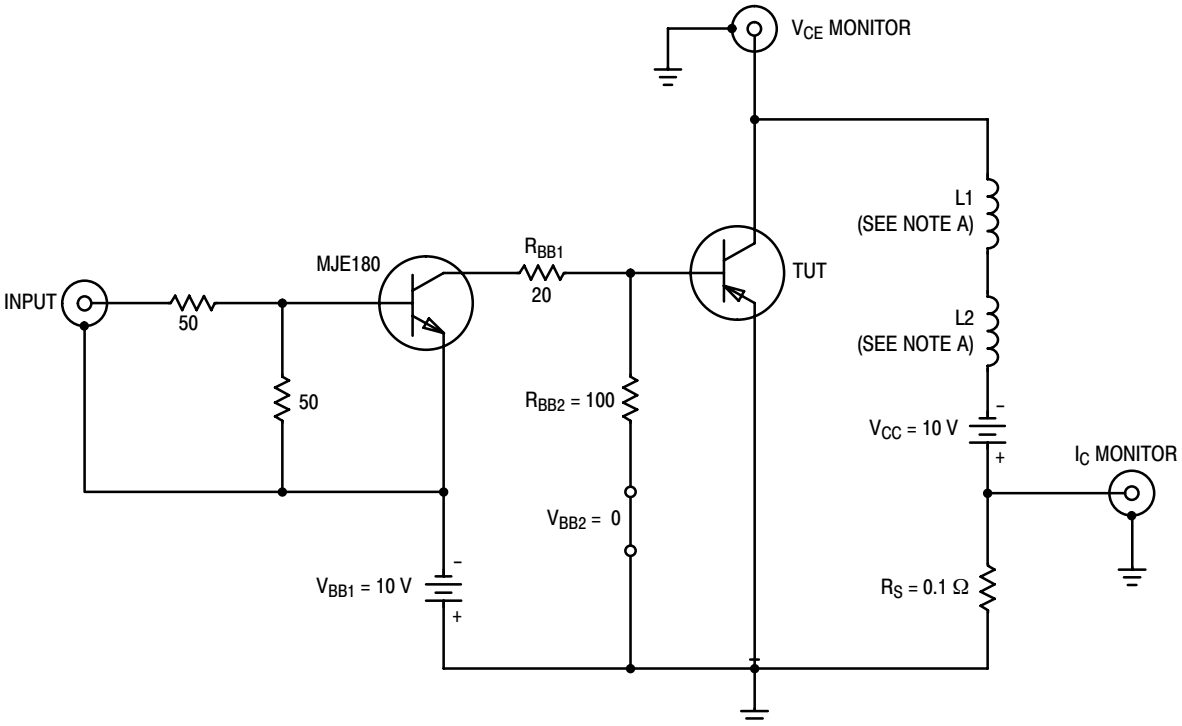
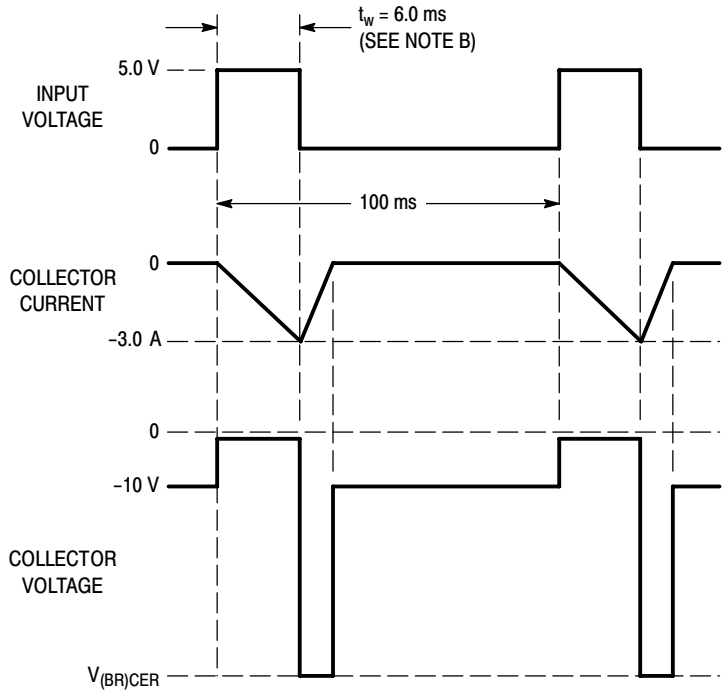


Figure 7. Maximum Rated Forward Bias Safe Operating Area

TEST CIRCUIT



VOLTAGE AND CURRENT WAVEFORMS



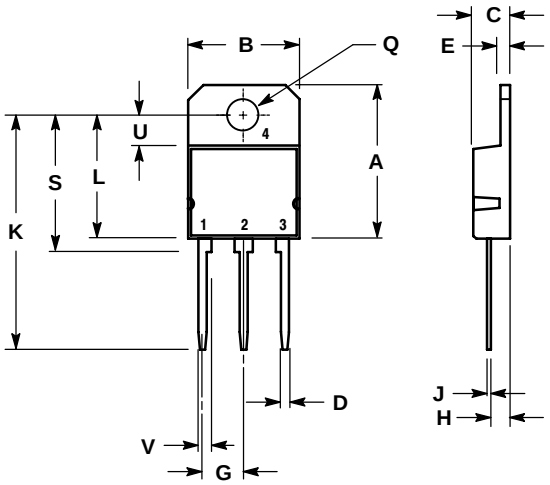
NOTES:

A. L1 and L2 are 10 mH, 0.11 Ω, Chicago Standard Transformer Corporation C−2688, or equivalent.
B. Input pulse width is increased until I_{CM} = −3.0 A.
C. For NPN, reverse all polarities.

Figure 8. Inductive Load Switching

PACKAGE DIMENSIONS

SOT−93 (TO−218)
CASE 340D−02
ISSUE E



NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	---	20.35	---	0.801
B	14.70	15.20	0.579	0.598
C	4.70	4.90	0.185	0.193
D	1.10	1.30	0.043	0.051
E	1.17	1.37	0.046	0.054
G	5.40	5.55	0.213	0.219
H	2.00	3.00	0.079	0.118
J	0.50	0.78	0.020	0.031
K	31.00 REF		1.220 REF	
L	---	16.20	---	0.638
Q	4.00	4.10	0.158	0.161
S	17.80	18.20	0.701	0.717
U	4.00 REF		0.157 REF	
V	1.75 REF		0.069	

STYLE 1:
PIN 1. BASE
2. COLLECTOR
3. EMITTER
4. COLLECTOR

PUBLICATION ORDERING INFORMATION

LITERATURE FULFILLMENT:
Literature Distribution Center for ON Semiconductor
P.O. Box 61312, Phoenix, Arizona 85082−1312 USA
Phone: 480−829−7710 or 800−344−3860 Toll Free USA/Canada
Fax: 480−829−7709 or 800−344−3867 Toll Free USA/Canada
Email: orderlit@onsemi.com

N. American Technical Support: 800−282−9855 Toll Free USA/Canada

Japan: ON Semiconductor, Japan Customer Focus Center
2−9−1 Kamimeguro, Meguro−ku, Tokyo, Japan 153−0051
Phone: 81−3−5773−3850

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Order Literature: http://www.onsemi.com/litorder

For additional information, please contact your local Sales Representative.

TIP35A/D