DATA SHEET

TDA9991HL
Vertical line driver and DC-DC converter for Full Frame and Frame Transfer CCD image sensors

Preliminary specification
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Philips
Semiconductors

PHILIPS

Vertical line driver and DC-DC converter for Full Frame and Frame Transfer CCD image sensors

TDA9991HL

FEATURES

- Enables compact and cost effective camera design
- Eight two-level low-ohmic line drivers suitable for Philips Full Frame (FF) and Frame Transfer (FT) CCD image sensors
- Versatile programmable DC-DC converters and voltage regulators to create all required low-noise supply voltages for the Philips FT CCD sensor family and for the on-chip drivers
- DC-DC converter can be operated with an on-chip free running oscillator or with an external clock
- Wide supply range also suitable for direct use on batteries
- Electronic shutter driver (charge reset)
- Fast start-up
- DC ready signal available indicating the TDA9991HL has started up
- 3-wire serial bus
- Separate digital supply voltage for optimal interfacing with DSP circuit and serial bus
- Low current consumption in Power-down mode.

APPLICATIONS

- Digital still camera
- Desktop video camera
- Security camera
- Camcorder
- DSP applications.

GENERAL DESCRIPTION

The TDA9991HL forms the interface between the pulse pattern generator and the CCD image sensor in camera systems and minimizes the component count significantly by integration of various functions. The device contains eight vertical line drivers, a shutter driver for charge reset, a versatile programmable DC-DC converter, a non-programmable DC-DC converter and voltage regulators which create all required low noise supply voltages for FT and FF CCD sensors. A three wire serial bus, similar to the ones used in the Philips front-end ICs (TDA8786 and TDA8783) is used for programming the device.

The versatile programmable DC-DC converter generates two positive voltages (V_{CAPNS} and V_{CAPH}) and the non programmable DC-DC converter generates a negative voltage (V_{VL}) which is used internally. Voltage regulators convert the DC-DC converter outputs into low-noise output voltages (V_{NS}, V_{SFD}, V_{HFB} and V_{SH}). The required voltages for the image sensor and the drivers can be programmed via the serial bus with sufficient accuracy to optimize the performance of the sensors. An on-board reference voltage ensures stable output voltages over the entire temperature range.

An internal DCOK signal enables the vertical line drivers when the DC-DC converter output voltages and the regulator output voltages are at their required (programmable) level. When either V_{HFB}, V_{CAPNS} or V_{NS} drops below 80% of it's programmed level, the DCOK signal will become LOW. A signal on pin START (inverse of DCOK signal) indicates that the device has started up and is externally available.

The use of two external coils enables high efficiency of the DC-DC converters and fast starting up. The maximum current built-up in coil L2 can be set with an external resistor R_{LIM} optimizing the efficiency of the DC-DC converter and making it independent of supply voltage variations.

The DC-DC converter operates from an on-chip free running oscillator or from an external clock signal.

The low impedance of the drivers enables fast transfer of the image of the sensor. The drivers can switch between 0 V and V_{HFB} (8 to 15 V). The eight vertical drivers (image gate drivers) can be put into 3-state via the serial bus.

Charge reset of the CCD can be performed with a separate electronic shutter driver.

When the TDA9991 is in Power-on mode, a HIGH level at pin PWD will put the chip in Power-down mode. A LOW level at pin PWD will enable Power-on mode again. When pin PWD is left open-circuit, a pull-down resistor will keep this input LOW.

In the Power-down mode (set via the serial bus or through pin PWD) the current consumption becomes virtually zero. The serial bus is still available.

QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Supplies						
V_{DDA1}	analog supply voltage 1		3.6	–	7	V
V_{DDA2}	analog supply voltage 2		3.6	–	7	V
V_{DDD}	digital supply voltage		2.6	–	3.6	V
Vertical line drivers						
$R_{o(on)}$	HIGH- and LOW-level output on-resistance	$I_{L(H)}$ = 200 mA; $I_{L(L)}$ = –200 mA	–	0.66	–	Ω
Shutter driver						
$R_{o(on)}$	HIGH- and LOW-level output on-resistance	$I_{L(H)}$ = 3 mA; $I_{L(L)}$ = –3 mA	–	16.5	–	Ω
Output voltage regulators						
V_{HFB}	high output voltage	programmable	8	–	15	V
V_{NS}	Nwell substrate output voltage	programmable	17	–	31	V
V_{SFD}	source follower drain output voltage	programmable	18	–	24	V
V_{SH}	shutter driver output voltage	programmable	3	–	10	V
Temperature range						
T_{oper}	operating temperature		–20	–	+70	°C

ORDERING INFORMATION

TYPE NUMBER	PACKAGE		
	NAME	DESCRIPTION	VERSION
TDA9991HL	LQFP48	plastic low profile quad flat package; 48 leads; body 7 × 7 × 1.4 mm	SOT313-2

BLOCK DIAGRAM

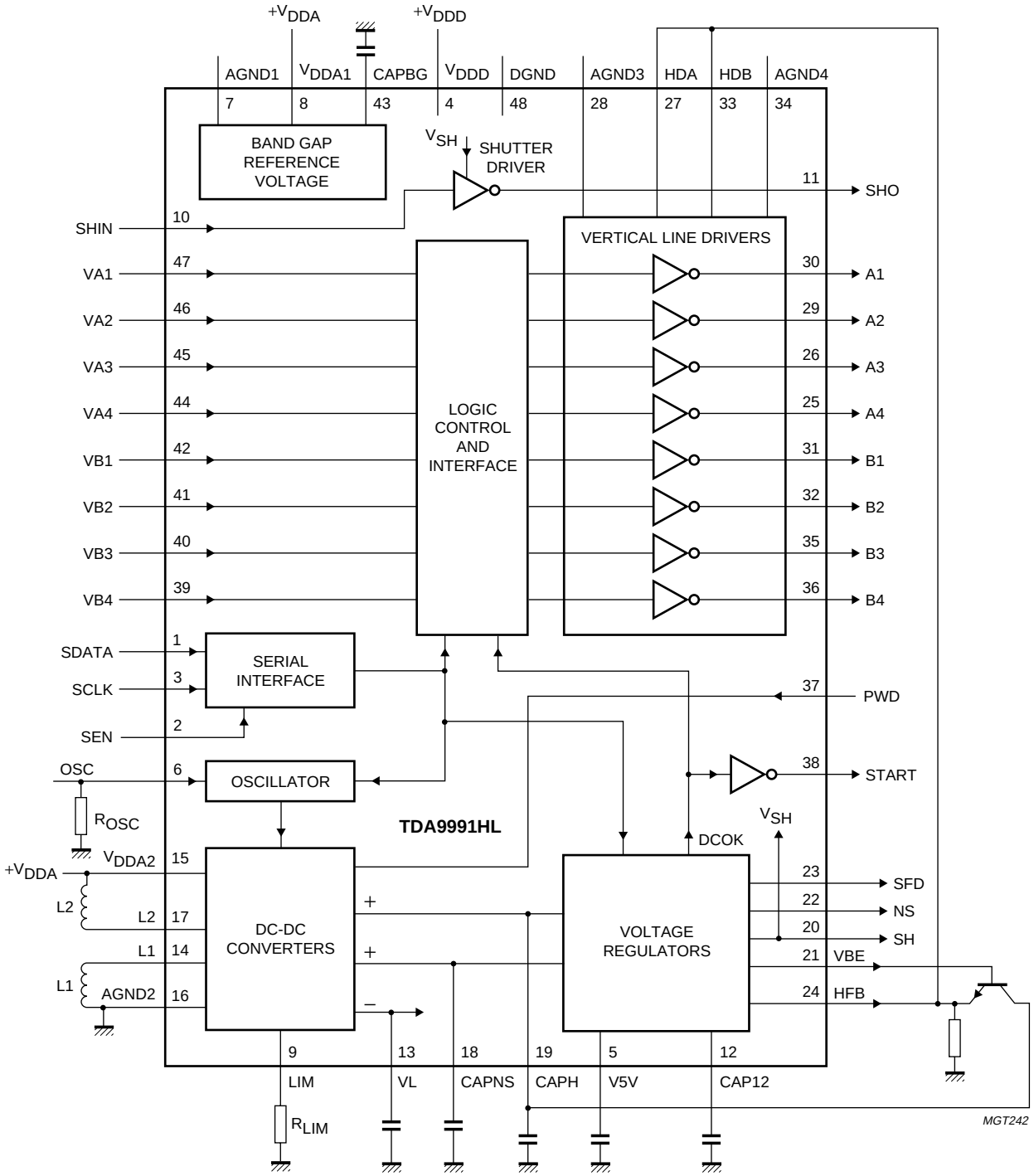


Fig.1 Block diagram.

PINNING

SYMBOL	PIN	DESCRIPTION
SDATA	1	serial bus data input
SEN	2	serial bus enable input
SCLK	3	serial bus clock input
V_{DDD}	4	digital supply voltage
V5V	5	filter capacitor of digital supply voltage
OSC	6	external oscillator resistor or clock input
AGND1	7	analog ground 1
V_{DDA1}	8	analog supply voltage 1
LIM	9	peak current limiting resistor
SHIN	10	electronic shutter driver input
SHO	11	electronic shutter driver output
CAP12	12	filter capacitor of DC-DC converter
VL	13	DC-DC converter negative low voltage
L1	14	coil 1 connection
V_{DDA2}	15	DC-DC converter analog supply voltage 2
AGND2	16	DC-DC converter analog ground 2
L2	17	coil 2 connection
CAPNS	18	filter capacitor of DC-DC converter CAPNS voltage
CAPH	19	filter capacitor of DC-DC converter CAPH voltage output
SH	20	shutter voltage output
VBE	21	base voltage output
NS	22	Nwell substrate voltage output
SFD	23	source follower drain voltage output
HFB	24	horizontal voltage feedback output
A4	25	A4 driver output
A3	26	A3 driver output
HDA	27	A drivers high voltage supply
AGND3	28	A drivers analog ground 3
A2	29	A2 driver output
A1	30	A1 driver output
B1	31	B1 driver output
B2	32	B2 driver output
HDB	33	B drivers high voltage supply
AGND4	34	B drivers analog ground 4
B3	35	B3 driver output
B4	36	B4 driver output
PWD	37	power-down input
START	38	DC voltages ready output
VB4	39	B4 driver digital input
VB3	40	B3 driver digital input
VB2	41	B2 driver digital input
VB1	42	B1 driver digital input
CAPBG	43	filter capacitor of band gap reference
VA4	44	A4 driver digital input
VA3	45	A3 driver digital input
VA2	46	A2 driver digital input
VA1	47	A1 driver digital input
DGND	48	digital ground

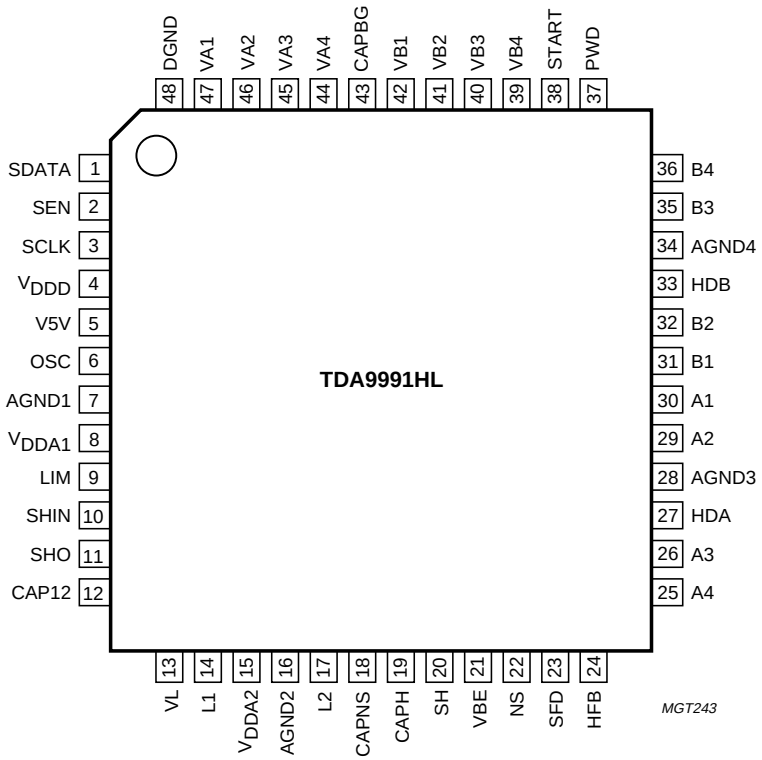


Fig.2 Pin configuration.

FUNCTIONAL DESCRIPTION

The TDA9991HL can be separated into three main blocks (see Fig.1):

- DC-DC converters
- Voltage regulators
- Drivers.

The functionality of the blocks is described below.

DC-DC converters

The principle of the DC-DC converter with positive output voltages V_{CAPNS} and V_{CAPH} is shown in Fig.3. The two voltages are generated by charging coil L2 (closing S1) and then discharging the charge built-up in coil L2 (by opening S1) into the capacitor at pin CAPNS or, when S2 is closed, into the capacitor at pin CAPH. Since V_{CAPNS} is always higher than V_{CAPH}, closing S2 will not cause a discharge of the capacitor at pin CAPNS into the capacitor at pin CAPH.

The current through switch S1 is being monitored and will not exceed the maximum value set by an external resistor at pin LIM. Limiting the maximum current will make the charge built-up in coil L2 independent of the supply voltage therefore keeping the converter efficiency constant.

The principle of the DC-DC converter with the negative output voltage V_{VL} is shown in Fig.4. The negative voltage is generated by charging coil L1 (closing S3) and then discharging the charge built-up in coil L1 (by opening S3) into the capacitor at pin VL. The capacitor at pin VL will be charged to approximately –3 V; there is no current limiting.

Voltage regulators

For an optimal performance of the CCD, the sensor voltages V_{SH}, V_{NS}, V_{SFD} and V_{HFB} are being generated by programmable voltage regulators with a very high ripple rejection.

The voltage regulators for V_{SH}, V_{NS} and V_{SFD} all have the same principle shown in Fig.5.

Peak currents are being supplied by the capacitor at the output while the voltage regulator charges the capacitor more slowly. The value of the capacitor determines the output voltage drop when a peak current is being drawn.

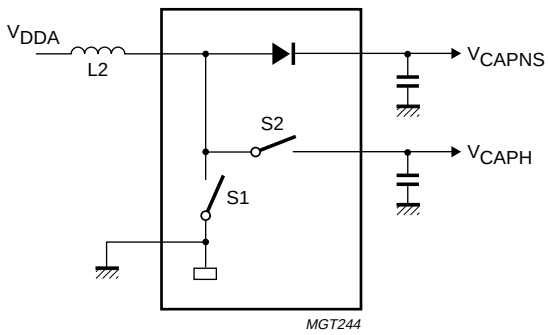


Fig.3 Principle of DC-DC converter with positive output voltage.

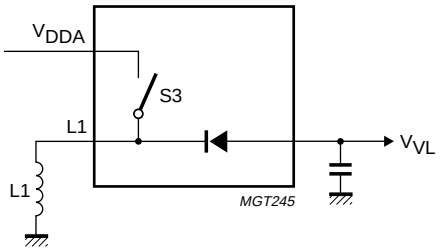


Fig.4 Principle of DC-DC converter with negative output voltage.

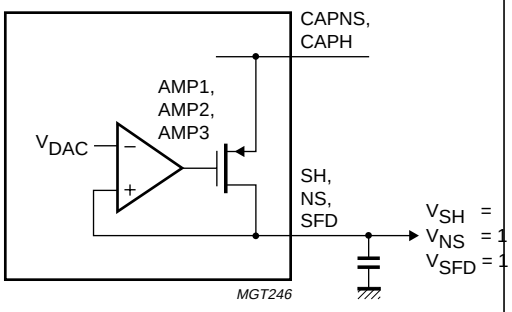


Fig.5 Principle of voltage regulators.

The voltage regulator for the drivers supply (V_{HFB}) can operate in two modes, depending on the application it is used in:

- Mode 1 at fast transport with high peak current
- Mode 2 at slow transport with constant current.

MODE 1

In applications where the transport of the image is done in a very short period large currents (up to 1.5 A) are being drawn which cannot be supplied by the voltage regulator itself. In that event an external transistor is used to supply the large peak currents (see Fig.6). Mode 1 is selected via the serial interface (Latch 1, bit D1 = 0; see Table 3).

In mode 1 the external transistor can supply large peak currents which are being drawn from the capacitor used at pin CAPH. Since V_{CAPH} is chosen to be 2.6 or 5.15 V (programmable via the serial bus with bit VD2X) above V_{HFB} the voltage at the capacitor at pin CAPH can drop approximately 1.8 or 4.5 V during the transport without affecting V_{HFB}. This reduces the value (size) of the capacitor required at pin CAPH. During the transport the base-emitter voltage of the external transistor will increase causing a drop on V_{HFB}. The drop depends on the static current set by R1 and the maximum peak current being drawn and can be calculated with the following formula:

$$V_{drop} = 25\ mV \times Ln\frac{I_{peak}}{I_{R1}}$$

The static current should be approximately 500 μA. Capacitor C2, connected to the emitter, filters out the spikes averaging the peak current. When the peak current stops, the increased base-emitter voltage will drop back to its normal level (see Fig.7).

The base voltage V_{VBE} might have been changed slightly (tens of millivolts) but will get back to its desired level fast. After transport the capacitor at pin CAPH will be charged again by the DC-DC converter.

MODE 2

In applications where the transport of the image is slow, a constant current is required which can be supplied by the voltage regulator and no external transistor is needed. Mode 2 is selected via the serial interface (bit D1 = 1).

In mode 2, pins VBE and HFB must be tied together (see Fig.8).

In this mode the voltage regulator can supply currents up to 30 mA. Peak currents need to be filtered out by capacitor C1.

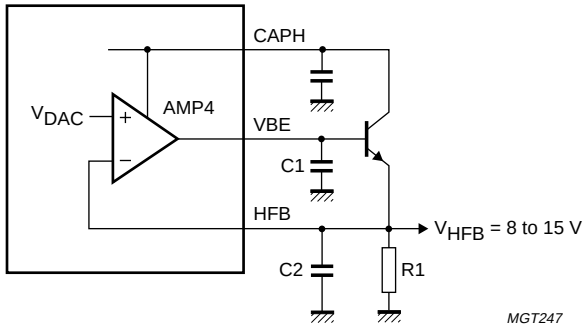


Fig.6 Principle of voltage regulator of drivers supply in mode 1.

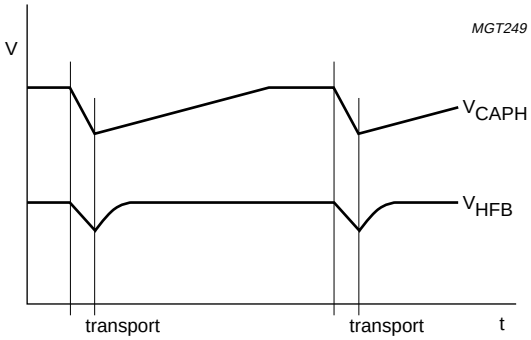


Fig.7 Output voltage at pin CAPH during transport.

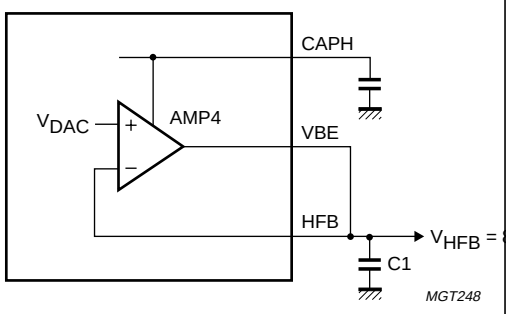


Fig.8 Principle of voltage regulator of drivers supply in mode 2.

START-UP CYCLE

During the start-up (pin START = HIGH and the internal signal DCOK = LOW) the maximum output current of AMP4 (see Fig.8) will be increased from 0.5 mA minimum to 30 mA maximum. This is done to decrease the time required to fully charge capacitor C1 during starting up.

When pin START = LOW (all voltages are at their required level) or when V_{VBE} is at its required level, the minimum output current of AMP4 will automatically drop back to 0.5 mA. When mode 2 is selected the maximum output current of AMP4 will remain 30 mA after starting up.

An integrated start-up cycle ensures a fast and safe start-up of the TDA9991HL. The principle of the start-up cycle (hysteresis) is shown in Fig.9. When starting up the signal at pin START will be HIGH. When V_{CAPNS} and V_{CAPH} are at 100% of their programmed level and V_{HFB} and V_{NS} are above 80% of their programmed level, pin START will become LOW. When V_{CAPNS}, V_{HFB} or V_{NS} drops below approximately 80% of their programmed level the TDA9991HL will start again with the start-up cycle.

When starting up, the capacitor at pin CAPNS will be charged prior to the capacitor at pin CAPH. The capacitor at pin VL is charged by a separate DC-DC converter independent of the start-up cycle.

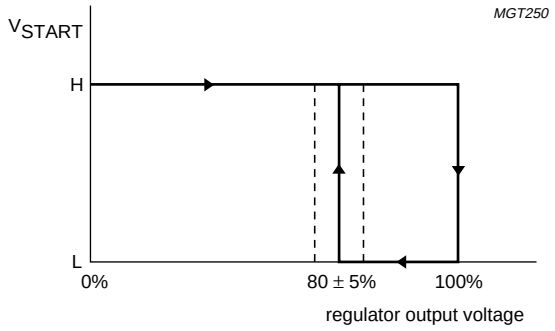


Fig.9 Hysteresis of start-up cycle.

Vertical line drivers

For frame transport the TDA9991HL has eight two-level low-ohmic drivers available. The principle of the driver outputs is shown in Fig.10.

A logic interface converts the digital input signal into the two control signals for the driver transistors. It also prevents both transistors to switch on at the same time. During start-up the drivers are kept in 3-state.

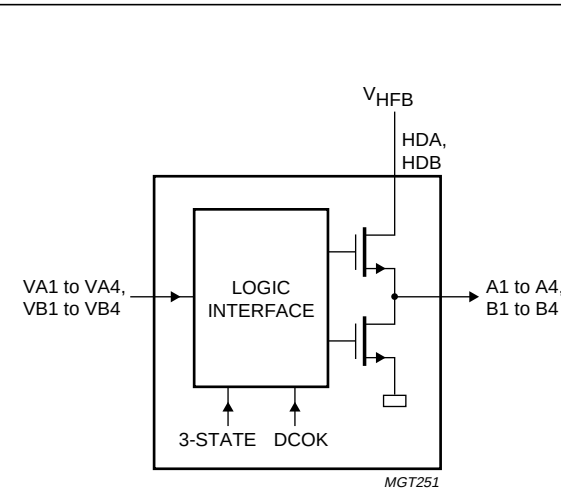


Fig.10 Principle of driver output.

Table 1 A and B drivers; note 1

LEVEL AT INPUT PINS	LEVEL AT OUTPUT PINS
LOW	HIGH
HIGH	LOW

Note

1. The internal DCOK signal will keep the A and B outputs in 3-state until the output voltages of the DC-DC converter and voltage regulators are at their required level.

Shutter driver

Table 2 Shutter driver output

INPUT LEVEL AT PIN SHIN	OUTPUT LEVEL AT PIN SHO
LOW	HIGH
HIGH	LOW

Serial interface

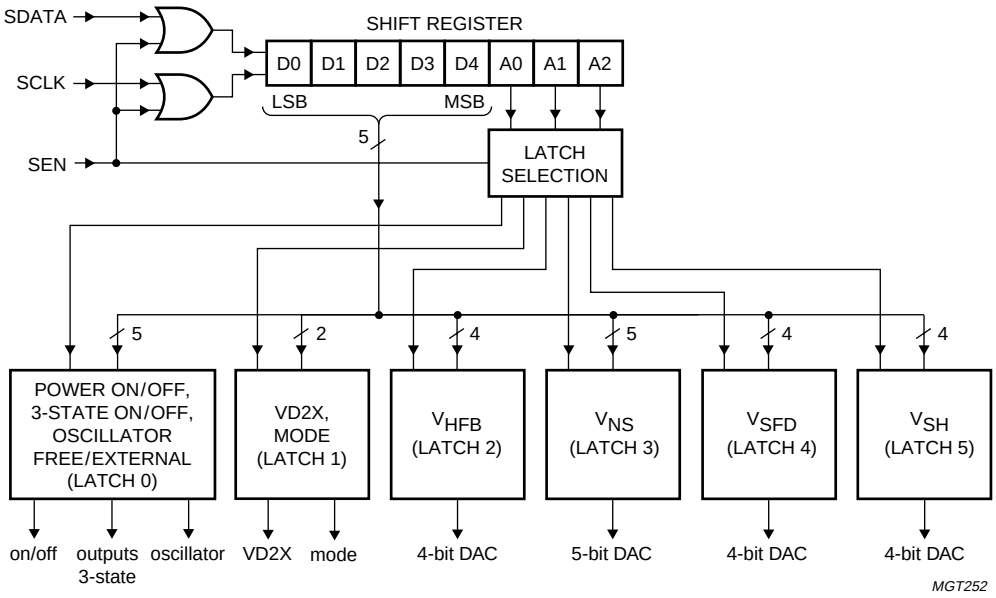
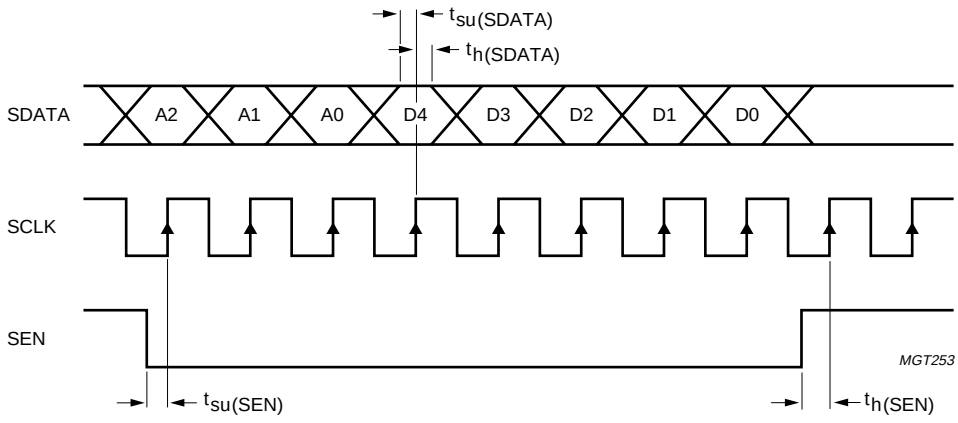


Fig.11 Serial interface block diagram.



Pin SEN must stay HIGH for at least two clock cycles after each word.

Fig.12 Loading sequence of input data to control DACs via the serial interface.

Table 3 Serial interface programming (see Fig.11)

LATCH	ADDRESS BITS			DATA BITS[1]					DESCRIPTION
	A2	A1	A0	D4	D3	D2	D1	D0	
0	0	0	0						power-on, 3-state and clock selection
								0	power-down (note 2)
								1	power-on
							0		outputs in normal operation
							1		outputs in 3-state
						X			don't care
					0				free running oscillator
					1				external clock signal
				0					fixed value
1	0	0	1						voltage drop and mode selection
								0	2.7 V drop (bit VD2X = 0)
								1	5.4 V drop (bit VD2X = 1)
							0		mode 1
							1		mode 2
2	0	1	0						4 bits of V_{HFB}
				X	0	0	0	0	output is 8 V
				X	:	:	:	:	steps of approximately 467 mV
				X	1	1	1	1	output is 15 V
3	0	1	1						5 bits of V_{NS}
				0	0	0	0	0	output is 17 V
				:	:	:	:	:	steps of approximately 450 mV
				1	1	1	1	1	output is 31 V
4	1	0	0						4 bits of V_{SFD}
				X	0	0	0	0	output is 18 V
				X	:	:	:	:	steps of approximately 400 mV
				X	1	1	1	1	output is 24 V
5	1	0	1						4 bits of V_{SH}
				X	0	0	0	0	output is 3 V
				X	:	:	:	:	steps of approximately 467 mV
				X	1	1	1	1	output is 10 V

Notes

1. X is a don't care.
2. The Power-down mode also shuts down the DC-DC converter.

LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 60134).

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{DDA1}	analog supply voltage 1		–0.3	+7	V
V_{DDA2}	analog supply voltage 2		–0.3	+7	V
V_{DDD}	digital supply voltage		–0.3	+5.5	V
V_n	voltage at pins				
	VA1 to VA4, VB1 to VB4, V5V, PWD, SDATA, SEN, SCLK, SHIN and OSC		–0.3	V_{DDD} + 0.3[1]	V
	CAPBG		–0.3	V_{V5V} + 0.3	V
	CAP12		–0.3	+15	V
	VBE, SH, HFB, HDA and HDB		–0.3	+20	V
	CAPH	coil not connected	–0.3	+20	V
	CAPNS	coil not connected	–0.3	+45	V
	NS and SFD		–0.3	+45	V
	VL		–6	–	V
	AGND1, AGND2, AGND3 and AGND4		V_{DGND} – 0.3	V_{DGND} + 0.3	V
I_n	current at pins				
	A1 to A4 and B1 to B4	static current	–100	+100	mA
	VL		0	5	mA
	LIM		–3	0	mA
	SHO		–50	+50	mA
	START		–3	+0.2	mA

Note

1. Maximum value of V_{DDD} + 0.3 V but not higher than 5.5 V.

QUALITY SPECIFICATION

In accordance with *“SNW-FQ-611E”*.

CHARACTERISTICS

V_{DDA} = 5 V; V_{DDD} = 3.3 V; T_{amb} = 25 °C; inputs VA1 to VA4 and VB1 to VB4 are HIGH; V_{SHIN} = 0 V; L1 = 47 µH; L2 = 4.7 µH; R_{LIM} = 680 Ω; V_{HFB} = 12 V; V_{NS} = 24 V; V_{SFD} = 20 V; V_{SH} = 8 V; V_{START} = LOW; no load for regulator output voltages; unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Supplies						
V_{DDA1}	analog supply voltage 1		3.6	5	7	V
I_{DDA1}	analog supply current 1	V_{VA1} to V_{VA4} = V_{DDD}; V_{VB1} to V_{VB4} = V_{DDD}; V_{SEN} = 0	–	3.5	–	mA
$I_{q(DDA1)}$	quiescent analog supply current 1	Power-down mode; latch 0 = 00X00; note 1	–	–	300	µA
V_{DDA2}	analog supply voltage 2		3.6	5	7	V

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
I_{DDA2}	analog supply current 2	V_{VA1} to V_{VA4} = V_{DDD}; V_{VB1} to V_{VB4} = V_{DDD}; V_{SEN} = 0; note 2	–	130	–	mA
$I_{q(DDA2)}$	quiescent analog supply current 2	Power-down mode; latch 0 = 00X00; note 1	–	–	4	µA
V_{DDD}	digital supply voltage		2.6	3.3	3.6	V
I_{DDD}	digital supply current	V_{VA1} to V_{VA4} = V_{DDD}; V_{VB1} to V_{VB4} = V_{DDD}; V_{SEN} = 0	–	460	–	µA
$I_{q(DDD)}$	quiescent digital supply current	Power-down mode; latch 0 = 00X00; note 1	–	–	100	µA
Vertical line drivers A and B						
$R_{o(on)}$	HIGH- and LOW-level output on-resistance	$I_{L(H)}$ = 200 mA; $I_{L(L)}$ = –200 mA	0.6	0.66	0.72	Ω
t_r	rise time of outputs	V_{NS} – V_{HFB} > 7 V; C_L = 6.8 nF	16	20	29	ns
t_f	fall time of outputs	V_{NS} – V_{HFB} > 7 V; C_L = 6.8 nF	18	23	29	ns
V_{OH}	HIGH-level output voltage		–	V_{HFB}	–	V
V_{OL}	LOW-level output voltage		–	0	–	V
$I_{LO(Z)}$	output leakage current in 3-state	3-state; V_O < 6 V; latch 0 = 00X11	–1	–	+1	µA
t_{PD}	propagation delay	no load		40		ns
Δt_{PD}	propagation delay difference between channels		–	–	3	ns
Shutter driver (pin SHO)						
$R_{o(on)}$	HIGH- and LOW-level output on-resistance	$I_{L(H)}$ = 3 mA; $I_{L(L)}$ = –3 mA	–	16.5	–	Ω
V_{OH}	HIGH-level output voltage		–	V_{SH}	–	V
V_{OL}	LOW-level output voltage		–	0	–	V
t_r	rise time	V_{NS} – V_{SH} > 7 V; C_L = 2 nF	–	50		ns
t_f	fall time	V_{NS} – V_{SH} > 7 V; C_L = 2 nF	–	50		ns
DC-DC converters						
V_{CAPNS}	output voltage at pin CAPNS		–	V_{NS} + 6	–	V
V_{CAPH}	output voltage at pin CAPH	bit VD2X = 0; note 3	V_{HFB} + 2.45	V_{HFB} + 2.6	V_{HFB} + 2.75	V
		bit VD2X = 1; note 3	V_{HFB} + 4.9	V_{HFB} + 5.15	V_{HFB} + 5.4	V
$\Delta I_{L2(max)}$	variation of maximum current built-up in coil L2	note 4	–15	–	+15	%
t_{start}	start-up time of the DC-DC converter	V_{START} = HIGH; R_{LIM} = 680 Ω; V_{HFB} = 13.1 V; note 5	–	35	60	ms

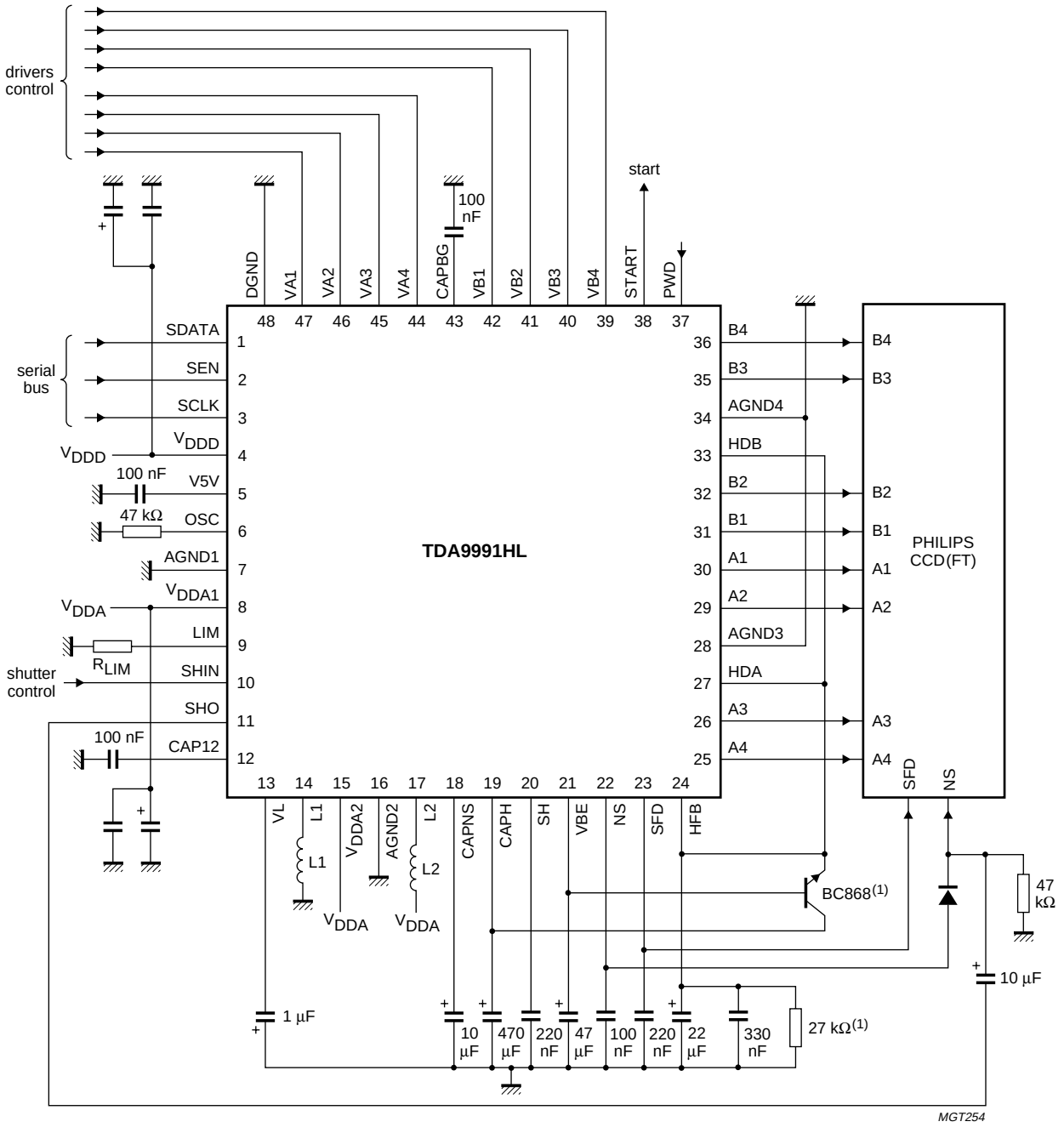
SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Output voltage regulators						
HIGH VOLTAGE FEEDBACK OUTPUT (PIN HFB)						
V_{HFB}	high voltage output	programmable (4 bits)	8	–	15	V
ΔV_{HFB}	output voltage variation		–5	0	+5	%
$\Delta V_{HFB(T)}$	output voltage variation with temperature	T_{amb} = –20 to +70 °C	–	–	0.5	%
RR	ripple rejection	V_{START} = LOW; f = 0 to 1 MHz; note 6	60	–	–	dB
BASE VOLTAGE OUTPUT (PIN VBE)						
I_{VBE}	DC output current	V_{START} = LOW; note 7	0.5	–	–	mA
$I_{VBE(start)}$	output current during start-up	V_{START} = HIGH or in mode 2; note 7	30	–	–	mA
NWELL SUBSTRATE VOLTAGE OUTPUT (PIN NS)						
V_{NS}	output voltage	programmable (5 bits); note 8	17	–	31	V
I_{NS}	DC output current		–	–	4	mA
ΔV_{NS}	output voltage variation		–5	0	+5	%
$\Delta V_{NS(T)}$	output voltage variation with temperature	T_{amb} = –20 to +70 °C	–	–	0.5	%
RR	ripple rejection	V_{START} = LOW; f = 0 to 1 MHz; note 6	50	–	–	dB
SOURCE FOLLOWER DRAIN VOLTAGE OUTPUT (PIN SFD)						
V_{SFD}	output voltage	programmable (4 bits); note 8	18	–	24	V
I_{SFD}	DC output current		–	–	20	mA
ΔV_{SFD}	output voltage variation		–5	0	+5	%
$\Delta V_{SFD(T)}$	output voltage variation with temperature	T_{amb} = –20 to +70 °C	–	–	0.5	%
RR	ripple rejection	V_{START} = LOW; f = 0 to 1 MHz; note 6	50	–	–	dB
SHUTTER DRIVER VOLTAGE OUTPUT (PIN SH)						
V_{SH}	output voltage	programmable (4 bits)	3	–	10	V
I_{SH}	DC output current		–	–	3	mA
ΔV_{SH}	output voltage variation		–5	0	+5	%
$\Delta V_{SH(T)}$	output voltage variation with temperature	T_{amb} = –20 to +70 °C	–	–	0.5	%
RR	ripple rejection	V_{START} = LOW; f = 0 to 1 MHz; note 6	60	–	–	dB

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Oscillator						
f_{fr}	free running oscillator frequency	latch 0 = 00X01; R_{OSC} = 47 kΩ; note 9	4	5.35	6.75	MHz
f_{clk}	external clock input frequency	latch 0 = 01X01; note 9	4	–	6.75	MHz
δ	duty factor external clock input frequency		40	–	60	%
Serial interface (see Fig.12)						
$f_{SCLK(max)}$	maximum clock frequency	V_{DDD} = 3.6V	–	–	4.0	MHz
		V_{DDD} = 3.3V	–	–	3.3	MHz
		V_{DDD} = 3.0V	–	–	2.5	MHz
		V_{DDD} = 2.6V	–	–	1.8	MHz
$t_{su(SEN)}$	SEN set-up time	compared to SCLK rising edge	$\frac{0.16}{f_{SCLK(max)}}$	–	–	s
$t_{su(SDATA)}$	SDATA set-up time	compared to SCLK rising edge	$\frac{0.16}{f_{SCLK(max)}}$	–	–	s
$t_{h(SEN)}$	SEN hold time	compared to SCLK rising edge	$\frac{0.08}{f_{SCLK(max)}}$	–	–	s
$t_{h(SDATA)}$	SDATA hold time	compared to SCLK rising edge	$\frac{0.16}{f_{SCLK(max)}}$	–	–	s
Control inputs						
V_{IL}	LOW-level input voltage at pins SEN, SDATA, SCLK, SHIN, PWD, VA1 to VA4, VB1 to VB4 and OSC	note 10	–0.2	–	$0.3V_{DDD}$	V
V_{IH}	HIGH-level input voltage at pins SEN, SDATA, SCLK, SHIN, PWD, VA1 to VA4, VB1 to VB4 and OSC	note 11	$0.7V_{DDD}$	–	5.5	V
Digital output (pin START)						
$V_{START(L)}$	LOW-level output voltage	$I_{sink(max)}$ = 20 μA; note 12	–	–	0.4	V
$V_{START(H)}$	HIGH-level output voltage	$I_{source(max)}$ = 20 μA; note 13	V_{DDD} − 0.4	–	–	V
Temperature range						
T_{oper}	operating temperature		–20	–	+70	°C

Notes

1. A Power-on reset function puts the TDA9991HL in the Power-down mode when V_{DDD} is supplied.
2. The supply current is measured without load (CCD) using the following programmed voltages: V_{NS} = 28 V; V_{SFD} = 21 V; V_{HFB} = 13 V; V_{SH} = 8 V. The power consumption depends on the value of R_{LIM}, the supply voltages, programmed voltages and the efficiency of the DC-DC convertor under load condition. Therefore, the value of I_{DDA2} in this table is a rough indication.
3. During transport V_{CAPH} may drop to V_{HFB} + 0.7 V (over the entire temperature range):
   a) Bit VDX2 = 0: voltage drop is 1.8 V
   b) Bit VDX2 = 1: voltage drop is 4.5 V.
4. $I_{L2(max)} = \frac{1308}{R_{LIM}}$
5. The charging time of the electrolytic capacitor at pin CAPNS is very small compared to the charging time of the electrolytic capacitor at pin CAPH. The start-up time depends on:
   a) Peak current $I_{L2(max)}$ chosen through coil L2; the maximum allowable peak current is 2.1 A
   b) Value of the electrolytic capacitor at pin CAPH (470 μF)
   c) Oscillator frequency
   d) Required voltage level at pin CAPH.
6. Drivers not active.
7. During start-up (V_{START} = HIGH) the maximum output current at pin HFB is increased to allow fast starting up.
8. $V_{NS} > V_{SFD}$.
9. Pin OSC can be connected to an external clock or to an external resistor (in case the internal oscillator is used).
10. At V_{DDD} = 2.6 V the maximum LOW-level voltage is $0.2V_{DDD}$.
11. At V_{DDD} = 2.6 V the minimum HIGH-level voltage is $0.8V_{DDD}$.
12. V_{START} will become LOW when:
    a) All output voltages at pins HFB, NS and CAPNS are at 100% of their required (programmable) level
    b) $V_{CAPH} = V_{HFB}$ + 2.7 V (bit VD2X = 0) or $V_{CAPH} = V_{HFB}$ + 5.4 V (bit VD2X = 1); V_{CAPH} needs to have reached the programmed voltage only once for V_{START} to go LOW.
13. V_{START} will become HIGH when either V_{HFB}, V_{NS} or V_{CAPNS} drops below 80% (typical) of their programmed level.

APPLICATION INFORMATION



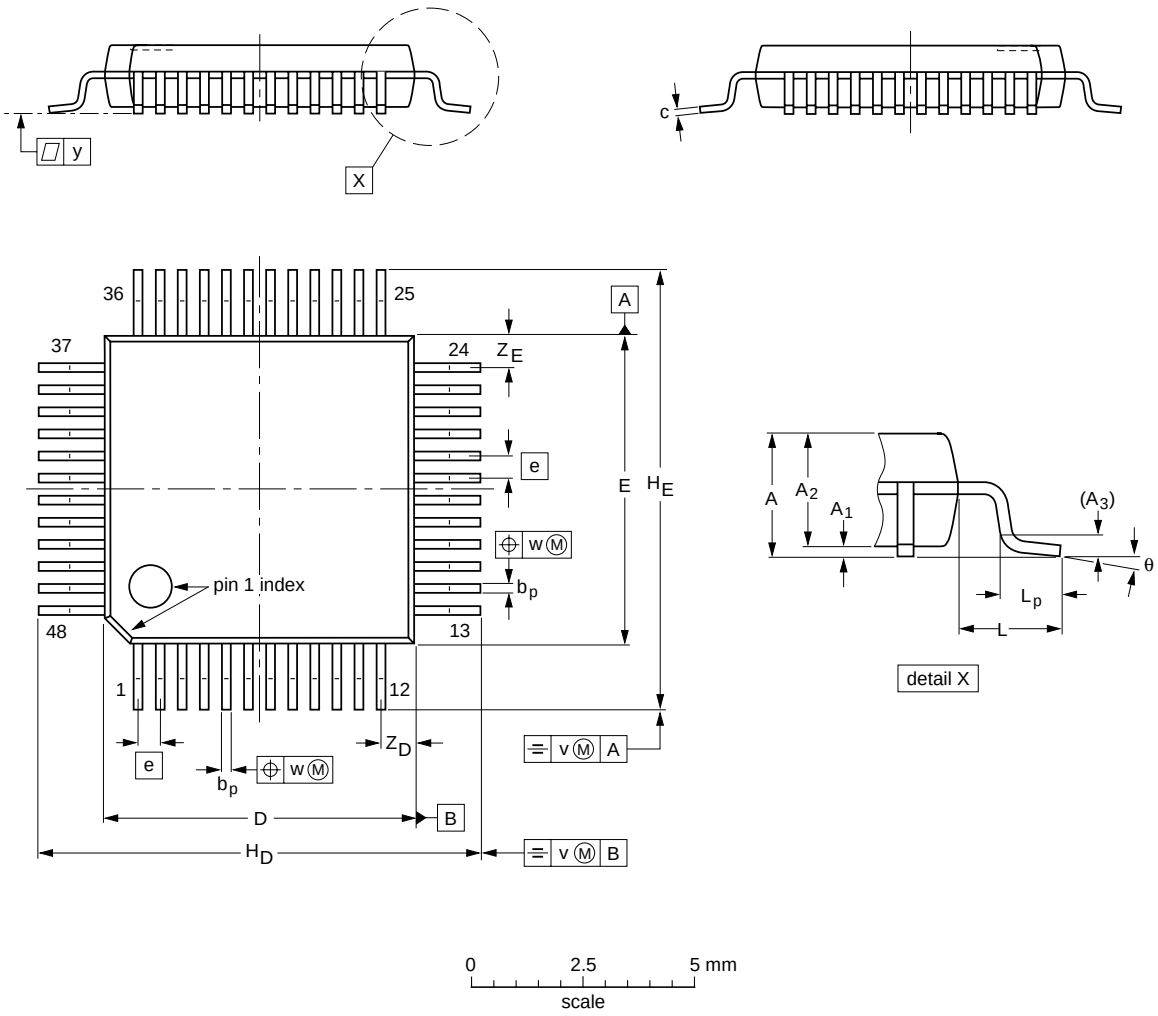
(1) The (emitter) current through the external resistor should be approximately 500 µA. The value of the resistor can be adjusted depending on the emitter voltage (V_{HFB}).

L1 = 47 µH.
L2 = 4.7 µH.
R_{LIM} = 680 Ω.

Fig.13 Application diagram.

PACKAGE OUTLINE

LQFP48: plastic low profile quad flat package; 48 leads; body 7 x 7 x 1.4 mm **SOT313-2**



DIMENSIONS (mm are the original dimensions)

UNIT	A max.	A_1	A_2	A_3	b_p	c	$D^{(1)}$	$E^{(1)}$	e	H_D	H_E	L	L_p	v	w	y	$Z_D^{(1)}$	$Z_E^{(1)}$	θ
mm	1.60	0.20 0.05	1.45 1.35	0.25	0.27 0.17	0.18 0.12	7.1 6.9	7.1 6.9	0.5	9.15 8.85	9.15 8.85	1.0	0.75 0.45	0.2	0.12	0.1	0.95 0.55	0.95 0.55	7^o 0^o

Note

1. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT313-2	136E05	MS-026				~~99-12-27~~ 00-01-19

SOLDERING

Introduction to soldering surface mount packages

This text gives a very brief insight to a complex technology. A more in-depth account of soldering ICs can be found in our *"Data Handbook IC26; Integrated Circuit Packages"* (document order number 9398 652 90011).

There is no soldering method that is ideal for all surface mount IC packages. Wave soldering can still be used for certain surface mount ICs, but it is not suitable for fine pitch SMDs. In these situations reflow soldering is recommended.

Reflow soldering

Reflow soldering requires solder paste (a suspension of fine solder particles, flux and binding agent) to be applied to the printed-circuit board by screen printing, stencilling or pressure-syringe dispensing before package placement.

Several methods exist for reflowing; for example, convection or convection/infrared heating in a conveyor type oven. Throughput times (preheating, soldering and cooling) vary between 100 and 200 seconds depending on heating method.

Typical reflow peak temperatures range from 215 to 250 °C. The top-surface temperature of the packages should preferable be kept below 220 °C for thick/large packages, and below 235 °C for small/thin packages.

Wave soldering

Conventional single wave soldering is not recommended for surface mount devices (SMDs) or printed-circuit boards with a high component density, as solder bridging and non-wetting can present major problems.

To overcome these problems the double-wave soldering method was specifically developed.

If wave soldering is used the following conditions must be observed for optimal results:

- Use a double-wave soldering method comprising a turbulent wave with high upward pressure followed by a smooth laminar wave.
- For packages with leads on two sides and a pitch (e):
  - larger than or equal to 1.27 mm, the footprint longitudinal axis is **preferred** to be parallel to the transport direction of the printed-circuit board;
  - smaller than 1.27 mm, the footprint longitudinal axis **must** be parallel to the transport direction of the printed-circuit board.

  The footprint must incorporate solder thieves at the downstream end.
- For packages with leads on four sides, the footprint must be placed at a 45° angle to the transport direction of the printed-circuit board. The footprint must incorporate solder thieves downstream and at the side corners.

During placement and before soldering, the package must be fixed with a droplet of adhesive. The adhesive can be applied by screen printing, pin transfer or syringe dispensing. The package can be soldered after the adhesive is cured.

Typical dwell time is 4 seconds at 250 °C.
A mildly-activated flux will eliminate the need for removal of corrosive residues in most applications.

Manual soldering

Fix the component by first soldering two diagonally-opposite end leads. Use a low voltage (24 V or less) soldering iron applied to the flat part of the lead. Contact time must be limited to 10 seconds at up to 300 °C.

When using a dedicated tool, all other leads can be soldered in one operation within 2 to 5 seconds between 270 and 320 °C.

Suitability of surface mount IC packages for wave and reflow soldering methods

PACKAGE	SOLDERING METHOD	
	WAVE	REFLOW(1)
BGA, HBGA, LFBGA, SQFP, TFBGA	not suitable	suitable
HBCC, HLQFP, HSQFP, HSOP, HTQFP, HTSSOP, HVQFN, SMS	not suitable(2)	suitable
PLCC(3), SO, SOJ	suitable	suitable
LQFP, QFP, TQFP	not recommended(3)(4)	suitable
SSOP, TSSOP, VSO	not recommended(5)	suitable

Notes

1. All surface mount (SMD) packages are moisture sensitive. Depending upon the moisture content, the maximum temperature (with respect to time) and body size of the package, there is a risk that internal or external package cracks may occur due to vaporization of the moisture in them (the so called popcorn effect). For details, refer to the Drypack information in the *"Data Handbook IC26; Integrated Circuit Packages; Section: Packing Methods"*.
2. These packages are not suitable for wave soldering as a solder joint between the printed-circuit board and heatsink (at bottom version) can not be achieved, and as solder may stick to the heatsink (on top version).
3. If wave soldering is considered, then the package must be placed at a 45° angle to the solder wave direction. The package footprint must incorporate solder thieves downstream and at the side corners.
4. Wave soldering is only suitable for LQFP, TQFP and QFP packages with a pitch (e) equal to or larger than 0.8 mm; it is definitely not suitable for packages with a pitch (e) equal to or smaller than 0.65 mm.
5. Wave soldering is only suitable for SSOP and TSSOP packages with a pitch (e) equal to or larger than 0.65 mm; it is definitely not suitable for packages with a pitch (e) equal to or smaller than 0.5 mm.

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