CY14B256P

256-Kbit (32 K × 8) Serial (SPI) nvSRAM with Real Time Clock

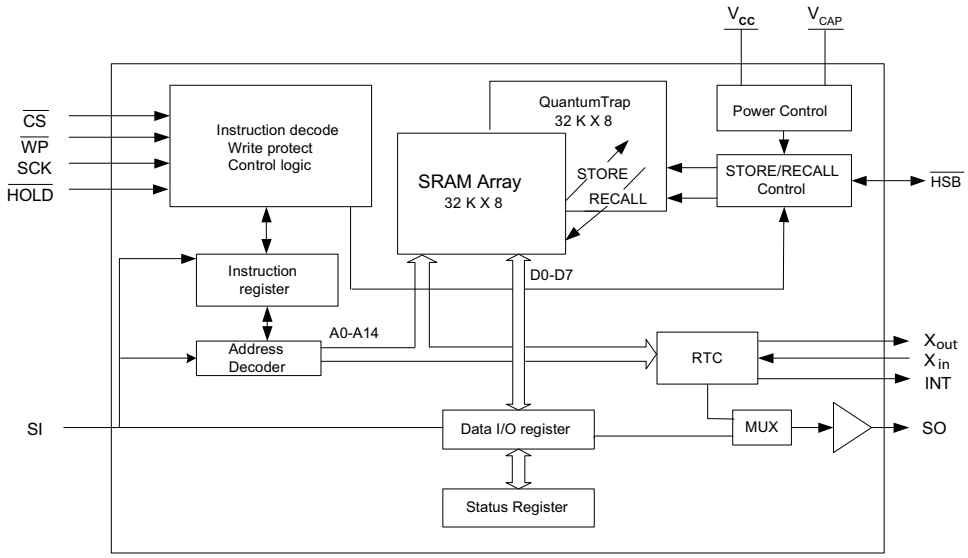
Features

- 256-Kbit nonvolatile static random access memory (nvSRAM)
  - Internally organized as 32 K × 8
  - STORE to QuantumTrap nonvolatile elements initiated automatically on power-down (AutoStore) or by user using $\overline{\text{HSB}}$ pin (Hardware STORE) or SPI instruction (Software STORE)
  - RECALL to SRAM initiated on power-up (Power-Up RECALL) or by SPI instruction (Software RECALL)
  - Automatic STORE on power-down with a small capacitor
- High reliability
  - Infinite read, write, and RECALL cycles
  - 1 million STORE cycles to QuantumTrap
  - Data retention: 20 years
- Real time clock (RTC)
  - Full-featured RTC
  - Watchdog timer
  - Clock alarm with programmable interrupts
  - Capacitor or battery backup for RTC
  - Backup current of 0.35 µA (typical)
- High-speed serial peripheral interface (SPI)
  - 40-MHz clock rate – SRAM memory access
  - 25-MHz clock rate – RTC memory access
  - Supports SPI mode 0 (0,0) and mode 3 (1,1)
- Write protection
  - Hardware protection using Write Protect ($\overline{\text{WP}}$) pin
  - Software protection using Write Disable instruction
  - Software block protection for 1/4, 1/2, or entire array
- Low power consumption
  - Single 3 V +20%, –10% operation
  - Average active current of 10 mA at 40 MHz operation
- Industry standard configurations
  - Industrial temperature
  - 16-pin small outline integrated circuit (SOIC) package
  - Restriction of hazardous substances (RoHS) compliant

Overview

The Cypress CY14B256P combines a 256-Kbit nvSRAM[1] with a full-featured real time clock in a monolithic integrated circuit with serial SPI interface. The memory is organized as 32 K words of 8 bits each. The embedded nonvolatile elements incorporate the QuantumTrap technology, creating the world's most reliable nonvolatile memory. The SRAM provides infinite read and write cycles, while the QuantumTrap cells provide highly reliable nonvolatile storage of data. Data transfers from SRAM to the nonvolatile elements (STORE operation) takes place automatically at power-down. On power-up, data is restored to the SRAM from the nonvolatile memory (RECALL operation). The STORE and RECALL operations can also be initiated by the user through SPI instruction.

Logic Block Diagram



Note
1. This device will be referred to as nvSRAM throughout the document.

Contents

Pinouts

Figure 1. Pin Diagram – 16-pin SOIC

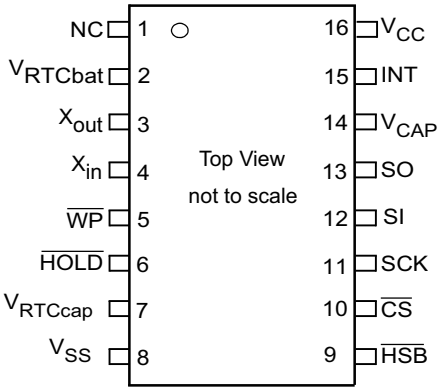


Table 1. Pin Definitions

Pin Name	I/O Type	Description
$\overline{CS}$	Input	Chip select. Activates the device when pulled LOW. Driving this pin HIGH puts the device in low power standby mode.
SCK	Input	Serial clock. Runs at speeds up to maximum of f_{SCK}. Serial input is latched at the rising edge of this clock. Serial output is driven at the falling edge of the clock.
SI	Input	Serial input. Pin for input of all SPI instructions and data.
SO	Output	Serial output. Pin for output of data through SPI.
$\overline{WP}$	Input	Write protect. Implements hardware write protection in SPI.
$\overline{HOLD}$	Input	$\overline{HOLD}$ pin. Suspends serial operation.
$\overline{HSB}$	Input/output	Hardware STORE busy: Output: Indicates busy status of nvSRAM when LOW. After each hardware and software STORE operation HSB is driven HIGH for a short time (t_{HHHD}) with standard output high current and then a weak internal pull-up resistor keeps this pin HIGH (external pull-up resistor connection optional). Input: Hardware STORE implemented by pulling this pin LOW externally.
V_{CAP}	Power supply	AutoStore capacitor. Supplies power to the nvSRAM during power loss to STORE data from the SRAM to nonvolatile elements. If AutoStore is not needed, this pin must be left as No Connect. It must never be connected to ground.
V_{RTCcap}	Power supply	Capacitor backup for RTC. Left unconnected if V_{RTCbat} is used.
V_{RTCbat}	Power supply	Battery backup for RTC. Left unconnected if V_{RTCcap} is used.
Xout	Output	Crystal output connection. Drives crystal on start up.
Xin	Input	Crystal input connection. For 32.768 kHz crystal.
INT	Output	Interrupt output. Programmable to respond to the clock alarm, the watchdog timer, and the power monitor. Also programmable to either active HIGH (push or pull) or LOW (open drain).
NC	No connect	No connect. This pin is not connected to the die.
V_{SS}	Power supply	Ground
V_{CC}	Power supply	Power supply (2.7 V to 3.6 V)

Device Operation

CY14B256P is a 256-Kbit nvSRAM memory with integrated RTC and SPI interface. All the reads and writes to nvSRAM happen to the SRAM which gives nvSRAM the unique capability to handle infinite writes to the memory. The data in SRAM is secured by a STORE sequence that transfers the data in parallel to the nonvolatile QuantumTrap cells. A small capacitor (V_{CAP}) is used to AutoStore the SRAM data in nonvolatile cells when power goes down providing power-down data security. The QuantumTrap nonvolatile elements built in the reliable SONOS technology make nvSRAM the ideal choice for secure data storage.

In CY14B256P, the 256-Kbit memory array is organized as 32 K words × 8 bits. The memory is accessed through a standard SPI interface that enables very high clock speeds up to 40 MHz with zero cycle delay read and write cycles. CY14B256P supports SPI modes 0 and 3 (CPOL, CPHA = 0, 0 and 1, 1) and operates as SPI slave. The device is enabled using the chip select ($\overline{CS}$) pin and accessed through serial input (SI), serial output (SO), and serial clock (SCK) pins.

CY14B256P provides the feature for hardware and software write protection through the $\overline{WP}$ pin and WRDI instruction. CY14B256P also provides mechanisms for block write protection (quarter, half, or full array) using BP0 and BP1 pins in the Status Register. Further, the $\overline{HOLD}$ pin is used to suspend any serial communication without resetting the serial sequence.

CY14B256P uses the standard SPI opcodes for memory access. In addition to the general SPI instructions for read and write, CY14B256P provides four special instructions that allow access to four nvSRAM specific functions: STORE, RECALL, AutoStore Disable (ASDISB), and AutoStore Enable (ASENB).

The major benefit of nvSRAM over serial EEPROMs is that all reads and writes to nvSRAM are performed at the speed of SPI bus with zero cycle delay. Therefore, no wait time is required after any of the memory accesses. The STORE and RECALL operations need finite time to complete and all memory accesses are inhibited during this time. While a STORE or RECALL operation is in progress, the busy status of the device is indicated by the Hardware STORE Busy ($\overline{HSB}$) pin and also reflected on the $\overline{RDY}$ bit of the Status Register.

SRAM Write

All writes to nvSRAM are carried out on the SRAM and do not use up any endurance cycles of the nonvolatile memory. This enables the user to perform infinite write operations. A write cycle is performed through the WRITE instruction. The WRITE instruction is issued through the SI pin of the nvSRAM and consists of the WRITE opcode, two bytes of address, and one byte of data. Write to nvSRAM is done at SPI bus speed with zero cycle delay.

CY14B256P allows burst mode writes to be performed through SPI. This enables write operations on consecutive addresses without issuing a new WRITE instruction. When the last address in memory is reached in burst mode, the address rolls over to 0x0000 and the device continues to write.

The SPI write cycle sequence is defined in the Memory Access section of SPI Protocol Description.

SRAM Read

A read cycle in CY14B256P is performed at the SPI bus speed and the data is read out with zero cycle delay after the READ instruction is executed. The READ instruction is issued through the SI pin of the nvSRAM and consists of the READ opcode and two bytes of address. The data is read out on the SO pin.

CY14B256P allows burst mode reads to be performed through SPI. This enables reads on consecutive addresses without issuing a new READ instruction. When the last address in memory is reached in burst mode read, the address rolls over to 0x0000 and the device continues to read.

The SPI read cycle sequence is defined in the Memory Access section of SPI Protocol Description.

STORE Operation

STORE operation transfers the data from the SRAM to the nonvolatile QuantumTrap cells. The CY14B256P STOREs data to the nonvolatile cells using one of the three STORE operations: AutoStore, activated on device power-down; Software STORE, activated by a STORE instruction; and Hardware STORE, activated by the $\overline{HSB}$. During the STORE cycle, an erase of the previous nonvolatile data is first performed, followed by a program of the nonvolatile elements. After a STORE cycle is initiated, read/write to CY14B256P is inhibited until the cycle is completed.

The $\overline{HSB}$ signal or the $\overline{RDY}$ bit in the Status Register can be monitored by the system to detect if a STORE or Software RECALL cycle is in progress. The busy status of nvSRAM is indicated by $\overline{HSB}$ being pulled LOW or $\overline{RDY}$ bit being set to '1'. To avoid unnecessary nonvolatile STOREs, AutoStore and Hardware STORE operations are ignored unless at least one write operation has taken place since the most recent STORE or RECALL cycle. However, software initiated STORE cycles are performed regardless of whether a write operation has taken place.

AutoStore Operation

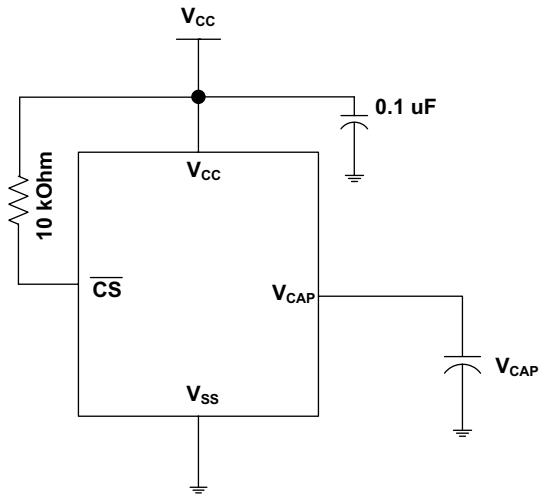
The AutoStore operation is a unique feature of nvSRAM which automatically stores the SRAM data to QuantumTrap cells during power-down. This STORE makes use of an external capacitor (V_{CAP}) and enables the device to safely STORE the data in the nonvolatile memory when power goes down.

During normal operation, the device draws current from V_{CC} to charge the capacitor connected to the V_{CAP} pin. When the voltage on the V_{CC} pin drops below V_{SWITCH} during power-down, the device inhibits all memory accesses to nvSRAM and automatically performs a conditional STORE operation using the charge from the V_{CAP} capacitor. The AutoStore operation is not initiated if no write cycle was performed since the last RECALL.

Note If a capacitor is not connected to V_{CAP} pin, AutoStore must be disabled by issuing the AutoStore Disable instruction specified in AutoStore Enable (ASENB) instruction on page 14. If AutoStore is enabled without a capacitor on V_{CAP} pin, the device attempts an AutoStore operation without sufficient charge to complete the store. This corrupts the data stored in the nvSRAM and Status Register. To resume normal functionality, the WRSR instruction must be issued to update the nonvolatile bits BP0, BP1 and WPEN in the Status Register.

Figure 2 shows the proper connection of the storage capacitor (V_{CAP}) for AutoStore operation. Refer to DC Electrical Characteristics on page 25 for the size of the V_{CAP}.

Figure 2. AutoStore Mode



Software STORE Operation

Software STORE allows the user to trigger a STORE operation through a special SPI instruction. STORE operation is initiated by executing STORE instruction irrespective of whether a write has been performed since the last NV operation.

A STORE cycle takes t_{STORE} time to complete, during which all the memory accesses to nvSRAM are inhibited. The RDY bit of the Status Register or the HSB pin may be polled to find the Ready/Busy status of the nvSRAM. After the t_{STORE} cycle time is completed, the SRAM is activated again for read and write operations.

Hardware STORE and $\overline{HSB}$ Pin Operation

The $\overline{HSB}$ pin in CY14B256P is used to control and acknowledge STORE operations. If no STORE/RECALL is in progress, this pin can be used to request a Hardware STORE cycle. When the HSB pin is driven LOW, the CY14B256P conditionally initiates a STORE operation after t_{DELAY} duration. An actual STORE cycle starts only if a write to the SRAM is performed since the last STORE or RECALL cycle. Reads and writes to the memory are inhibited for t_{STORE} duration or as long as $\overline{HSB}$ pin is LOW.

The $\overline{HSB}$ pin also acts as an open drain driver (internal 100 kΩ weak pull-up resistor) that is internally driven LOW to indicate a busy condition when the STORE (initiated by any means) is in progress.

Note After each Hardware and Software STORE operation $\overline{HSB}$ is driven HIGH for a short time (t_{HHHD}) with standard output high current and then remains HIGH by an internal 100 kΩ pull-up resistor.

Note For successful last data byte STORE, a hardware store should be initiated atleast one clock cycle after the last data bit D0 is received.

Upon completion of the STORE operation, the nvSRAM memory access is inhibited for t_{LZHSB} time after $\overline{HSB}$ pin returns HIGH. The $\overline{HSB}$ pin must be left unconnected if not used.

RECALL Operation

A RECALL operation transfers the data stored in the nonvolatile QuantumTrap elements to the SRAM. In CY14B256P, a RECALL may be initiated in two ways: Hardware RECALL, initiated on power-up; and Software RECALL, initiated by a SPI RECALL instruction.

Internally, RECALL is a two step procedure. First, the SRAM data is cleared. Next, the nonvolatile information is transferred into the SRAM cells. All memory accesses are inhibited while a RECALL cycle is in progress. The RECALL operation does not alter the data in the nonvolatile elements.

Hardware RECALL (Power-Up)

During power-up, when V_{CC} crosses V_{SWITCH}, an automatic RECALL sequence is initiated, which transfers the content of nonvolatile memory on to the SRAM.

A Power-Up RECALL cycle takes t_{FA} time to complete and the memory access is disabled during this time. HSB pin is used to detect the Ready status of the device.

Software RECALL

Software RECALL allows the user to initiate a RECALL operation to restore the content of nonvolatile memory on to the SRAM. In CY14B256P, this can be done by issuing a RECALL instruction in SPI.

A Software RECALL takes t_{RECALL} time to complete during which all memory accesses to nvSRAM are inhibited. The controller must provide sufficient delay for the RECALL operation to complete before issuing any memory access instructions.

Disabling and Enabling AutoStore

If the application does not require the AutoStore feature, it can be disabled in CY14B256P by using the ASDISB instruction. If this is done, the nvSRAM does not perform a STORE operation at power-down.

Note CY14B256P comes from the factory with AutoStore Enabled.

AutoStore can be re-enabled by using the ASENB instruction. However, these operations are not nonvolatile and if the user needs this setting to survive the power cycle, a STORE operation must be performed following AutoStore Disable or Enable operation.

Note If AutoStore is disabled and V_{CAP} is not required, then the V_{CAP} pin must be left open. The V_{CAP} pin must never be connected to ground. The power-up RECALL operation cannot be disabled in any case.

Noise Considerations

Refer to CY application note AN1064.

Serial Peripheral Interface

SPI Overview

The SPI is a four-pin interface with chip select ($\overline{CS}$), serial input (SI), serial output (SO), and serial clock (SCK) pins. CY14B256P provides serial access to nvSRAM through SPI interface. The SPI bus on CY14B256P can run at speeds of up to 40 MHz for all instructions except RDRTC which runs at 25 MHz.

The SPI is a synchronous serial interface which uses clock and data pins for memory access and supports multiple devices on the data bus. A device on SPI bus is activated using the $\overline{CS}$ pin.

The relationship between chip select, clock, and data is dictated by the SPI mode. CY14B256P supports SPI modes 0 and 3. In both these modes, data is clocked into the nvSRAM on the rising edge of SCK starting from the first rising edge after $\overline{CS}$ goes active.

The SPI protocol is controlled by opcodes. These opcodes specify the commands from the bus master to the slave device. After $\overline{CS}$ is activated the first byte transferred from the bus master is the opcode. Following the opcode, any addresses and data are then transferred. The $\overline{CS}$ must go inactive after an operation is complete and before a new opcode can be issued. The commonly used terms used in SPI protocol are as follows.

SPI Master

The SPI master device controls the operations on a SPI bus. A SPI bus may have only one master with one or more slave devices. All the slaves share the same SPI bus lines and the master may select any of the slave devices using the $\overline{CS}$ pin. All the operations must be initiated by the master activating a slave device by pulling the $\overline{CS}$ pin of the slave LOW. The master also generates the SCK and all the data transmission on SI and SO lines are synchronized with this clock.

SPI Slave

The SPI slave device is activated by the master through the chip select line. A slave device gets the SCK as an input from the SPI master and all the communication is synchronized with this clock. SPI slave never initiates a communication on the SPI bus and acts on the instruction from the master.

CY14B256P operates as a slave device and may share the SPI bus with multiple CY14B256P devices or other SPI devices.

Chip Select ($\overline{CS}$)

For selecting any slave device, the master needs to pull-down the corresponding $\overline{CS}$ pin. Any instruction can be issued to a slave device only when the $\overline{CS}$ pin is LOW.

The CY14B256P is selected when the $\overline{CS}$ pin is LOW. When the device is not selected, data through the SI pin is ignored and the serial output pin (SO) remains in a high-impedance state.

Note A new instruction must begin with the falling edge of $\overline{CS}$. Therefore, only one opcode can be issued for each active chip select cycle.

Serial Clock (SCK)

Serial clock is generated by the SPI master and the communication is synchronized with this clock after $\overline{CS}$ goes LOW.

CY14B256P allows SPI modes 0 and 3 for data communication. In both these modes, the inputs are latched by the slave device on the rising edge of SCK and outputs are issued on the falling edge. Therefore, the first rising edge of SCK signifies the arrival of the first bit (MSB) of SPI instruction on the SI pin. Further, all data inputs and outputs are synchronized with SCK.

Data Transmission SI and SO

SPI data bus consists of two lines, SI and SO, for serial data communication. The SI is also referred to as Master Out Slave In (MOSI) and SO is referred to as Master In Slave Out (MISO). The master issues instructions to the slave through the SI pin, while the slave responds through the SO pin. Multiple slave devices may share the SI and SO lines as described earlier.

CY14B256P has two separate pins for SI and SO which can be connected with the master as shown in Figure 3 on page 7.

Most Significant Bit (MSB)

The SPI protocol requires that the first bit to be transmitted is the most significant bit (MSB). This is valid for both address and data transmission.

The 256-Kbit serial nvSRAM requires a 2-byte address for any read or write operation. However, because the address is only 15 bits, it implies that the first MSB which is fed in is ignored by the device. Although this bit is ‘don’t care’, Cypress recommends that this bit is treated as 0 to enable seamless transition to higher memory densities.

Serial Opcode

After the slave device is selected with $\overline{CS}$ going LOW, the first byte received is treated as the opcode for the intended operation.

CY14B256P uses the standard opcodes for memory accesses. In addition to the memory accesses, CY14B256P provides additional opcodes for the nvSRAM specific functions: STORE, RECALL, AutoStore Enable, and AutoStore Disable. Refer to Table 2 on page 8 for details on opcodes.

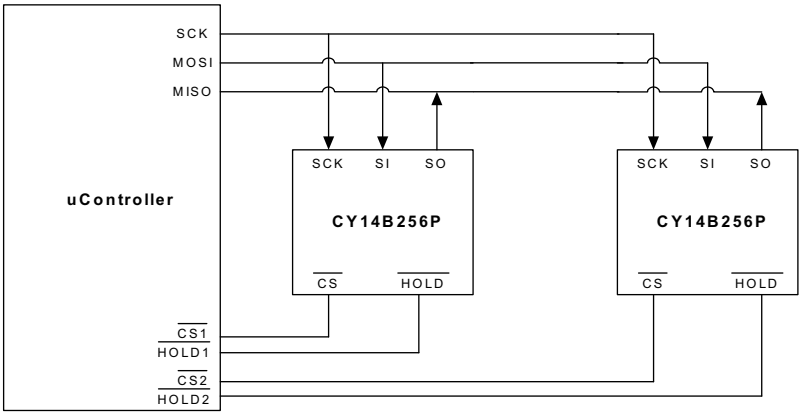
Invalid Opcode

If an invalid opcode is received, the opcode is ignored and the device ignores any additional serial data on the SI pin till the next falling edge of $\overline{CS}$ and the SO pin remains tri-stated.

Status Register

CY14B256P has an 8-bit Status Register. The bits in the Status Register are used to configure the SPI bus. These bits are described in the Table 4 on page 9.

Figure 3. System Configuration using SPI nvSRAM



SPI Modes

CY14B256P device may be driven by a microcontroller with its SPI peripheral running in either of these two modes:

- SPI Mode 0 (CPOL=0, CPHA=0)
- SPI Mode 3 (CPOL=1, CPHA=1)

For both these modes, the input data is latched in on the rising edge of SCK starting from the first rising edge after CS goes active. If the clock starts from a HIGH state (in mode 3), the first rising edge after the clock toggles is considered. The output data is available on the falling edge of SCK.

The two SPI modes are shown in Figure 4 and Figure 5. The status of clock when the bus master is in standby mode and not transferring data is:

- SCK remains at 0 for Mode 0
- SCK remains at 1 for Mode 3

CPOL and CPHA bits must be set in the SPI controller for the either Mode 0 or Mode 3. CY14B256P detects the SPI mode from the status of SCK pin when the device is selected by bringing the CS pin LOW. If SCK pin is LOW when the device is selected, SPI Mode 0 is assumed and if SCK pin is HIGH, CY14B256P works in SPI Mode 3.

Figure 4. SPI Mode 0

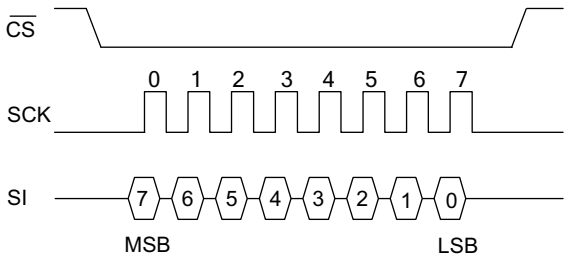
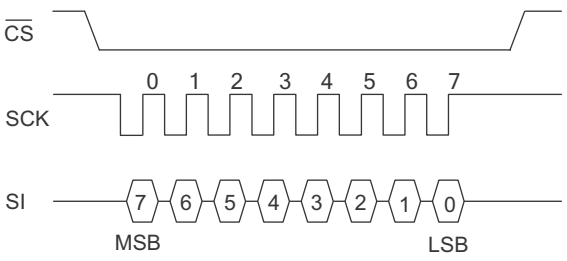


Figure 5. SPI Mode 3



SPI Operating Features

Power-Up

Power-up is defined as the condition when the power supply is turned on and V_{CC} crosses Vswitch voltage. During this time, the $\overline{CS}$ must be enabled to follow the V_{CC} voltage. Therefore, $\overline{CS}$ must be connected to V_{CC} through a suitable pull-up resistor. As a built in safety feature, $\overline{CS}$ is both edge-sensitive and level-sensitive. After power-up, the device is not selected until a falling edge is detected on $\overline{CS}$. This ensures that $\overline{CS}$ must have been HIGH, before going LOW to start the first operation.

As described earlier, nvSRAM performs a Power-Up RECALL operation after power-up and therefore, all memory accesses are disabled for t_{FA} duration after power-up. The $\overline{HSB}$ pin can be probed to check the Ready/Busy status of nvSRAM after power-up.

Power On Reset

A power on reset (POR) circuit is included to prevent inadvertent writes. At power-up, the device does not respond to any instruction until the V_{CC} reaches the POR threshold voltage (V_{SWITCH}). After V_{CC} transitions the POR threshold, the device is internally reset and performs an Power-Up RECALL operation. During Power-Up RECALL all device accesses are inhibited. The device is in the following state after POR:

- Deselected (after power-up, a falling edge is required on $\overline{CS}$ before any instructions are started).
- Standby power mode
- Not in the HOLD condition
- Status Register state:
  - Write enable (WEN) bit is reset to '0'.
  - WPEN, BP1, BP0 unchanged from previous STORE operation
  - Don't care bits 4-6 are reset to '0'.

The WPEN, BP1, and BP0 bits of the Status Register are nonvolatile bits and remain unchanged from the previous STORE operation.

Prior to selecting and issuing instructions to the memory, a valid and stable V_{CC} voltage must be applied. This voltage must remain valid until the end of the instruction transmission.

Power-Down

At power-down (continuous decay of V_{CC}), when V_{CC} drops from the normal operating voltage and below the V_{SWITCH} threshold voltage, the device stops responding to any instruction sent to it. If a write cycle is in progress and the last data bit D0 has been received when the power goes down, it is allowed t_{DELAY} time to complete the write. After this, all memory accesses are inhibited and a conditional AutoStore operation is performed (AutoStore is not performed if no writes have happened since the last RECALL cycle). This feature prevents inadvertent writes to nvSRAM from happening during power-down.

However, to avoid the possibility of inadvertent writes during power-down, ensure that the device is deselected and is in standby power mode, and the $\overline{CS}$ follows the voltage applied on V_{CC}.

Active Power and Standby Power Modes

When $\overline{CS}$ is LOW, the device is selected and is in the active power mode. The device consumes I_{CC} current, as specified in DC Electrical Characteristics on page 25. When $\overline{CS}$ is HIGH, the device is deselected and the device goes into the standby power mode if a STORE or RECALL cycle is not in progress. If a STORE/RECALL cycle is in progress, the device goes into the standby power mode after the STORE/RECALL cycle is completed. In the standby power mode, the current drawn by the device drops to I_{SB}.

SPI Functional Description

The CY14B256P uses an 8-bit instruction register. Instructions and their operation codes are listed in Table 2. All instructions, addresses, and data are transferred with the MSB first and start with a HIGH to LOW $\overline{CS}$ transition. There are, in all, 12 SPI instructions that provide access to most of the functions in nvSRAM. Further, the $\overline{WP}$, HOLD and $\overline{HSB}$ pins provide additional functionality driven through hardware.

Table 2. Instruction Set

Instruction Category	Instruction Name	Opcode	Operation
Status Register instructions	WREN	0000 0110	Set write enable latch
	WRDI	0000 0100	Reset write enable latch
	RDSR	0000 0101	Read Status Register
	WRSR	0000 0001	Write Status Register
SRAM read/write instructions	READ	0000 0011	Read data from memory array
	WRITE	0000 0010	Write data to memory array
RTC read/write instructions	RDRTC	0001 0011	Read RTC registers
	WRTC	0001 0010	Write RTC registers
Special NV instructions	STORE	0011 1100	Software STORE
	RECALL	0110 0000	Software RECALL
	ASENB	0101 1001	AutoStore enable
	ASDISB	0001 1001	AutoStore disable
Reserved	- Reserved -	0001 1110	

The SPI instructions in CY14B256P are divided based on their functionality in the following types:

- Status Register access: RDSR and WRSR instructions
- Write protection functions: WREN and WRDI instructions along with $\overline{WP}$ pin and WEN, BP0, and BP1 bits
- SRAM memory access: READ and WRITE instructions
- RTC access: RDRTC and WRTC instructions
- nvSRAM special instructions: STORE, RECALL, ASENB, and ASDISB

Status Register

The Status Register bits are listed in Table 3. The Status Register consists of a Ready bit ($\overline{RDY}$) and data protection bits BP1, BP0, WEN, and WPEN. The $\overline{RDY}$ bit can be polled to check the ready/busy status while a nvSRAM STORE or Software RECALL cycle is in progress. The Status Register can be modified by WRSR instruction and read by RDSR instruction. However, only the WPEN, BP1, and BP0 bits of the Status Register can be modified by using the WRSR instruction. The WRSR instruction has no effect on WEN and $\overline{RDY}$ bits. The default value shipped from the factory for WEN, BP0, BP1, bits 4-6 and WPEN bits is '0'.

Table 3. Status Register Format

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
WPEN (0)	X (0)	X (0)	X (0)	BP1 (0)	BP0 (0)	WEN (0)	$\overline{RDY}$

Table 4. Status Register Bit Definition

Bit	Definition	Description
Bit 0 ($\overline{RDY}$)	Ready	Read only bit indicates the ready status of device to perform a memory access. This bit is set to '1' by the device while a STORE or Software RECALL cycle is in progress.
Bit 1 (WEN)	Write enable	WEN indicates if the device is write enabled. This bit defaults to '0' (disabled) on power-up. WEN = '1' --> Write enabled WEN = '0' --> Write disabled
Bit 2 (BP0)	Block protect bit '0'	Used for block protection. For details see Table 5 on page 10.
Bit 3 (BP1)	Block protect bit '1'	Used for block protection. For details see Table 5 on page 10.
Bit 4-6	Don't care	Bits are writable and volatile. On power-up, bits are written with '0'.
Bit 7 (WPEN)	Write protect enable bit	Used for enabling the function of write protect pin ($\overline{WP}$). For details see Table 6 on page 11.

Read Status Register (RDSR) Instruction

The Read Status Register (RDSR) instruction provides access to the Status Register. This instruction is used to probe the write enable status of the device or the Ready status of the device. $\overline{RDY}$ bit is set by the device to '1' whenever a STORE or Software RECALL cycle is in progress. The block protection and WPEN bits indicate the extent of protection employed.

This instruction is issued after the falling edge of $\overline{CS}$ using the opcode for RDSR.

Write Status Register (WRSR) Instruction

The WRSR instruction enables the user to write to the Status Register. However, this instruction cannot be used to modify bit 0 and bit 1 ($\overline{RDY}$ and WEN). The BP0 and BP1 bits can be used to select one of four levels of block protection. Further, WPEN bit must be set to '1' to enable the use of Write Protect ($\overline{WP}$) pin.

WRSR instruction is a write instruction and needs writes to be enabled (WEN bit set to '1') using the WREN instruction before it is issued. The instruction is issued after the falling edge of $\overline{CS}$ using the opcode for WRSR followed by eight bits of data to be stored in the Status Register. Since only bits 2, 3, and 7 can be modified by WRSR instruction, it is recommended to leave the bits 4-6 as '0' while writing to the Status Register.

Note In CY14B256P, the values written to Status Register are saved to nonvolatile memory only after a STORE operation. If AutoStore is disabled, any modifications to the Status Register must be secured by performing a Software STORE operation.

Figure 6. Read Status Register (RDSR) Instruction Timing

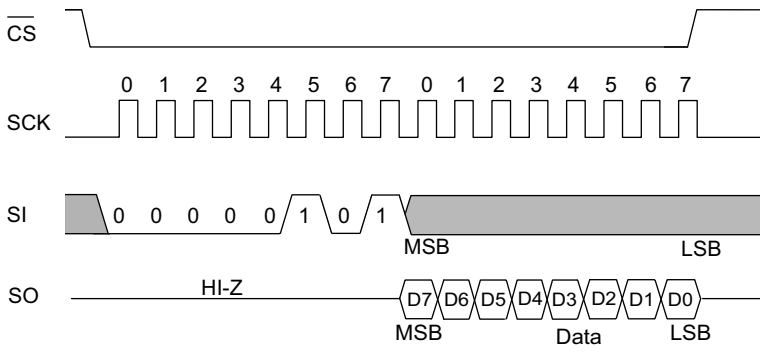
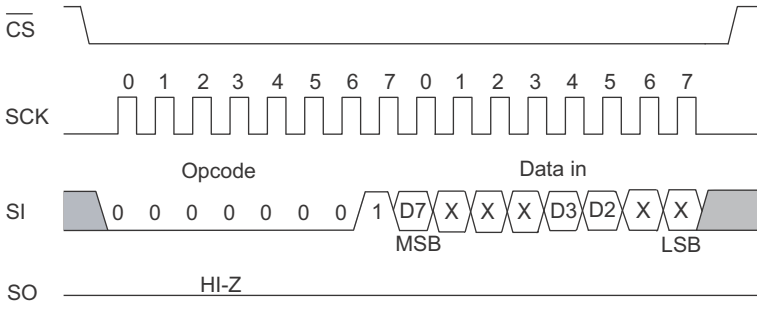


Figure 7. Write Status Register (WRSR) Instruction Timing



Write Protection and Block Protection

CY14B256P provides features for both software and hardware write protection using WRDI instruction and WP. Additionally, this device also provides block protection mechanism through BP0 and BP1 pins of the Status Register.

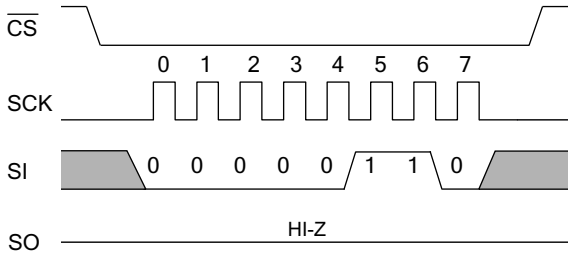
The write enable and disable status of the device is indicated by WEN bit of the Status Register. The write instructions (WRSR, WRITE, and WRTC) and nvSRAM special instruction (STORE, RECALL, ASENB, ASDISB) need the write to be enabled (WEN bit = 1) before they can be issued.

Write Enable (WREN) Instruction

On power-up, the device is always in the write disable state. The following WRITE, WRSR, WRTC, or nvSRAM special instruction must therefore be preceded by a Write Enable instruction. If the device is not write enabled (WEN = '0'), it ignores the write instructions and returns to the standby state when CS is brought HIGH. A new CS falling edge is required to re-initiate serial communication. The instruction is issued following the falling edge of CS. When this instruction is used, the WEN bit of Status Register is set to '1'. WEN bit defaults to '0' on power-up.

Note After completion of a write instruction (WRSR, WRITE, or WRTC) or nvSRAM special instruction (STORE, RECALL, ASENB, ASDISB) instruction, WEN bit is cleared to '0'. This is done to provide protection from any inadvertent writes. Therefore, WREN instruction must be used before a new write instruction is issued.

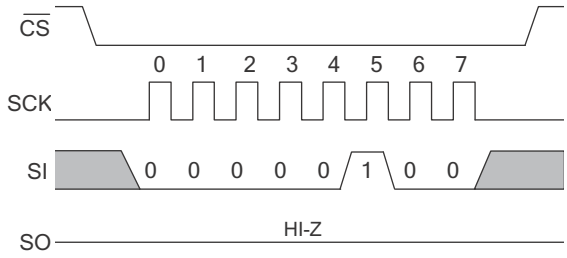
Figure 8. WREN Instruction



Write Disable (WRDI) Instruction

Write Disable instruction disables the write by clearing the WEN bit to '0' to protect the device against inadvertent writes. This instruction is issued following the falling edge of CS followed by opcode for WRDI instruction. The WEN bit is cleared on the rising edge of CS following a WRDI instruction.

Figure 9. WRDI Instruction



Block Protection

Block protection is provided using the BP0 and BP1 pins of the Status Register. These bits can be set using WRSR instruction and probed using the RDSR instruction. The nvSRAM is divided into four array segments. One-quarter, one-half, or all of the memory segments can be protected. Any data within the protected segment is read only. Table 5 shows the function of block protect bits.

Table 5. Block Write Protect Bits

Level	Status Register Bits		Array Addresses Protected
	BP1	BP0	
0	0	0	None
1 (1/4)	0	1	0x6000-0x7FFF
2 (1/2)	1	0	0x4000-0x7FFF
3 (All)	1	1	0x0000-0x7FFF

Hardware Write Protection ($\overline{WP}$ Pin)

The write protect pin ($\overline{WP}$) is used to provide hardware write protection. $\overline{WP}$ pin allows all normal read and write operations when held HIGH. When the $\overline{WP}$ pin is brought LOW and WPEN bit is '1', all write operations to the Status Register are inhibited. The hardware write protection function is blocked when the WPEN bit is '0'. This allows the user to install the CY14B256P in a system with the $\overline{WP}$ pin tied to ground, and still write to the Status Register.

$\overline{WP}$ pin can be used along with WPEN and block protect bits (BP1 and BP0) of the Status Register to inhibit writes to memory. When $\overline{WP}$ pin is LOW and WPEN is set to '1', any modifications to the Status Register are disabled. Therefore, the memory is protected by setting the BP0 and BP1 bits and the $\overline{WP}$ pin inhibits any modification of the Status Register bits, providing hardware write protection.

Note $\overline{WP}$ going LOW when $\overline{CS}$ is still LOW has no effect on any of the ongoing write operations to the Status Register.

Table 6 summarizes all the protection features provided in the CY14B256P.

Table 6. Write Protection Operation

WPEN	$\overline{WP}$	WEN	Protected Blocks	Unprotected Blocks	Status Register
X	X	0	Protected	Protected	Protected
0	X	1	Protected	Writable	Writable
1	LOW	1	Protected	Writable	Protected
1	HIGH	1	Protected	Writable	Writable

Memory Access

All memory accesses are done using the READ and WRITE instructions. These instructions cannot be used while a STORE or RECALL cycle is in progress. A STORE cycle in progress is indicated by the $\overline{RDY}$ bit of the Status Register and the $\overline{HSB}$ pin.

Read Sequence (READ) instruction

The read operations on CY14B256P are performed by giving the instruction on the SI pin and reading the output on SO pin. The following sequence needs to be followed for a read operation: After the $\overline{CS}$ line is pulled LOW to select a device, the read opcode is transmitted through the SI line followed by two bytes of address. The MSB bit (A15) of the address is a "don't care". After the last address bit is transmitted on the SI pin, the data (D7-D0) at the specific address is shifted out on the SO line on the falling edge of SCK starting with D7. Any other data on SI line after the last address bit is ignored.

CY14B256P allows reads to be performed in bursts through SPI which can be used to read consecutive addresses without issuing a new READ instruction. If only one byte is to be read, the $\overline{CS}$ line must be driven HIGH after one byte of data comes out. However, the read sequence may be continued by holding the $\overline{CS}$ line LOW and the address is automatically incremented and data continues to shift out on SO pin. When the last data memory address (0x7FFF) is reached, the address rolls over to 0x0000 and the device continues to read.

Write Sequence (WRITE) instruction

The write operations on CY14B256P are performed through the SI pin. To perform a write operation CY14B256P, if the device is write disabled, then the device must first be write enabled through the WREN instruction. When the writes are enabled (WEN = '1'), WRITE instruction is issued after the falling edge of $\overline{CS}$. A WRITE instruction constitutes transmitting the WRITE opcode on SI line followed by 2 bytes of address and the data (D7-D0) which is to be written. The MSB bit (A15) of the address is a "don't care".

CY14B256P allows writes to be performed in bursts through SPI which can be used to write consecutive addresses without issuing a new WRITE instruction. If only one byte is to be written, the $\overline{CS}$ line must be driven HIGH after the D0 (LSB of data) is transmitted. However, if more bytes are to be written, $\overline{CS}$ line must be held LOW and address is incremented automatically. The following bytes on the SI line are treated as data bytes and written in the successive addresses. When the last data memory address (0x7FFF) is reached, the address rolls over to 0x0000 and the device continues to write. The WEN bit is reset to '0' on completion of a WRITE sequence.

Note When a burst write reaches a protected block address, it continues the address increment into the protected space but does not write any data to the protected memory. If the address roll over takes the burst write to unprotected space, it resumes writes. The same operation is true if a burst write is initiated within a write protected block.

Figure 10. Read Instruction Timing

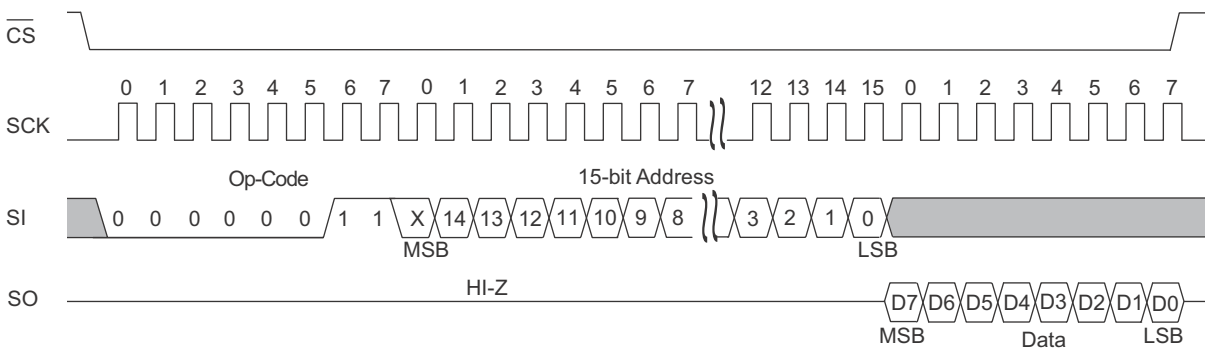


Figure 11. Burst Mode Read Instruction Timing

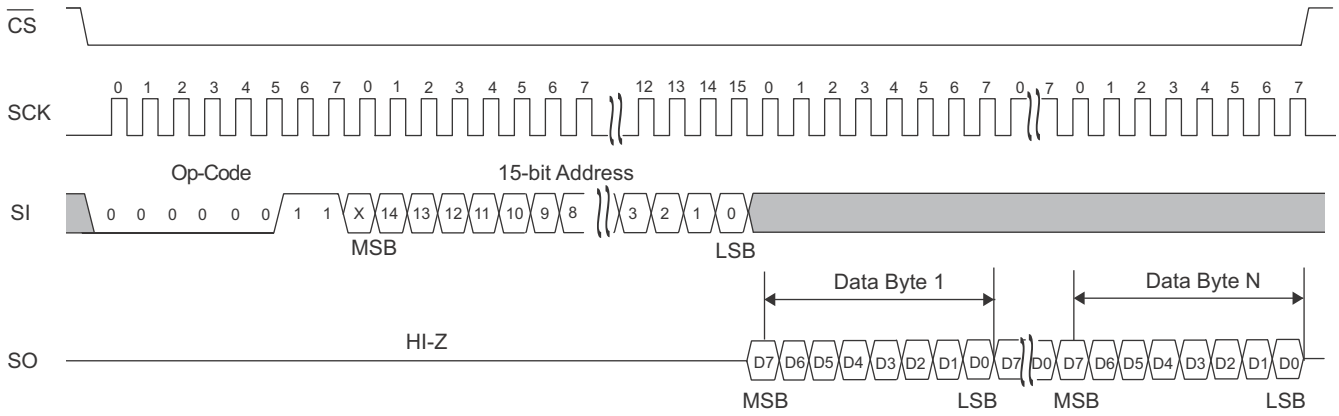


Figure 12. Write Instruction Timing

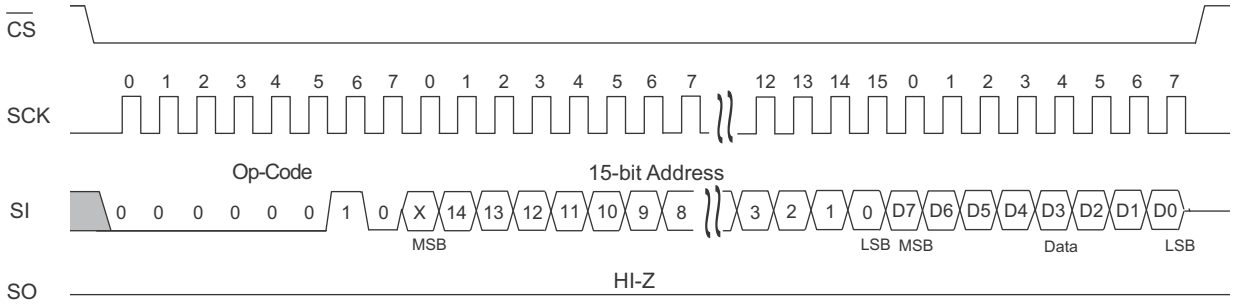
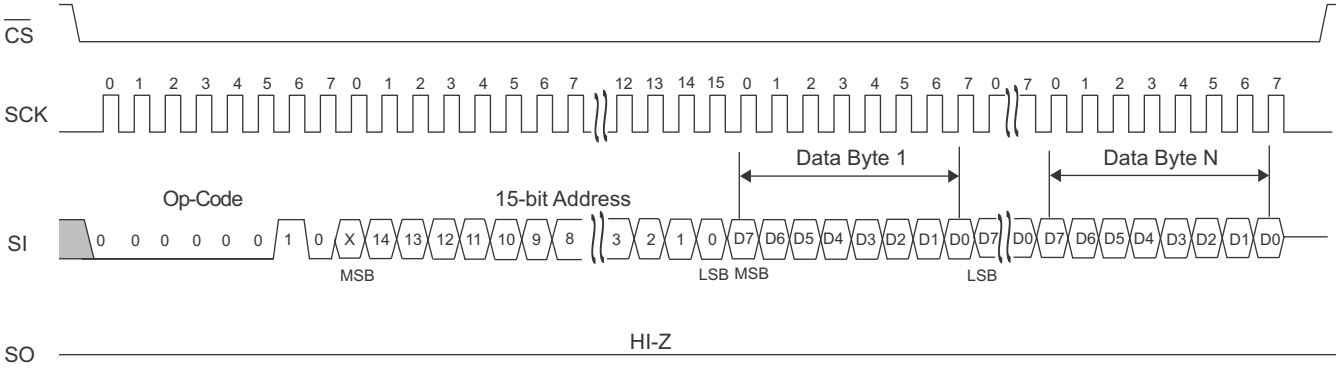


Figure 13. Burst Mode Write Instruction Timing



RTC Access

CY14B256P uses 16 registers for RTC. These registers can be read out or written to by accessing all 16 registers in burst mode or accessing each register, one at a time. The RDRTC and WRTC instructions are used to access the RTC.

All the RTC registers can be read in burst mode by issuing the RDRTC instruction and reading all 16 bytes without bringing the $\overline{CS}$ pin HIGH. The ‘R’ bit must be set while reading the RTC timekeeping registers to ensure that transitional values of time are not read.

Writes to the RTC register are performed using the WRTC instruction. Writing RTC timekeeping registers and control registers, except for the flags register needs the ‘W’ bit of the flags register to be set to ‘1’. The internal counters are updated with the new date and time setting when the ‘W’ bit is cleared to ‘0’. All the RTC registers can also be written in burst mode using the WRTC instruction.

READ RTC (RDRTC) Instruction

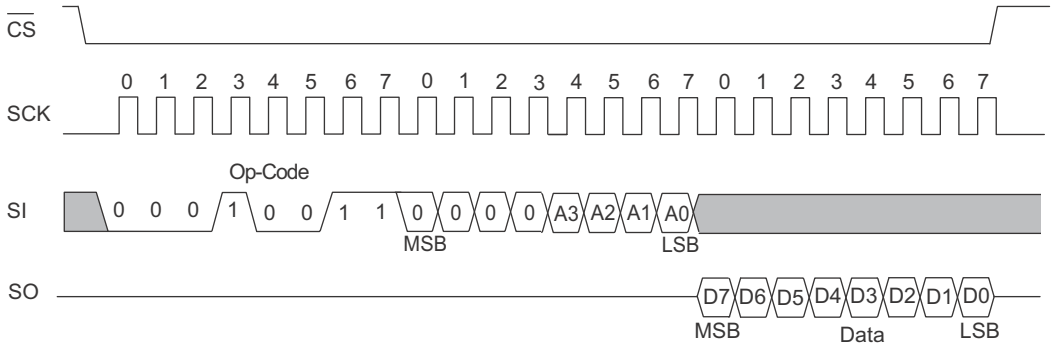
Read RTC (RDRTC) instruction allows the user to read the contents of RTC registers. Reading the RTC registers through the SO pin requires the following sequence: After the $\overline{CS}$ line is pulled LOW to select a device, the RDRTC opcode is transmitted through the SI line followed by eight address bits for selecting the register. Any data on the SI line after the address bits is ignored. The data (D7-D0) at the specified address is then shifted out onto the SO line. RDRTC also allows burst mode read operation. When reading multiple bytes from RTC registers, the address rolls over to 0x00 after the last RTC register address (0x0F) is reached.

The ‘R’ bit in RTC flags register must be set to '1' before reading RTC time keeping registers to avoid reading transitional data. Modifying the RTC flags register requires a Write RTC cycle. The R bit must be cleared to '0' after completion of the read operation.

The easiest way to read RTC registers is to perform RDRTC in burst mode. The read may start from the first RTC register (0x00) and the $\overline{CS}$ must be held LOW to allow the data from all 16 RTC registers to be transmitted through the SO pin.

Note Read RTC (RDRTC) instruction operates at a maximum clock frequency of 25 MHz. The opcode cycles, address cycles and data out cycles need to run at 25 MHz for the instruction to work properly.

Figure 14. Read RTC (RDRTC) Instruction Timing

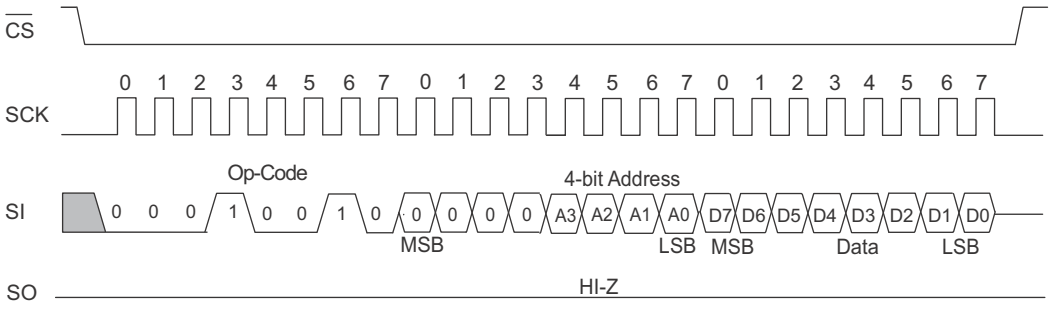


WRITE RTC (WRTC) Instruction

WRITE RTC (WRTC) instruction allows the user to modify the contents of RTC registers. The WRTC instruction requires the WEN bit to be set to '1' before it can be issued. If WEN bit is '0', a WREN instruction needs to be issued before using WRTC. Writing RTC registers requires the following sequence: After the $\overline{CS}$ line is pulled LOW to select a device, WRTC opcode is transmitted through the SI line followed by eight address bits identifying the register which is to be written to and one or more bytes of data. WRTC allows burst mode write operation. When writing more than one registers in burst mode, the address rolls over to 0x00 after the last RTC address (0x0F) is reached.

Note that writing to RTC timekeeping and control registers require the W bit to be set to '1'. The values in these RTC registers take effect only after the ‘W’ bit is cleared to '0'. Write enable bit (WEN) is automatically cleared to ‘0’ after completion of the WRTC instruction.

Figure 15. Write RTC (WRTC) Instruction Timing



nvSRAM Special Instructions

CY14B256P provides four special instructions that allow access to the nvSRAM specific functions: STORE, RECALL, ASDISB, and ASENB. Table 7 lists these instructions.

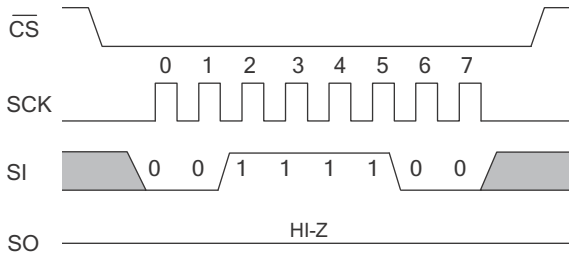
Table 7. nvSRAM Special Instructions

Function Name	Opcode	Operation
STORE	0011 1100	Software STORE
RECALL	0110 0000	Software RECALL
ASENB	0101 1001	AutoStore Enable
ASDISB	0001 1001	AutoStore Disable

Software STORE (STORE) instruction

When a STORE instruction is executed, CY14B256P performs a Software STORE operation. The STORE operation is performed irrespective of whether a write has taken place since the last STORE or RECALL operation.

Figure 16. Software STORE Operation



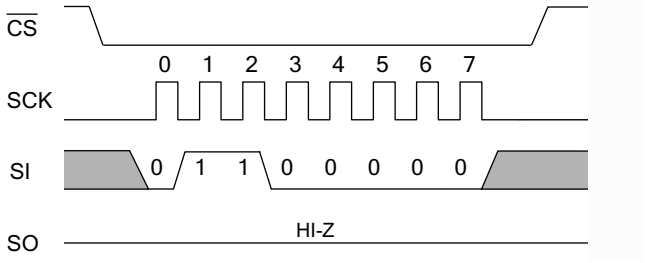
To issue this instruction, the device must be write enabled (WEN bit = '1').The instruction is performed by transmitting the STORE opcode on the SI pin following the falling edge of CS. The WEN bit is cleared on the positive edge of CS following the STORE instruction.

Software RECALL (RECALL) instruction

When a RECALL instruction is executed, CY14B256P performs a Software RECALL operation. To issue this instruction, the device must be write enabled (WEN = '1').

The instruction is performed by transmitting the RECALL opcode on the SI pin following the falling edge of CS. The WEN bit is cleared on the positive edge of CS following the RECALL instruction.

Figure 17. Software RECALL Operation

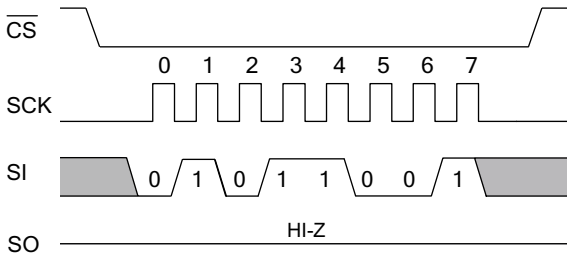


AutoStore Enable (ASENB) instruction

The AutoStore Enable instruction enables the AutoStore on CY14B256P. This setting is not nonvolatile and needs to be followed by a STORE sequence if this is desired to survive the power cycle.

To issue this instruction, the device must be write enabled (WEN = '1'). The instruction is performed by transmitting the ASENB opcode on the SI pin following the falling edge of CS. The WEN bit is cleared on the positive edge of CS following the ASENB instruction.

Figure 18. AutoStore Enable Operation

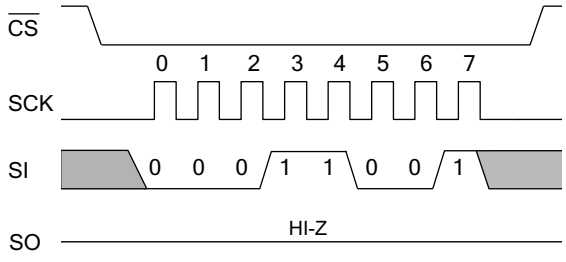


AutoStore Disable (ASDISB) instruction

AutoStore is enabled by default in CY14B256P. The AutoStore Disable instruction disables the AutoStore on CY14B256P. This setting is not nonvolatile and needs to be followed by a STORE sequence if this is desired to survive the power cycle.

To issue this instruction, the device must be write enabled (WEN = '1'). The instruction is performed by transmitting the ASDISB opcode on the SI pin following the falling edge of $\overline{CS}$. The WEN bit is cleared on the positive edge of $\overline{CS}$ following the ASDISB instruction.

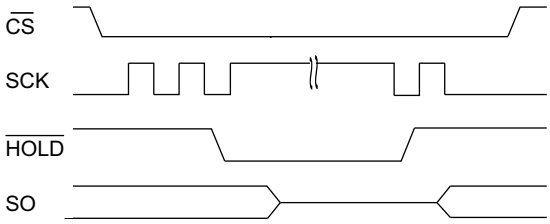
Figure 19. AutoStore Disable Operation



$\overline{HOLD}$ Pin Operation

The $\overline{HOLD}$ pin is used to pause the serial communication. When the device is selected and a serial sequence is underway, $\overline{HOLD}$ is used to pause the serial communication with the master device without resetting the ongoing serial sequence. To pause, the $\overline{HOLD}$ pin must be brought LOW when the SCK pin is LOW. $\overline{CS}$ pin must remain LOW along with $\overline{HOLD}$ pin to pause serial communication. While the device serial communication is paused, inputs to the SI pin are ignored and the SO pin is in the high impedance state. To resume serial communication, the $\overline{HOLD}$ pin must be brought HIGH when the SCK pin is LOW (SCK may toggle during $\overline{HOLD}$).

Figure 20. $\overline{HOLD}$ Operation



Real Time Clock Operation

nvTime Operation

The CY14B256P offers internal registers that contain clock, alarm, watchdog, interrupt, and control functions. The RTC registers occupy a separate address space from nvSRAM and are accessible through Read RTC (RDRTC) and Write RTC (WRTC) instructions on register addresses 0x00 to 0x0F. Internal double buffering of the clock and the timer information registers prevents accessing transitional internal clock data during a read or write operation. Double buffering also circumvents disrupting normal timing counts or the clock accuracy of the internal clock when accessing clock data. Clock and alarm registers store data in BCD format.

Clock Operations

The clock registers maintain time up to 9,999 years in one-second increments. The time can be set to any calendar time and the clock automatically keeps track of days of the week and month, leap years, and century transitions. There are eight registers dedicated to the clock functions, which are used to set time with a write cycle and to read time during a read cycle. These registers contain the time of day in BCD format. Bits defined as ‘0’ are currently not used and are reserved for future use by Cypress.

Reading the Clock

The double buffered RTC register structure reduces the chance of reading incorrect data from the clock. The user must stop internal updates to the CY14B256P time keeping registers before reading clock data, to prevent reading of data in transition. Stopping the register updates does not affect clock accuracy.

The updating process is stopped by writing a ‘1’ to the read bit ‘R’ (in the flags register at 0x00), and does not restart until a ‘0’ is written to the read bit. The RTC registers are read while the internal clock continues to run. After a ‘0’ is written to the read bit (‘R’), all RTC registers are simultaneously updated within 20 ms.

Setting the Clock

Setting the write bit ‘W’ (in the flags register at 0x00) to a ‘1’ stops updates to the time keeping registers and enables the time to be set. The correct day, date, and time is then written into the registers and must be in 24-hour BCD format. The time written is referred to as the “Base Time”. This value is stored in nonvolatile registers and used in the calculation of the current time. Resetting the write bit to ‘0’ transfers the values of timekeeping registers to the actual clock counters, after which the clock resumes normal operation.

If the time written to the timekeeping registers is not in the correct BCD format, each invalid nibble of the RTC registers continue counting to 0xF before rolling over to 0x0 after which RTC resumes normal operation.

Note After the ‘W’ bit is set to ‘0’, values written into the timekeeping, alarm, calibration, and interrupt registers are transferred to the RTC time keeping counters in t_{RTCp} time. These counter values must be saved to nonvolatile memory either by initiating a Software/Hardware STORE or AutoStore operation. While working in AutoStore disabled mode, perform a STORE operation after t_{RTCp} time while writing into the RTC registers for the modifications to be correctly recorded.

Backup Power

The RTC in the CY14B256P is intended for permanently powered operation. The V_{RTCcap} or V_{RTCbat} pin is connected depending on whether a capacitor or battery is chosen for the application. When the primary power, V_{CC}, fails and drops below V_{SWITCH} the device switches to the backup power supply.

The clock oscillator uses very little current, which maximizes the backup time available from the backup source. Regardless of the clock operation with the primary source removed, the data stored in the nvSRAM is secure, having been stored in the nonvolatile elements when power was lost.

During backup operation, the CY14B256P consumes 0.35 µA (typical) at room temperature. The user must choose capacitor or battery values according to the application.

Backup time values based on maximum current specifications are shown in the following table. Nominal backup times are approximately two times longer.

Table 8. RTC Backup Time

Capacitor Value	Backup Time
0.1 F	72 hours
0.47 F	14 days
1.0 F	30 days

Using a capacitor has the obvious advantage of recharging the backup source each time the system is powered up. If a battery is used, a 3-V lithium is recommended and the CY14B256P sources current only from the battery when the primary power is removed. However, the battery is not recharged at any time by the CY14B256P. The battery capacity must be chosen for the total anticipated cumulative down time required over the life of the system.

Stopping and Starting the Oscillator

The OSCEN bit in the calibration register at 0x08 controls the enable and disable of the oscillator. This bit is nonvolatile and is shipped to customers in the “enabled” (set to ‘0’) state. To preserve the battery life when the system is in storage, OSCEN must be set to ‘1’. This turns off the oscillator circuit, extending the battery life. If the OSCEN bit goes from disabled to enabled, it takes approximately one second (two seconds maximum) for the oscillator to start.

While system power is off, if the voltage on the backup supply (V_{RTCcap} or V_{RTCbat}) falls below their respective minimum level, the oscillator may fail. The CY14B256P has the ability to detect oscillator failure when system power is restored. This is recorded in the oscillator fail flag (OSCF) of the flags register at the address 0x00. When the device is powered on (V_{CC} goes above V_{SWITCH}) the OSCEN bit is checked for “enabled” status. If the OSCEN bit is enabled and the oscillator is not active within the first 5 ms, the OSCF bit is set to ‘1’. The system must check for this condition and then write ‘0’ to clear the flag. Note that in addition to setting the OSCF flag bit, the time registers are reset to the “Base Time” (see Setting the Clock on page 16), which is the value last written to the timekeeping registers. The control or calibration registers and the OSCEN bit are not affected by the ‘oscillator failed’ condition.

The value of OSCF must be reset to ‘0’ when the time registers are written for the first time. This initializes the state of this bit, which may have become set when the system was first powered on.

To reset OSCF, set the write bit ‘W’ (in the flags register at 0x00) to a ‘1’ to enable writes to the flags register. Write a ‘0’ to the OSCF bit and then reset the write bit to ‘0’ to disable writes.

Calibrating the Clock

The RTC is driven by a quartz controlled crystal with a nominal frequency of 32.768 kHz. Clock accuracy depends on the quality of the crystal and calibration. The crystals available in the market typically have an error of ±20 ppm to ±35 ppm. However, CY14B256P employs a calibration circuit that improves the accuracy to +1/–2 ppm at 25 °C. This implies an error of +2.5 seconds to –5 seconds per month.

The calibration circuit adds or subtracts counts from the oscillator divider circuit to achieve this accuracy. The number of pulses that are suppressed (subtracted, negative calibration) or split (added, positive calibration) depends upon the value loaded into the five calibration bits found in calibration register at 0x08. The calibration bits occupy the five lower order bits in the calibration register. These bits are set to represent any value between ‘0’ and 31 in binary form. Bit D5 is a sign bit, where a ‘1’ indicates positive calibration and a ‘0’ indicates negative calibration. Adding counts speeds the clock up and subtracting counts slows the clock down. If a binary ‘1’ is loaded into the register, it corresponds to an adjustment of 4.068 or –2.034 ppm offset in oscillator error, depending on the sign.

Calibration occurs within a 64-minute cycle. The first 62 minutes in the cycle may, once every minute, have one second shortened by 128 or lengthened by 256 oscillator cycles. If a binary ‘1’ is loaded into the register, only the first two minutes of the 64-minute cycle are modified. If a binary 6 is loaded, the first 12 are affected, and so on. Therefore, each calibration step has the effect of adding 512 or subtracting 256 oscillator cycles for every 125,829,120 actual oscillator cycles, that is, 4.068 or –2.034 ppm of adjustment per calibration step in the calibration register.

To determine the required calibration, the CAL bit in the flags register (0x00) must be set to ‘1’. This causes the INT pin to toggle at a nominal frequency of 512 Hz. Any deviation measured from the 512 Hz indicates the degree and direction of the required correction. For example, a reading of 512.01024 Hz indicates a +20 ppm error. Hence, a decimal value of –10 (001010b) must be loaded into the Calibration register to offset this error.

Note Setting or changing the calibration register does not affect the test output frequency.

To set or clear CAL, set the write bit “W” (in the flags register at 0x00) to ‘1’ to enable writes to the flags register. Write a value to CAL, and then reset the write bit to “0” to disable writes.

Alarm

The alarm function compares user programmed values of alarm time and date (stored in the registers 0x01-5) with the corresponding time of day and date values. When a match occurs, the alarm internal flag (AF) is set and an interrupt is generated on INT pin if alarm interrupt enable (AIE) bit is set.

There are four alarm match fields: date, hours, minutes, and seconds. Each of these fields has a match bit that is used to determine if the field is used in the alarm match logic. Setting the match bit to ‘0’ indicates that the corresponding field is used in the match process. Depending on the match bits, the alarm occurs as specifically as once a month or as frequently as once every minute. Selecting none of the match bits (all 1s) indicates that no match is required and therefore, alarm is disabled. Selecting all match bits (all 0s) causes an exact time and date match.

There are two ways to detect an alarm event: by reading the AF flag or monitoring the INT pin. The AF flag in the flags register at 0x00 indicates that a date or time match has occurred. The AF bit is set to ‘1’ when a match occurs. Reading the flags register clears the alarm flag bit (and all others). A hardware interrupt pin may also be used to detect an alarm event.

To set, clear or enable an alarm, set the ‘W’ bit (in the flags register – 0x00) to ‘1’ to enable writes to alarm registers. After writing the alarm value, clear the ‘W’ bit back to ‘0’ for the changes to take effect.

Note CY14B256P requires the alarm match bit for seconds (0x02 - D7) to be set to ‘0’ for proper operation of alarm flag and Interrupt.

Watchdog Timer

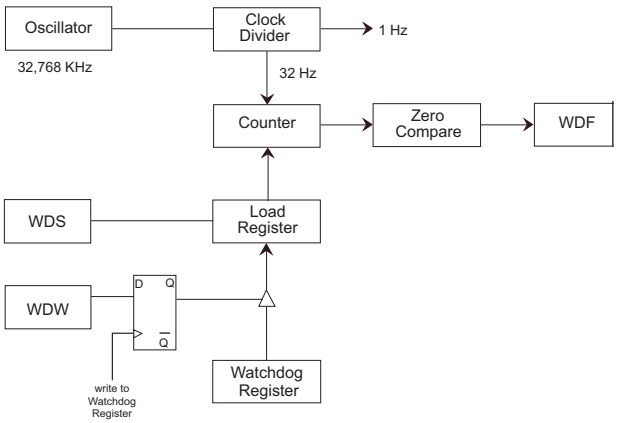
The watchdog timer is a free running down counter that uses the 32-Hz clock (31.25 ms) derived from the crystal oscillator. The oscillator must be running for the watchdog to function. It begins counting down from the value loaded in the Watchdog Timer register.

The timer consists of a loadable register and a free running counter. On power-up, the watchdog time out value in register 0x07 is loaded into the counter load register. Counting begins on power-up and restarts from the loadable value any time the watchdog strobe (WDS) bit is set to ‘1’. The counter is compared to the terminal value of ‘0’. If the counter reaches this value, it causes an internal flag and an optional interrupt output. You can prevent the time out interrupt by setting WDS bit to ‘1’ prior to the counter reaching ‘0’. This causes the counter to reload with the watchdog time out value and to be restarted. As long as the user sets the WDS bit prior to the counter reaching the terminal value, the interrupt and WDT flag never occur.

New time out values are written by setting the watchdog write bit to ‘0’. When the WDW is ‘0’, new writes to the watchdog time out value bits D5-D0 are enabled to modify the time out value. When WDW is ‘1’, writes to bits D5-D0 are ignored. The WDW function enables a user to set the WDS bit without concern that the watchdog timer value is modified. A logical diagram of the watchdog timer is shown in Figure 21 on page 18. Note that setting the watchdog time out value to ‘0’ disables the watchdog function.

The output of the watchdog timer is the flag bit WDF that is set if the watchdog is allowed to time out. If the watchdog interrupt enable (WIE) bit in the interrupt register is set, a hardware interrupt on INT pin is also generated on watchdog timeout. The flag and the hardware interrupt are both cleared when the user reads the flags register.

Figure 21. Watchdog Timer Block Diagram



Power Monitor

The CY14B256P provides a power management scheme with the power fail interrupt capability. It also controls the internal switch to backup power for the clock and protects the memory from low V_{CC} access. The power monitor is based on an internal band gap reference circuit that compares the V_{CC} voltage to V_{SWITCH} threshold.

As described in the section AutoStore Operation on page 4, when V_{SWITCH} is reached as V_{CC} decays from power loss, a data STORE operation is initiated from SRAM to the nonvolatile elements, securing the last SRAM data state. Power is also switched from V_{CC} to the backup supply (battery or capacitor) to operate the RTC oscillator.

When operating from the backup source, read and write operations to nvSRAM are inhibited and the RTC functions are not available to the user. The RTC clock continues to operate in the background. The updated RTC time keeping registers data are available to the user after V_{CC} is restored to the device (see AutoStore or Power-Up RECALL on page 29).

Interrupts

The CY14B256P has a flags register, interrupt register, and Interrupt logic that can signal interrupt to the microcontroller. There are three potential sources for interrupt: watchdog timer, power monitor, and alarm timer. Each of these can be individually enabled to drive the INT pin by appropriate setting in the interrupt register (0x06). In addition, each has an associated flag bit in the flags register (0x00) that the host processor uses to determine the cause of the interrupt. The INT pin driver has two bits that specify its behavior when an interrupt occurs.

An interrupt is raised only if both a flag is raised by one of the three sources and the respective interrupt enable bit in interrupts register is enabled (set to ‘1’). After an interrupt source is active, two programmable bits, H/L and P/L, determine the behavior of the output pin driver on INT pin. These two bits are located in the interrupt register and can be used to drive level or pulse mode output from the INT pin. In pulse mode, the pulse width is internally fixed at approximately 200 ms. This mode is intended to reset a host microcontroller. In the level mode, the pin goes to its active polarity until the flags register is read by the user. This mode is used as an interrupt to a host microcontroller. The control bits are summarized in the following section.

Interrupts are only generated while working on normal power and are not triggered when system is running in backup power mode.

Note CY14B256P generates valid interrupts only after the Power-up RECALL sequence is completed. All events on INT pin must be ignored for t_{FA} duration after powerup.

Interrupt Register

Watchdog Interrupt Enable (WIE): When set to ‘1’, the watchdog timer drives the INT pin and an internal flag when a watchdog time out occurs. When WIE is set to ‘0’, the watchdog timer only affects the WDF flag in flags register.

Alarm Interrupt Enable (AIE): When set to ‘1’, the alarm match drives the INT pin and an internal flag. When AIE is set to ‘0’, the alarm match only affects the AF flag in flags register.

Power Fail Interrupt Enable (PFE): When set to ‘1’, the power fail monitor drives the pin and an internal flag. When PFE is set to ‘0’, the power fail monitor only affects the PF flag in flags register.

High/Low (H/L): When set to a ‘1’, the INT pin is active HIGH and the driver mode is push pull. The INT pin drives HIGH only when V_{CC} is greater than V_{SWITCH}. When set to a ‘0’, the INT pin is active LOW and the drive mode is open drain. The INT pin must be pulled up to Vcc by a 10 k resistor while using the interrupt in active LOW mode.

Pulse/Level (P/L): When set to a ‘1’ and an interrupt occurs, the INT pin is driven for approximately 200 ms. When P/L is set to a ‘0’, the INT pin is driven HIGH or LOW (determined by H/L) until the flags register is read.

When an enabled interrupt source activates the INT pin, an external host reads the flags registers to determine the cause. Remember that all flags are cleared when the register is read. If the INT pin is programmed for level mode, then the condition clears and the INT pin returns to its inactive state. If the pin is programmed for pulse mode, then reading the flag also clears the flag and the pin. The pulse does not complete its specified duration if the flags register is read. If the INT pin is used as a host reset, the flags register is not read during a reset.

Flags Register

The flags register has three flag bits, WDF, AF, and PF, which can be used to generate an interrupt. These flags are set by the watchdog timeout, alarm match, or power fail monitor respectively. The processor can either poll this register or enable interrupts to be informed when a flag is set. These flags are automatically reset after the register is read. The flags register is automatically loaded with the value 0x00 on power-up (except for the OSCF bit. See Stopping and Starting the Oscillator on page 16)

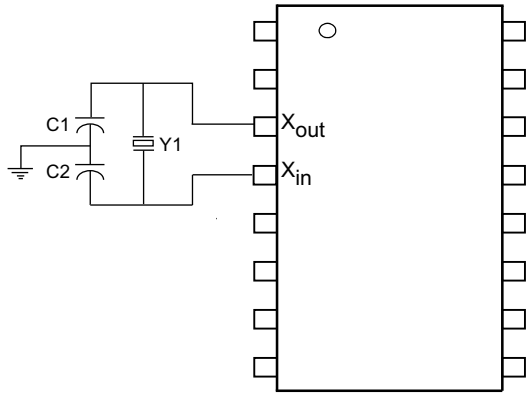
Accessing the Real Time Clock through SPI

CY14B256P uses 16 registers for RTC. These registers can be read out or written to by accessing all 16 registers in burst mode or accessing each register, one at a time. The RDRTC and WRTC instructions are used to access the RTC.

All the RTC registers can be read in burst mode by issuing the RDRTC instruction and reading all 16 bytes without bringing the CS pin HIGH. The 'R' bit must be set while reading the RTC timekeeping registers to ensure that transitional values of time are not read.

Writes to the RTC register are performed using the WRTC instruction. Writing RTC timekeeping registers and control registers, except for the flags register needs the 'W' bit of the flags register to be set to '1'. The internal counters are updated with the new date and time setting when the 'W' bit is cleared to '0'. All the RTC registers can also be written in burst mode using the WRTC instruction.

Figure 22. RTC Recommended Component Configuration

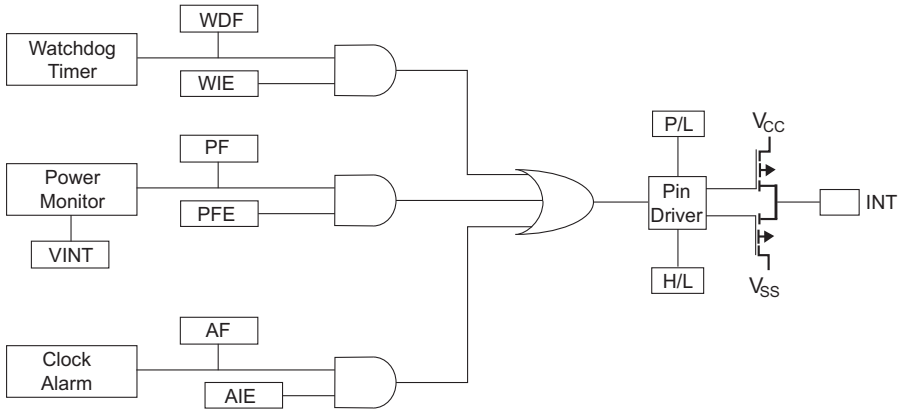


Recommended Values

Y1 = 32.768 KHz (12.5 pF)
C_1 = 10 pF
C_2 = 67 pF

Note: The recommended values for C1 and C2 include board trace capacitance.

Figure 23. Interrupt Block Diagram



WDF - Watchdog Timer Flag
WIE - Watchdog Interrupt Enable
PF - Power Fail Flag
PFE - Power Fail Enable
AF - Alarm Flag
AIE - Alarm Interrupt Enable
P/L - Pulse Level
H/L - High/Low

Table 9. RTC Register Map[2, 3]

Register	BCD Format Data								Function/Range
	D7	D6	D5	D4	D3	D2	D1	D0	
0x0F	10s years				Years				Years: 00–99
0x0E	0	0	0	10s months	Months				Months: 01–12
0x0D	0	0	10s day of month		Day of month				Day of month: 01–31
0x0C	0	0	0	0	0	Day of week			Day of week: 01–07
0x0B	0	0	10s hours		Hours				Hours: 00–23
0x0A	0	10s minutes			Minutes				Minutes: 00–59
0x09	0	10s seconds			Seconds				Seconds: 00–59
0x08	OSCEN (0)	0	Cal sign (0)	Calibration (00000)					Calibration values [4]
0x07	WDS (0)	WDW (0)	WDT (000000)						Watchdog [4]
0x06	WIE (0)	AIE (0)	PFE (0)	0	H/L (1)	P/L (0)	0	0	Interrupts [4]
0x05	M (1)	0	10s alarm date		Alarm, day				Alarm, day of month: 01–31
0x04	M (1)	0	10s alarm hours		Alarm, hours				Alarm, hours: 00–23
0x03	M (1)	10s alarm minutes			Alarm, minutes				Alarm, minutes: 00–59
0x02	M (1)	10s alarm seconds			Alarm, seconds				Alarm, seconds: 00–59
0x01	10s centuries				Centuries				Centuries: 00–99
0x00	WDF	AF	PF	OSCF[5]	0	CAL (0)	W (0)	R (0)	Flags [4]

Notes
2. ( ) designates values shipped from the factory.
3. The unused bits of RTC registers are reserved for future use and should be set to '0'.
4. This is a binary value, not a BCD value.
5. When user resets OSCF flag bit, the flags register will be updated after t_{RTCp} time.

Table 10. Register Map Detail

Register	Description							
0x0F	**Time Keeping - Years**							
	D7	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
	10s years				Years			
	Contains the lower two BCD digits of the year. Lower nibble (four bits) contains the value for years; upper nibble (four bits) contains the value for 10s of years. Each nibble operates from 0 to 9. The range for the register is 0–99.							
0x0E	**Time Keeping - Months**							
	D7	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
	0	0	0	10s month	Months			
	Contains the BCD digits of the month. Lower nibble (four bits) contains the lower digit and operates from 0 to 9; upper nibble (one bit) contains the upper digit and operates from 0 to 1. The range for the register is 1–12.							
0x0D	**Time Keeping - Date**							
	D7	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
	0	0	10s day of month		Day of month			
	Contains the BCD digits for the date of the month. Lower nibble (four bits) contains the lower digit and operates from 0 to 9; upper nibble (two bits) contains the 10s digit and operates from 0 to 3. The range for the register is 1–31. Leap years are automatically adjusted for.							
0x0C	**Time Keeping - Day**							
	D7	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
	0	0	0	0	0	Day of week		
	Lower nibble (three bits) contains a value that correlates to day of the week. Day of the week is a ring counter that counts from 1 to 7 then returns to 1. The user must assign meaning to the day value, because the day is not integrated with the date.							
0x0B	**Time Keeping - Hours**							
	D7	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
	0	0	10s hours		Hours			
	Contains the BCD value of hours in 24 hour format. Lower nibble (four bits) contains the lower digit and operates from 0 to 9; upper nibble (two bits) contains the upper digit and operates from 0 to 2. The range for the register is 0–23.							
0x0A	**Time Keeping - Minutes**							
	D7	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
	0	10s minutes			Minutes			
	Contains the BCD value of minutes. Lower nibble (four bits) contains the lower digit and operates from 0 to 9; upper nibble (three bits) contains the upper minutes digit and operates from 0 to 5. The range for the register is 0–59.							
0x09	**Time Keeping - Seconds**							
	D7	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
	0	10s seconds			Seconds			
	Contains the BCD value of seconds. Lower nibble (four bits) contains the lower digit and operates from 0 to 9; upper nibble (three bits) contains the upper digit and operates from 0 to 5. The range for the register is 0–59.							
0X08	**Calibration/Control**							
	D7	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
	OSCEN	0	Calibration sign	Calibration				
OSCEN	Oscillator enable. When set to ‘1’, the oscillator is stopped. When set to ‘0’, the oscillator runs. Disabling the oscillator saves battery or capacitor power during storage.							
Calibration sign	Determines if the calibration adjustment is applied as an addition (1) to or as a subtraction (0) from the time-base.							
Calibration	These five bits control the calibration of the clock.							

Table 10. Register Map Detail *(continued)*

Register	Description							
0x07	**Watchdog Timer**							
	D7	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
	WDS	WDW	WDT					
WDS	Watchdog strobe. Setting this bit to ‘1’ reloads and restarts the watchdog timer. Setting the bit to ‘0’ has no effect. The bit is cleared automatically after the watchdog timer is reset. The WDS bit is write only. Reading it always returns a ‘0’.							
WDW	Watchdog write enable. Setting this bit to ‘1’ disables any WRITE to the watchdog timeout value (D5–D0). This enables the user to set the watchdog strobe bit without disturbing the timeout value. Setting this bit to ‘0’ allows bits D5–D0 to be written to the watchdog register when the next write cycle is complete. This function is explained in more detail in Watchdog Timer on page 17.							
WDT	Watchdog timeout selection. The watchdog timer interval is selected by the 6-bit value in this register. It represents a multiplier of the 32 Hz count (31.25 ms). The range of timeout value is 31.25 ms (a setting of 1) to 2 seconds (setting of 3 Fh). Setting the watchdog timer register to ‘0’ disables the timer. These bits can be written only if the WDW bit was set to 0 on a previous cycle.							
0x06	**Interrupt Status/Control**							
	D7	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
	WIE	AIE	PFE	0	H/L	P/L	0	0
WIE	Watchdog interrupt enable. When set to ‘1’ and a watchdog timeout occurs, the watchdog timer drives the INT pin and the WDF flag. When set to ‘0’, the watchdog timeout affects only the WDF flag.							
AIE	Alarm interrupt enable. When set to ‘1’, the alarm match drives the INT pin and the AF flag. When set to ‘0’, the alarm match only affects the AF flag.							
PFE	Power fail enable. When set to ‘1’, the alarm match drives the INT pin and the PF flag. When set to ‘0’, the power fail monitor affects only the PF flag.							
0	Reserved for future use							
H/L	HIGH/LOW. When set to ‘1’, the INT pin is driven active HIGH. When set to ‘0’, the INT pin is open drain, active LOW.							
P/L	Pulse/Level. When set to ‘1’, the INT pin is driven active (determined by H/L) by an interrupt source for approximately 200 ms. When set to ‘0’, the INT pin is driven to an active level (as set by H/L) until the flags register is read.							
0x05	**Alarm - Day**							
	D7	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
	M	0	10s alarm date		Alarm date			
	Contains the alarm value for the date of the month and the mask bit to select or deselect the date value.							
M	Match. When this bit is set to ‘0’, the date value is used in the alarm match. Setting this bit to ‘1’ causes the match circuit to ignore the date value.							
0x04	**Alarm - Hours**							
	D7	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
	M	0	10s alarm hours		Alarm hours			
	Contains the alarm value for the hours and the mask bit to select or deselect the hours value.							
M	Match. When this bit is set to ‘0’, the hours value is used in the alarm match. Setting this bit to ‘1’ causes the match circuit to ignore the hours value.							
0x03	**Alarm - Minutes**							
	D7	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
	M	10s alarm minutes			Alarm minutes			
	Contains the alarm value for the minutes and the mask bit to select or deselect the minutes value.							
M	Match. When this bit is set to ‘0’, the minutes value is used in the alarm match. Setting this bit to ‘1’ causes the match circuit to ignore the minutes value.							

Table 10. Register Map Detail *(continued)*

Register	Description							
0x02	**Alarm - Seconds**							
	D7	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
	M	10s alarm seconds			Alarm seconds			
	Contains the alarm value for the seconds and the mask bit to select or deselect the seconds' value.							
M	Match. When this bit is set to '0', the seconds value is used in the alarm match. Setting this bit to '1' causes the match circuit to ignore the seconds value.							
0x01	**Time Keeping - Centuries**							
	D7	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
	10s centuries				Centuries			
	Contains the BCD value of centuries. Lower nibble contains the lower digit and operates from 0 to 9; upper nibble contains the upper digit and operates from 0 to 9. The range for the register is 0-99 centuries.							
0x00	**Flags**							
	D7	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
	WDF	AF	PF	OSCF	0	CAL	W	R
WDF	Watchdog timer flag. This read only bit is set to '1' when the watchdog timer is allowed to reach 0 without being reset by the user. It is cleared to '0' when the flags register is read or on power-up							
AF	Alarm flag. This read only bit is set to '1' when the time and date match the values stored in the alarm registers with the match bits = '0'. It is cleared when the flags register is read or on power-up.							
PF	Power fail flag. This read only bit is set to '1' when power falls below the power fail threshold V_{SWITCH}. It is cleared to 0 when the flags register is read or on power-up.							
OSCF	Oscillator fail flag. Set to '1' on power-up if the oscillator is enabled and not running in the first 5 ms of operation. This indicates that RTC backup power failed and clock value is no longer valid. This bit survives the power cycle and is never cleared internally by the chip. The user must check for this condition and write '0' to clear this flag. When user resets OSCF flag bit, the bit will be updated after t_{RTCp} time.							
CAL	Calibration mode. When set to '1', a 512 Hz square wave is output on the INT pin. When set to '0', the INT pin resumes normal operation. This bit defaults to 0 (disabled) on power-up.							
W	Write enable: Setting the 'W' bit to '1' freezes updates of the RTC registers. The user can then write to RTC registers, alarm registers, calibration register, interrupt register and flags register. Setting the 'W' bit to '0' causes the contents of the RTC registers to be transferred to the time keeping counters if the time has changed. This transfer process takes t_{RTCp} time to complete. This bit defaults to 0 on power-up.							
R	Read enable: Setting 'R' bit to '1', stops clock updates to user RTC registers so that clock updates are not seen during the reading process. Set 'R' bit to '0' to resume clock updates to the holding register. Setting this bit does not require 'W' bit to be set to '1'. This bit defaults to 0 on power-up.							

Best Practices

nvSRAM products have been used effectively for over 27 years. While ease-of-use is one of the product's main system values, experience gained working with hundreds of applications has resulted in the following suggestions as best practices:

- The nonvolatile cells in this nvSRAM product are delivered from Cypress with 0x00 written in all cells. Incoming inspection routines at customer or contract manufacturer's sites sometimes reprogram these values. Final NV patterns are typically repeating patterns of AA, 55, 00, FF, A5, or 5A. End product's firmware should not assume an NV array is in a set programmed state. Routines that check memory content values to determine first time system configuration, cold or warm boot status, and so on should always program a unique NV pattern (that is, complex 4 byte pattern of 46 E6 49 53 hex or more random bytes) as part of the final system manufacturing test to ensure these system routines work consistently.
- Power up boot firmware routines should rewrite the nvSRAM into the desired state (for example, AutoStore enabled). While the nvSRAM is shipped in a preset state, best practice is to again rewrite the nvSRAM into the desired state as a safeguard against events that might flip the bit inadvertently such as program bugs and incoming inspection routines.
- The V_{CAP} value specified in this data sheet includes a minimum and a maximum value size. Best practice is to meet this requirement and not exceed the maximum V_{CAP} value because the nvSRAM internal algorithm calculates V_{CAP} charge and discharge time based on this maximum V_{CAP} value. Customers that want to use a larger V_{CAP} value to make sure there is extra STORE charge and STORE time should discuss their V_{CAP} size selection with Cypress to understand any impact on the V_{CAP} voltage level at the end of a t_{RECALL} period.
- When base time is updated, these updates are transferred to the time keeping registers when 'W' bit is set to '0'. This transfer takes t_{RTCp} time to complete. It is recommended to initiate software STORE or Hardware STORE after t_{RTCp} time to save the base time into nonvolatile memory.

Maximum Ratings

Exceeding maximum ratings may shorten the useful life of the device. These user guidelines are not tested.

Storage temperature ..... –65 °C to +150 °C

Maximum accumulated storage time

At 150 °C ambient temperature..... ..... 1000 h

At 85 °C ambient temperature..... 20 Years

Ambient temperature with power applied ..... –55 °C to +150 °C

Supply voltage on V_{CC} relative to V_{SS}.....–0.5 V to +4.1 V

DC voltage applied to outputs in high Z state ..... –0.5 V to V_{CC} + 0.5 V

Input voltage ..... –0.5 V to V_{CC} + 0.5 V

Transient voltage (< 20 ns) on any pin to ground potential ..... –2.0 V to V_{CC} + 2.0 V

Package power dissipation capability (T_A = 25 °C) ..... 1.0 W

Surface mount lead soldering temperature (3 Seconds)..... +260 °C

DC output current (1 output at a time, 1 s duration). ... 15 mA

Static discharge voltage..... > 2001 V (per MIL-STD-883, method 3015)

Latch up current..... > 200 mA

Operating Range

Range	Ambient Temperature	V_{CC}
Industrial	–40 °C to +85 °C	2.7 V to 3.6 V

DC Electrical Characteristics

Over the Operating Range

Parameter	Description	Test Conditions	Min	Typ[6]	Max	Unit
V_{CC}	Power supply voltage		2.7	3.0	3.6	V
I_{CC1}	Average V_{cc} current	At f_{SCK} = 40 MHz. Values obtained without output loads (I_{OUT} = 0 mA)	–	–	10	mA
I_{CC2}	Average V_{CC} current during STORE	All inputs don't care, V_{CC} = Max Average current for duration t_{STORE}	–	–	10	mA
I_{CC4}	Average V_{CAP} current during AutoStore cycle	All inputs don't care. Average current for duration t_{STORE}	–	–	5	mA
I_{SB}	V_{CC} standby current	$\overline{CS} \geq (V_{CC} – 0.2\ V)$. $V_{IN} \leq 0.2$ V or $\geq (V_{CC} – 0.2\ V)$. W bit set to '0'. Standby current level after nonvolatile cycle is complete. Inputs are static. f = 0 MHz.	–	–	5	mA
I_{IX}[7]	Input leakage current (except $\overline{HSB}$)	V_{CC} = Max, $V_{SS} \leq V_{IN} \leq V_{CC}$	–1	–	+1	µA
	Input leakage current (for $\overline{HSB}$)	V_{CC} = Max, $V_{SS} \leq V_{IN} \leq V_{CC}$	–100	–	+1	µA
I_{OZ}	Off state output leakage current	V_{CC} = Max, $V_{SS} \leq V_{OUT} \leq V_{CC}$	–1	–	+1	µA
V_{IH}	Input HIGH voltage		2.0	–	V_{CC} + 0.5	V
V_{IL}	Input LOW voltage		V_{SS} – 0.5	–	0.8	V
V_{OH}	Output HIGH voltage	I_{OUT} = –2 mA	2.4	–		V
V_{OL}	Output LOW voltage	I_{OUT} = 4 mA	–	–	0.4	V
V_{CAP}[8]	Storage capacitor	Between V_{CAP} pin and V_{SS}, 5 V rated	61	68	180	µF

Notes

6. Typical values are at 25 °C, V_{CC}= V_{CC} (Typ). Not 100% tested.
7. The $\overline{HSB}$ pin has I_{OUT} = –2 µA for V_{OH} of 2.4 V when both active HIGH and LOW drivers are disabled. When they are enabled standard V_{OH} and V_{OL} are valid. This parameter is characterized but not tested.
8. Min V_{CAP} value guarantees that there is a sufficient charge available to complete a successful AutoStore operation. Max V_{CAP} value guarantees that the capacitor on V_{CAP} is charged to a minimum voltage during a Power-Up RECALL cycle so that an immediate power-down cycle can complete a successful AutoStore. Therefore it is always recommended to use a capacitor within the specified min and max limits. Refer application note AN43593 for more details on V_{CAP} options.

Data Retention and Endurance

Over the Operating Range

Parameter	Description	Min	Unit
$DATA_R$	Data retention	20	Years
NV_C	Nonvolatile STORE operations	1,000	K

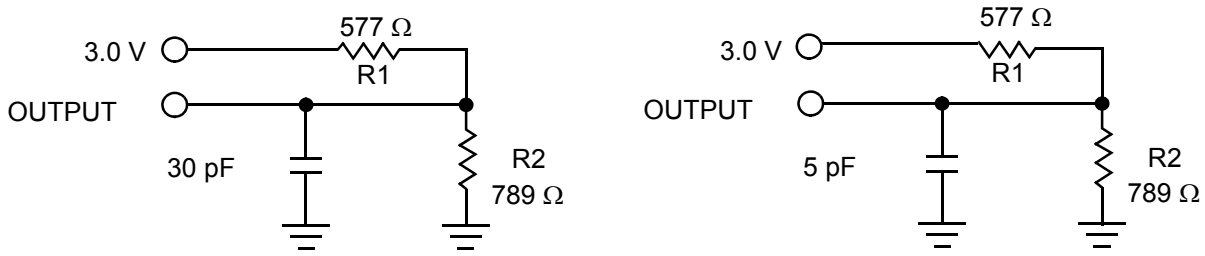
Capacitance

Parameter[9]	Description	Test Conditions	Max	Unit
C_{IN}	Input capacitance	T_A = 25 °C, f = 1 MHz, V_{CC} = V_{CC} (Typ)	6	pF
C_{OUT}	Output pin capacitance		8	pF

Thermal Resistance

Parameter[9]	Description	Test Conditions	16-SOIC	Unit
θ_{JA}	Thermal resistance (junction to ambient)	Test conditions follow standard test methods and procedures for measuring thermal impedance, per EIA / JESD51.	55.17	°C/W
θ_{JC}	Thermal resistance (junction to case)		2.64	°C/W

Figure 24. AC Test Loads and Waveforms



AC Test Conditions

Input pulse levels..... 0 V to 3 V
Input rise and fall times (10% to 90%)..... ≤ 3 ns
Input and output timing reference levels..... 1.5 V

Note
9. These parameters are guaranteed by design and are not tested.

RTC Characteristics

Over the Operating Range

Parameter	Description		Min	Typ[10]	Max	Units
V_{RTCbat}	RTC battery pin voltage		1.8	3.0	3.6	V
I_{BAK}[11]	RTC backup current	T_A (Min)	–	–	0.35	µA
		25 °C	–	0.35	–	µA
		T_A (Max)	–	–	0.5	µA
V_{RTCcap}[12]	RTC capacitor pin voltage	T_A (Min)	1.6	–	3.6	V
		25 °C	1.5	3.0	3.6	V
		T_A (Max)	1.4	–	3.6	V
tOCS	RTC oscillator time to start		–	1	2	sec
t_{RTCp}	RTC processing time from end of ‘W’ bit set to ‘0’		–	–	350	µs
R_{BKCHG}	RTC backup capacitor charge current-limiting resistor		350	–	850	Ω

AC Switching Characteristics

Over the Operating Range[13]

Cypress Parameter	Alt. Parameter	Description	40 MHz		25 MHz (RDRTC Instruction)[14]		Unit
			Min	Max	Min	Max	
f_{SCK}	f_{SCK}	Clock frequency, SCK	–	40	–	25	MHz
t_{CL}	t_{WL}	Clock pulse width LOW	11	–	18	–	ns
t_{CH}	t_{WH}	Clock pulse width HIGH	11	–	18	–	ns
t_{CS}	t_{CE}	$\overline{CS}$ HIGH time	20	–	20	–	ns
t_{CSS}	t_{CES}	$\overline{CS}$ setup time	10	–	10	–	ns
t_{CSH}	t_{CEH}	$\overline{CS}$ hold time	10	–	10	–	ns
t_{SD}	t_{SU}	Data in setup time	5	–	5	–	ns
t_{HD}	t_{H}	Data in hold time	5	–	5	–	ns
t_{HH}	t_{HD}	$\overline{HOLD}$ hold time	5	–	5	–	ns
t_{SH}	t_{CD}	$\overline{HOLD}$ setup time	5	–	5	–	ns
t_{CO}	t_{V}	Output valid	–	9	–	15	ns
t_{HHZ}[15]	t_{HZ}	$\overline{HOLD}$ to output high Z	–	15	–	15	ns
t_{HLZ}[15]	t_{LZ}	$\overline{HOLD}$ to output low Z	–	15	–	15	ns
t_{OH}	t_{HO}	Output hold time	0	–	0	–	ns
t_{HZCS}	t_{DIS}	Output disable time	–	25		25	ns

Notes
10. Typical values are at 25 °C, V_{CC}= V_{CC} (Typ). Not 100% tested.
11. Current drawn from either V_{RTCcap} or V_{RTCbat} when V_{CC} < V_{SWITCH}.
12. If V_{RTCcap} > 0.5 V or if no capacitor is connected to V_{RTCcap} pin, the oscillator starts in tOCS time. If a backup capacitor is connected and V_{RTCcap} < 0.5 V, the capacitor must be allowed to charge to 0.5 V for oscillator to start.
13. Test conditions assume signal transition time of 3 ns or less, timing reference levels of V_{CC}/2, input pulse levels of 0 to V_{CC} (typ), and output loading of the specified I_{OL}/I_{OH} and load capacitance shown in Figure 24.
14. Applicable for RTC opcode cycles, address cycles, and dataout cycles.
15. These parameters are guaranteed by design and are not tested.

Figure 25. Synchronous Data Timing (Mode 0)

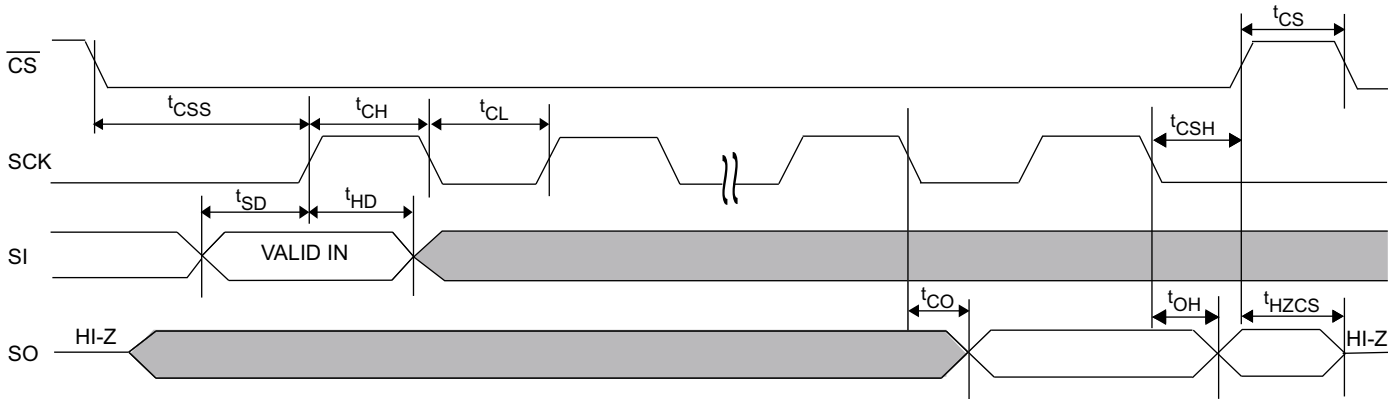
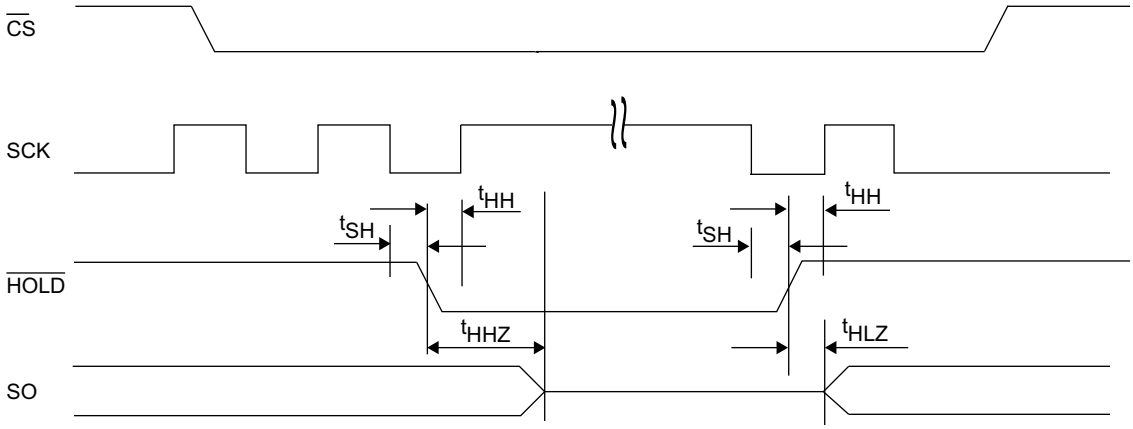


Figure 26. HOLD Timing



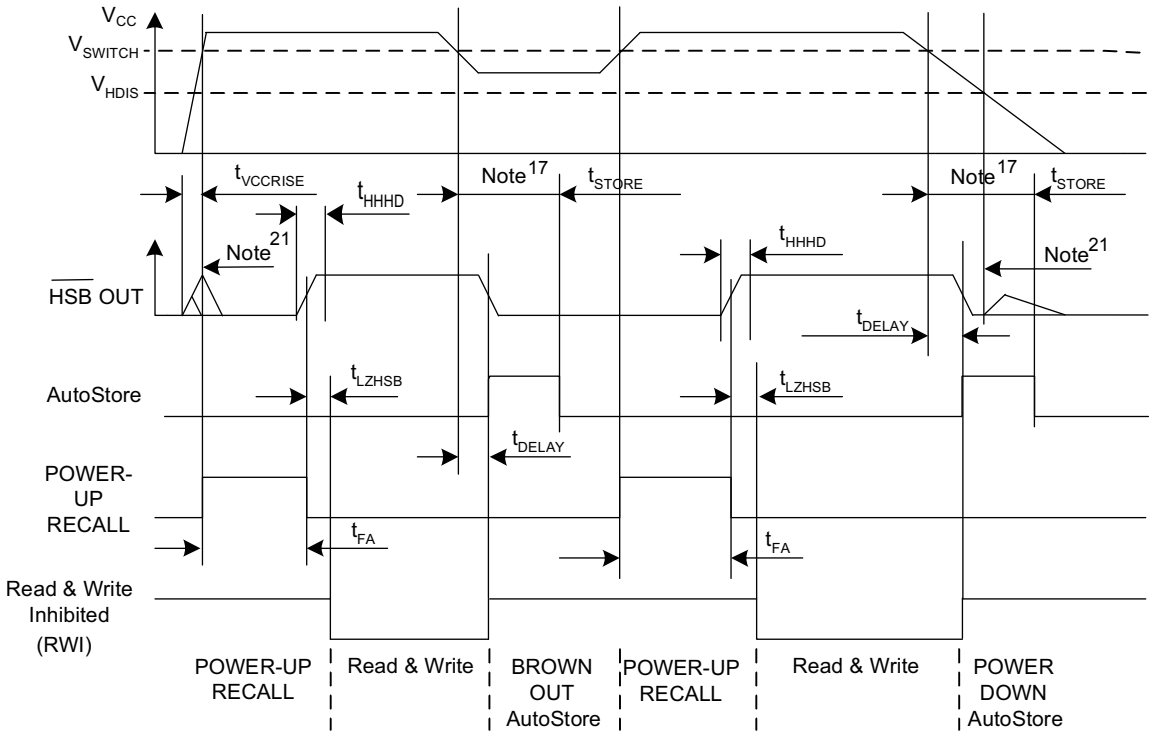
AutoStore or Power-Up RECALL

Over the Operating Range

Parameter	Description	CY14B256P		Unit
		Min	Max	
t_{FA} [16]	Power-Up RECALL duration	–	20	ms
t_{STORE} [17]	STORE cycle duration	–	8	ms
t_{DELAY} [18]	Time allowed to complete SRAM write cycle	–	25	ns
V_{SWITCH}	Low voltage trigger level	–	2.65	V
$t_{VCCRISE}$ [19]	V_{CC} rise time	150	–	µs
V_{HDIS} [19]	$\overline{HSB}$ output disable voltage	–	1.9	V
t_{LZHSB} [19]	$\overline{HSB}$ high to nvSRAM active time	–	5	µs
t_{HHHD} [19]	$\overline{HSB}$ high active time	–	500	ns

Switching Waveforms

Figure 27. AutoStore or Power-Up RECALL[20]



Notes

16. t_{FA} starts from the time V_{CC} rises above V_{SWITCH}.
17. If an SRAM write has not taken place since the last nonvolatile cycle, no AutoStore or Hardware STORE takes place.
18. On a Hardware STORE and AutoStore initiation, SRAM write operation continues to be enabled for time t_{DELAY}.
19. These parameters are guaranteed by design and are not tested.
20. Read and Write cycles are ignored during STORE, RECALL, and while V_{CC} is below V_{SWITCH}.
21. During power up and power down, $\overline{HSB}$ glitches when $\overline{HSB}$ pin is pulled up through an external resistor.

Software Controlled STORE/RECALL Cycles

Over the Operating Range

Parameter	Description	CY14B256P		Unit
		Min	Max	
t_{RECALL}	RECALL duration	–	200	µs
t_{SS} [22, 23]	Soft sequence processing time	–	100	µs

Figure 28. Software STORE Cycle[23]

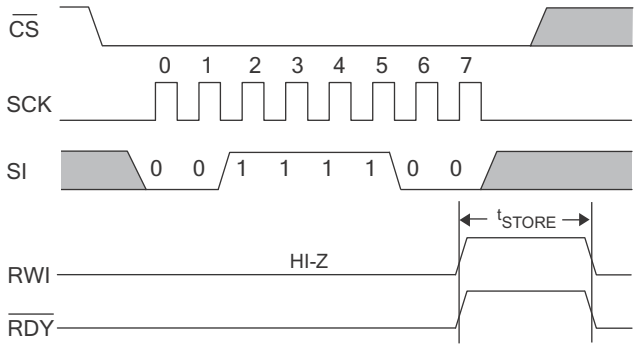


Figure 29. Software RECALL Cycle[23]

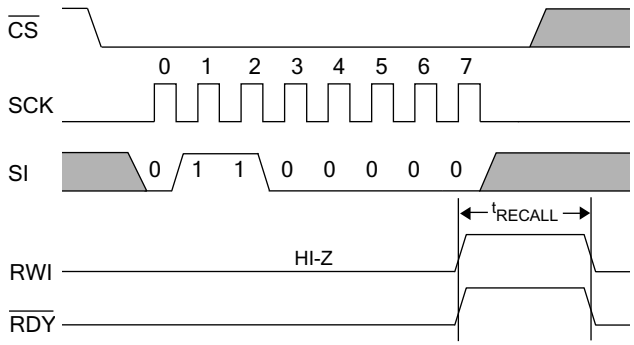


Figure 30. AutoStore Enable Cycle

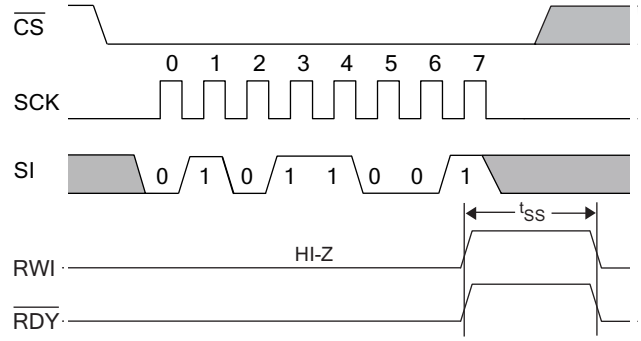
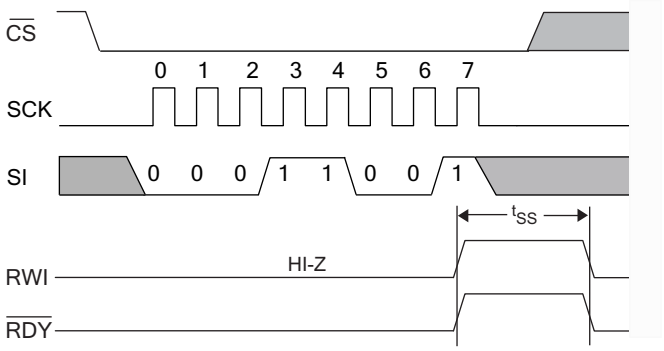


Figure 31. AutoStore Disable Cycle



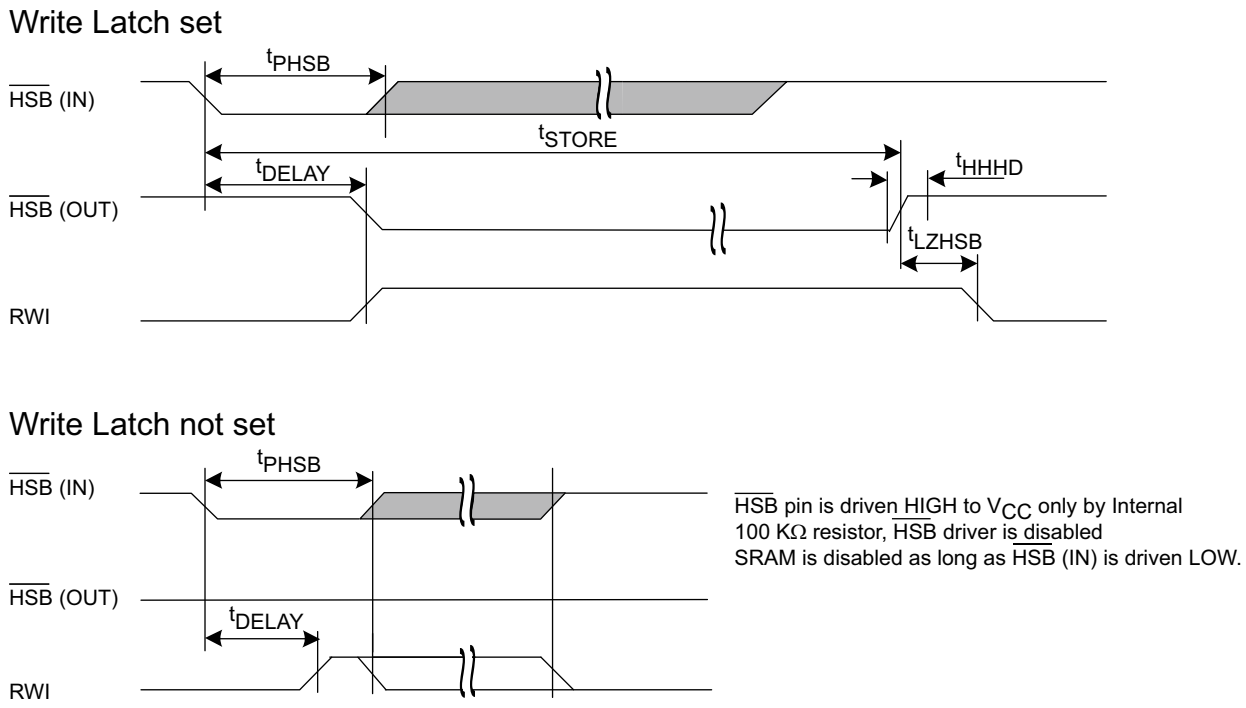
Notes
22. This is the amount of time it takes to take action on a soft sequence command. Vcc power must remain HIGH to effectively register command.
23. Commands such as STORE and RECALL lock out I/O until operation is complete which further increases this time. See the specific command.

Hardware STORE Cycle

Over the Operating Range

Parameter	Description	CY14B256P		Unit
		Min	Max	
t_{PHSB}	Hardware STORE pulse width	15	–	ns

Figure 32. Hardware STORE Cycle[24]



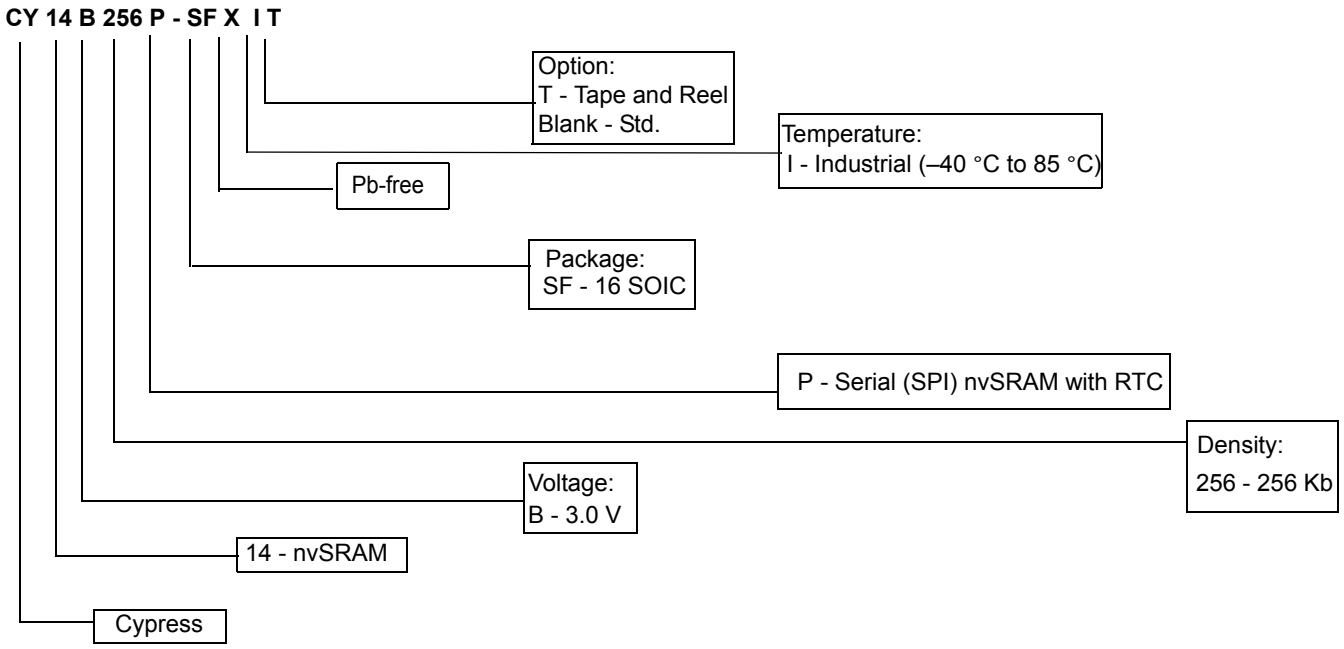
Note
24. If an SRAM write has not taken place since the last nonvolatile cycle, no AutoStore or Hardware STORE takes place.

Ordering Information

Ordering Code	Package Diagram	Package Type	Operating Range
CY14B256P-SFXIT	51-85022	16-pin SOIC	Industrial
CY14B256P-SFXI			

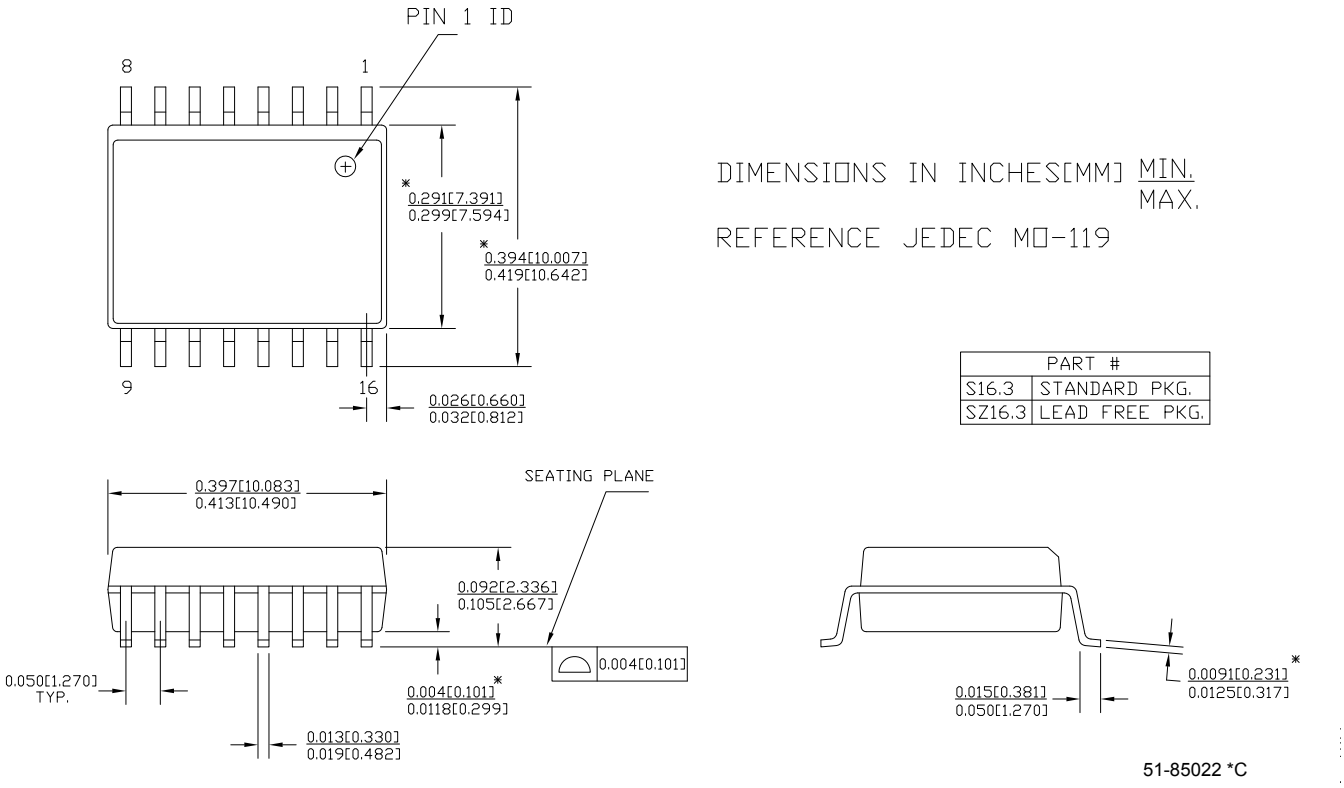
All the above parts are Pb-free.

Ordering Code Definition



Package Diagram

Figure 33. 16-pin (300 mil) SOIC Package



Acronyms

Acronym	Description
BCD	Binary coded decimal
CMOS	Complementary metal oxide semiconductor
CRC	Cyclic redundancy check
CPHA	Clock phase
CPOL	Clock polarity
EEPROM	Electrically erasable programmable read-only memory
EIA	Electronic Industries Alliance
I/O	Input/output
JEDEC	Joint Electron Devices Engineering Council
nvSRAM	nonvolatile static random access memory
RoHS	Restriction of hazardous substances
RWI	Read and write inhibited
SOIC	Small outline integrated circuit
SONOS	Silicon-oxide-nitride-oxide-silicon
SPI	Serial peripheral interface

Document Conventions

Units of Measure

Symbol	Unit of Measure
°C	degree Celsius
Hz	Hertz
KΩ	kilo ohm
µA	micro Amperes
µF	micro Farad
µs	micro second
mA	milli Amperes
MHz	Mega Hertz
ns	nano seconds
Ω	ohm
pF	pico Farad
V	Volts
W	Watts

Document History Page

Document Title: CY14B256P 256-Kbit (32 K x 8) Serial (SPI) nvSRAM with Real Time Clock Document Number: 001-53881				
Revision	**ECN**	**Orig. of Change**	**Submission Date**	**Description of Change**
**	2733272	GVCH/AESA	07/16/09	New Datasheet
*A	2758444	GVCH	09/01/09	Moved data sheet status from preliminary to Final Removed commercial temperature related specs Added thermal resistance values for 16-SOIC package Added note to Write Sequence (WRITE) description Changed V_{RTCbat} max value from 3.3 V to 3.6 V Changed R_{BKCHG} min value from 450 Ω to 350 Ω Updated footnote 8
*B	2839453	GVCH/PYRS	01/06/10	Changed STORE cycles to QuantumTrap from 200 K to 1 Million Updated Figure 2 Updated I_{BAK} RTC backup current spec unit from nA to µA Added Contents
*C	3008637	GVCH	08/16/10	Changed ground naming convention from GND to V_{SS} Table 1: Added more clarity on $\overline{HSB}$ pin operation Hardware STORE and HSB Pin Operation: Added more clarity on $\overline{HSB}$ pin operation Updated Power-Down description Power On Reset: Added status of bits 4-6 Table 4: Added definition of bits 4-6 Updated Figure 7, Figure 25, Figure 26, and Figure 27 Updated footnote 19 Added Figure 30 and Figure 31 Removed t_{DHSB} parameter Updated Figure 32 Updated Package Diagram Added Acronyms and Document Conventions.
*D	3033665	GVCH	09/24/10	Added watermark as “For Evaluation Samples only. Production will be supported with the next revision silicon in SOIC package.” Updated HOLD Pin Operation, Figure 20 and Figure 26 to indicate that $\overline{CS}$ pin must remain LOW along with HOLD pin to pause serial communication.
*E	3143330	GVCH	01/17/11	Hardware STORE and HSB Pin Operation: Added more clarity on $\overline{HSB}$ pin operation Updated Setting the Clock description Updated ‘W’ bit description in Register Map Detail table Updated Best Practices Added t_{RTCp} parameter to RTC Characteristics table Updated t_{LZHSB} parameter description Fixed typo in Figure 27.
*F	3320715	GVCH	07/19/11	Added footnote 8 and 13.

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