BIPOLAR ANALOG INTEGRATED CIRCUIT

NEC ELECTRON DEVICE

μPC1820

COLOR TV/VTR PLL IF SIGNAL PROCESSING IC

The μPC1820 is a semiconductor integrated circuit for processing the color TV/VTR PIF/SIF signals. This IC is housed in a 30-pin shrink dual-in-line package (DIP). Its main features are supported by the built-in keyed-pulse generator circuit needed for the L-SECAM, the VTR-oriented EQ amplifier, the SECAM-L/PAL B/G switch, the PLL VCO circuit, and the split sound carrier output.

FEATURES

- SECAM-L system (keyed AGC) and PAL B/G system (peak AGC) application.
- For SECAM L system, the built-in keying pulse generator circuit realizes the VTR application which has no FBP.
- Good DG, DP characteristics is realized by the PLL system video detection circuit.
- Video equalizer circuit for VTR application.
- Split-carrier system realizes high audio-sensitivity and good S/buzz characteristics.
- Built-in Mute detection circuit
- AFT polarity switching circuit is provided.
- Supply voltage 9 V
- Power consumption 477 mW

ORDERING INFORMATION

Part number	Package	Quality Grade
μPC1820CA	30 pin plastic shrink DIP (400 mil)	Standard

Please refer to "Quality grade on NEC Semiconductor Devices" (Document number IEI-1209) published by NEC Corporation to know the specification of quality grade on the devices and its recommended applications.
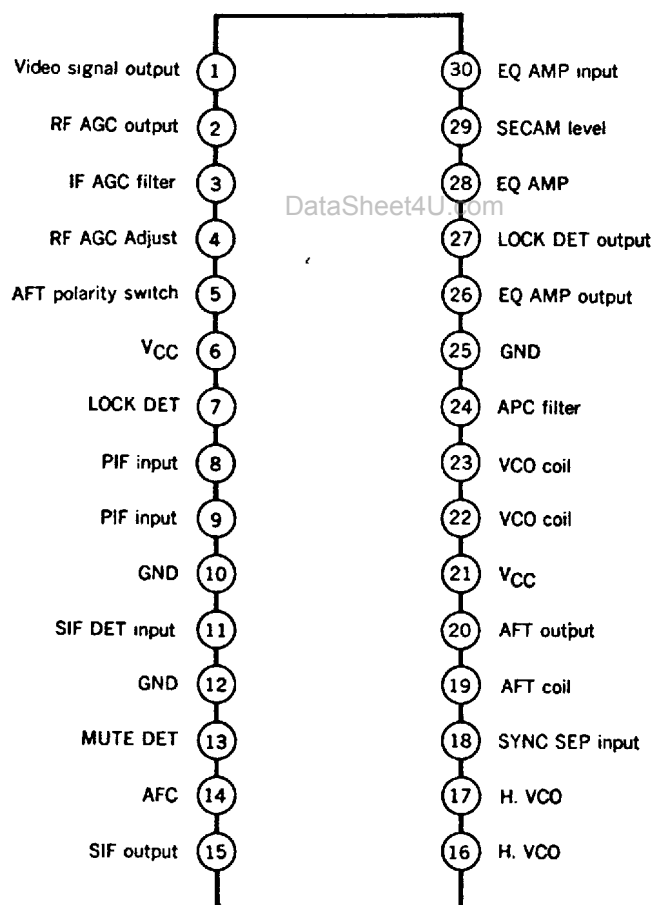
BLOCK DIAGRAM

© NEC Corporation 1988
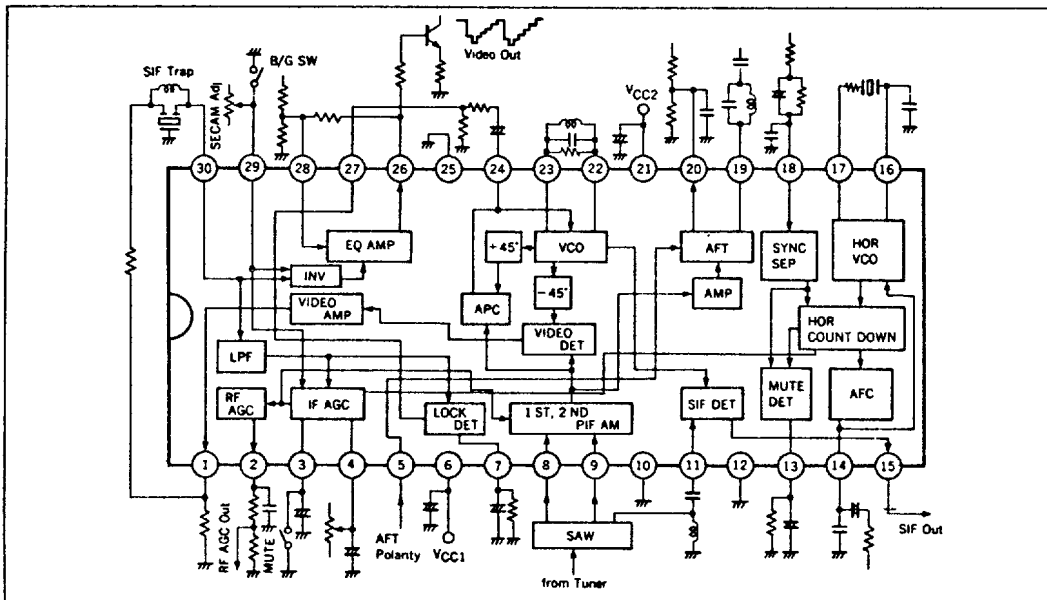
ABSOLUTE MAXIMUM RATINGS ($T_a = 25\,°C$)

Supply Voltage	V_{CC}	11	V
Control Voltage	V_{29}	7	V
AFT Control Voltage	V_5	V_{CC}	V
Power Dissipation	P_D	590 ($T_a = 75\,°C$)	mW
Operating Temperature Range	T_{opt}	-20 to $+75$	$°C$
Storage Temperature Range	T_{stg}	-40 to $+125$	$°C$

RECOMMENDED OPERATING RANGE ($T_a = 25\,°C$)

CHARACTERISTIC	SYMBOL	RECOMMENDED VALUE	UNIT
Supply Voltage	V_{CC}	8.0 to 9.0 to 10.0	V
Control Voltage (B/G)	V_{29L}	0 to 1.0	V
Control Voltage (L)	V_{29H}	3.0 to 5.0	V
AFT Control Voltage (1)	V_{5L}	0 to 1.7	V
AFT Control Voltage (2)	V_{5H}	3.7 to 8	V

PIN CONNECTION (Top View)

Video signal output (1)	(30) EQ AMP input
RF AGC output (2)	(29) SECAM level
IF AGC filter (3)	(28) EQ AMP
RF AGC Adjust (4)	(27) LOCK DET output
AFT polarity switch (5)	(26) EQ AMP output
V_{CC} (6)	(25) GND
LOCK DET (7)	(24) APC filter
PIF input (8)	(23) VCO coil
PIF input (9)	(22) VCO coil
GND (10)	(21) V_{CC}
SIF DET input (11)	(20) AFT output
GND (12)	(19) AFT coil
MUTE DET (13)	(18) SYNC SEP input
AFC (14)	(17) H. VCO
SIF output (15)	(16) H. VCO

2

ELECTRICAL RATINGS (T$_a$ = 25 ±3 °C, RH ≤ 70 %, unless otherwise specified)

Characteristic	Symbol	MIN.	TYP.	MAX.	UNIT	Test conditions
Circuit current	I$_{CC}$	42	53	68	mA	No signal (L mode)
Video detection output voltage 1	V$_0$(B)	1.6	1.9	2.4	V$_{p-p}$	V$_{ip}$ = 90 dBμ, f$_o$ = 32.7 MHz, and video modulation is 87.5 %. (B/G mode)
Video detection output voltage 2	V$_0$(L)		2.0		V$_{p-p}$	V$_{ip}$ = 90 dBμ, f$_O$ = 32.7 MHz, and video modulation is 94 %. (L mode)
Video detection output DC voltage 1	V$_1$(B)	4.8	5.0	5.3	V	No signal (B/G mode)
Video detection output DC voltage 2	V$_1$(L)	4.8	5.0	5.2	V	No signal (L mode)
Video detection output DC voltage 3	V$_{26}$(B)	5.1	5.5	6.0	V	No signal (B/G mode)
Video detection output DC voltage 4	V$_{26}$(L)	2.4	2.8	3.2	V	No signal (L mode)
Video S/N	P/N	47	52		dB	V$_i$ = 90 dBμ (L mode)
Video frequency characteristics	BW(B)	6.0	8.0		MHz	Modulated frequency when V$_o$(P) has decreased by 3 dB due to a change of the input IF modulated signal.
Input sensitivity	V$_{ip}$SENSE		49	53	dBμ	Input voltage when V$_o$(P) has decreased by 3 dB as the input IF voltage was gradually reduced. (L mode)
Premissible maximum input	V$_{ip}$MAX.	105			dBμ	Input voltage when V$_o$(P) was increased by 1 dB as the input IF voltage was gradually reduced. (L mode)
AFT detector sensitivity 1	μ-1	60	90		mV/kHz	Black video signal at V$_{ip}$ = 90 dBμ (B/G mode) and AFT polarity (Pin 5) = L.
Maximum AFT voltage 1	V$_{20H}$-1	8.0	8.7		V	Black video signal at V$_{ip}$ = 90 dBμ (B/G mode) and AFT polarity (Pin 5) = L.
Minimum AFT voltage 1	V$_{20L}$-1		0.24	0.8	V	Black video signal at V$_{ip}$ = 90 dBμ (B/G mode) and AFT polarity (Pin 5) = L.
AFT defeat voltage	V$_{20TH}$	4.3	4.7	5.3	V	Black video signal: V$_{ip}$ = 90 dBμ (B/G mode)
AFT defeat current	I$_{19DEF}$	290	340	390	μA	Current that flows from pin 19 at AFT defeat
AFT polarity threshold voltage	V$_{5TH}$	2.2	2.7	3.2	V	Voltage of pin 5 when the output of pin 20 is reversed
AFT detector sensitivity 2	μ-2	91	108	119	%	Black video signal: V$_{ip}$ = 90 dBμ (B/G mode) and AFT polarity (Pin 5) = H. The ratio of μ-1/μ-2
Maximum AFT voltage 2	V$_{20H}$-2	8.0	8.7		V	Black video signal: V$_{ip}$ = 90 dBμ (B/G mode) and AFT polarity (Pin 5) = H.
Minimum AFT voltage 2	V$_{20L}$-2		0.24	0.8	V	Black video signal: V$_{ip}$ = 90 dBμ (B/G mode) and AFT polarity (Pin 5) = H.
IF AGC minimum voltage	V$_{3H}$	8.2	8.6		V	No input (L mode)
IF AGC minimum voltage	V$_{3L}$	3.0	3.2	3.4	V	Voltage of pin 3 at maximum input (L mode)
Maximum RF AGC voltage	V$_{2H}$	7.0	8.0		V	V$_{ip}$ = 90 dBμ, f$_o$ = 32.7 MHz (B/G mode) video modulation is 87.5 %, and APL = 50 %.
Minimum RF AGC voltage	V$_{2L}$		0	0.5	V	V$_{ip}$ = 90 dBμ, f$_o$ = 32.7 MHz (B/G mode) video modulation is 87.5 %, and APL = 50 %.
Cap challenge (Upper 1)	f$_{CLU}$-1	0.5	1.49		MHz	V$_{ip}$ = 90 dBμ, f$_o$ = 32.7 MHz, video modulation is 87.5 %, APL = 50 %, and Lock SW = OFF (B/G mode)
Cap challenge (Lower 1)	f$_{CLL}$-1	1.25	1.64		MHz	V$_{ip}$ = 90 dBμ, f$_o$ = 32.7 MHz, video modulation is 87.5 %, APL = 50 %, and Lock SW = OFF (B/G mode)

Characteristic	Symbol	MIN.	TYP.	MAX.	UNIT	Test conditions
Cap challenge (Upper 2)	f_{COU-2}	0.5	1.49		MHz	V_{ip} = 90 dBμ, f_O = 32.7 MHz video modulation is 87.5 %, APL = 50 %, and Lock SW = ON (B/G mode)
Cap challenge (Lower 2)	f_{CLL-2}	1.20	1.49		MHz	V_{ip} = 90 dBμ, f_O = 32.7 MHz, video modulation is 87.5 %, APL = 50 %, and Lock SW = ON (B/G mode)
Lock detection threshold voltage	V_{7th}	3.9	4.2	4.5	V	Pin 29 is grounded. (B/G mode)
EQ frequency characteristics 1	FC1		2.6		dB	32.7 MHz +0.5 MHz mixed waves (B/G mode)
EQ frequency characteristics 2	FC2		4.7		dB	32.7 MHz +3.43 MHz mixed waves (B/G mode)
EQ frequency characteristics 3	FC3		7.5		dB	32.7 MHz +4.43 MHz mixed waves (B/G mode)
Intermodulation	IM	30	35		dB	CW compound frequency of 32.7 MHz, 37.13 MHz, and 38.2 MHz is input as the PIF input. (B/G mode)
Differential gain	DG		2	5	%	V_{ip} = 90 dBμ, f_O = 32.7 MHz, in the standard 10 step frequency modulation. (B/G mode)
Differential phase	DP		2	5	deg.	V_{ip} = 90 dBμ, f_O = 32.7 MHz, in the standard 10 step frequency modulation. (B/G mode)
SYNC chip level 1	$V_{sync(B)}$	3.0	3.4	3.8	V	V_{ip} = 90 dBμ, f_O = 32.7 MHz (B/G mode), 87.5 % video modulation, and APL = 50 %.
SYNC chip level 2	$V_{sync(L)}$	2.5	2.9	3.2	V	V_{ip} = 90 dBμ, f_O = 32.7 MHz (L-SECAM) 94 % video modulation, and APL = 50 %.
PAL sync ratio	$SR_{(B)}$	26	29	32	%	(Black level − sync level)/V_O(P) x 100 (B/G mode)
SECAM sync ratio	$SR_{(L)}$	28	30	32	%	(Black level − sync level)/2 x 100 (L mode)
Input resistance	$R_{in(V)}$		1		kΩ	
Input capacitance	$C_{in(V)}$		4		pF	
Horizontal oscillation starting voltage	V_{ccmin}		4	5.0	V	
Horizontal free run frequency	f_H	15.25	15.625	16.0	kHz	
Horizontal pulling range	f_{PL}	310	445		Hz	V_{ip} = 90 dBμ (L mode)
Horizontal pulling range	f_{PH}	374	423		Hz	V_{ip} = 90 dBμ (L mode)
G/L switch threshold level	V_{TH}	1.5	2.0	2.5	V	Voltage of pin 29 when the video output is reversed.
SECAM AFT detector sensitivity	μ-S	60	90		mV/kHz	V_{ip} = 90 dBμ, f_O = 32.7 MHz (L mode), 94 % video modulation, and white = 100 %.
Maximum AFT voltage S	V_{20H-S}	8.0	8.7		V	V_{ip} = 90 dBμ, f_O = 32.7 MHz (L mode), 94 % video modulation, and white = 100 %.
Minimum AFT voltage S	V_{20L-S}		0.24	0.80	V	V_{ip} = 90 dBμ, f_O = 32.7 MHz (L mode), 94 % video modulation, and white = 100 %.
RF AGC temperature characteristics	RFAGC ΔTa		3	6	dB	V_{ip} = 90 dBμ, f_O = 32.7 MHz, 87.5 % video modulation, and APL = 50 %.
SIF DET input sensitivity	V_{is}SENSE		69	73	dBμ	V_{ip} = 90 dBμ SIF input voltage when V_O(S) has decreased by 3 dB as the input SIF voltage was gradually reduced.
SIF DET maximum output voltage	V_O(S)	158 104	282 109	502 114	mV dBμ	V_{ip} = 90 dBμ SIF output voltage when V_O(S) has limited by the SIF input voltage was gradually increased.
Horizontal oscillation output voltage	V_O(H)	0.60	0.70	0.80	V_{p-p}	Pin 17 output voltage when horizontal free-running frequency.

4

MEASURING CIRCUIT 1

MEASURING CIRCUIT 2

6
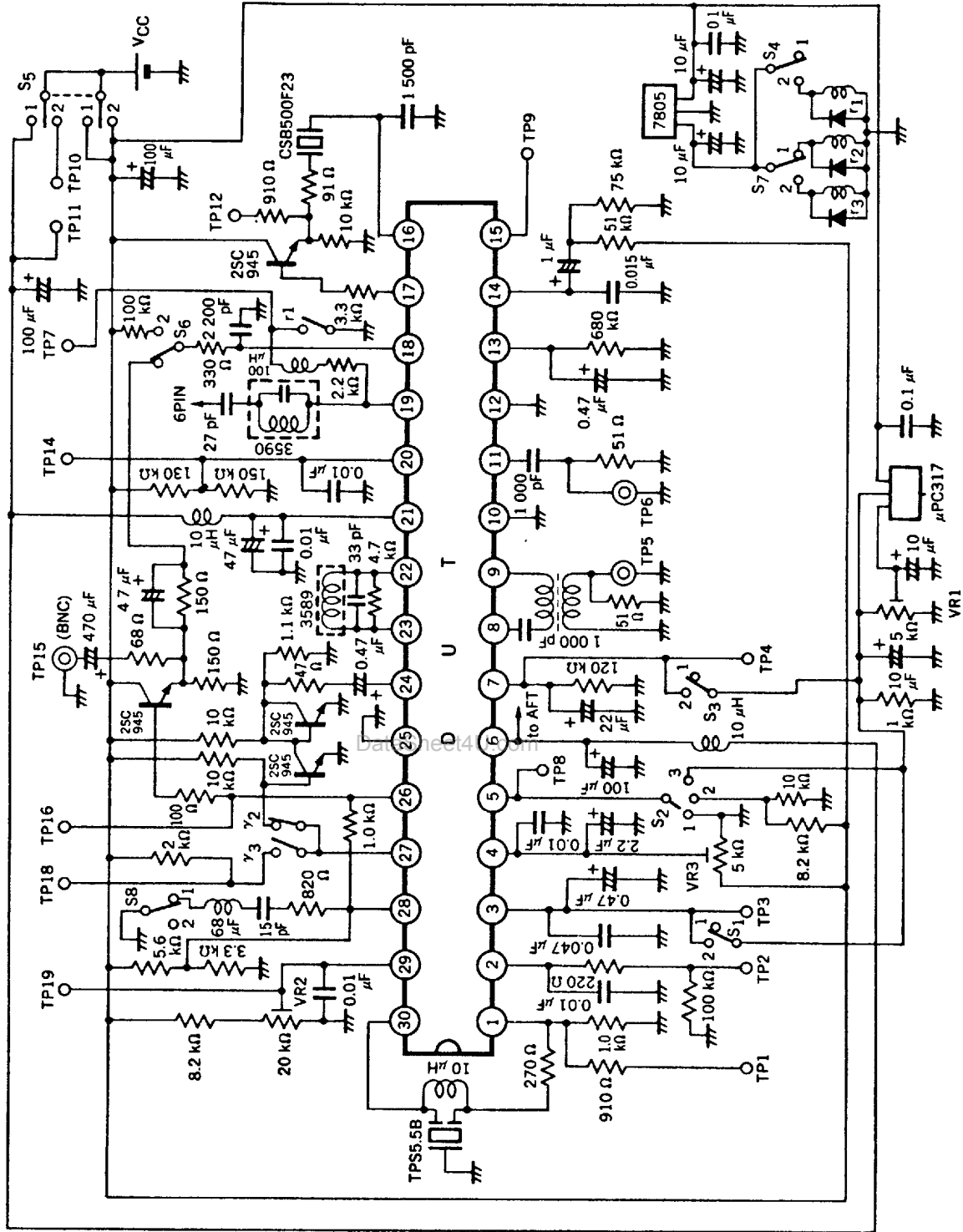
MEASURING CIRCUIT SWITCHES

No.	Symbol	Measuring circuit	S1	S2	S3	S4	S5	S6	S7	S8	TP1	TP2	TP3	TP4	TP5	TP6	TP7	TP8	TP9	TP10	TP11	TP12	TP13	TP14	TP15	TP16	TP17	TP18	TP19	Remarks
1	I_{CC}	1	1	1	1	1	2	1	1	1										M(+)	M(−)									Note 1
2	$v_{0(B)}$	1	1	1	1	1	1	1	1	1					SG1											M				Note 2
3	$v_{0(L)}$	1	1	1	1	1	1	1	1	1					SG9											M				Note 3
4	$V_{1(B)}$	1	1	1	1	1	1	1	1	1	M																			TP19 = 0 V
5	$V_{1(L)}$	1	1	1	1	1	1	1	1	1	M																			TP19 = 4 V
6	$V_{26(B)}$	1	1	1	1	1	1	1	1																	M				TP19 = 0 V
7	$V_{26(L)}$	1	1	1	1	1	1	1	1																	M				TP19 = 4 V
8	P/N	1	1	1	1	1	1	1	1	2					SG2										M					Note 4
9	$BW_{(B)}$	1	1	1	1	1	1	1	1	1	(M)				SG3																Note 5
10	v_{ip} SENSE	1	1	1	1	1	1	1	1	1					SG9											M				Note 6
11	v_{ip} MAX.	1	1	1	1	1	1	1	1	1					SG9											M				Note 7
12	μ-1	1	1	1	1	1	1	1	1	1					SG4									M						Note 8
13	$V_{20H\text{-}1}$	1	1	1	1	1	1	1	1	1					SG4									M						Note 9
14	$V_{20L\text{-}1}$	1	1	1	1	1	1	1	1	1					SG4									M						Note 10
15	V_{20TH}	1	1	1	1	2	1	1	1	1					SG4									M						
16	I_{19DEF}	1	1	1	1	1	1	1	1	1							M													Note 11
17	V_{5TH}	1	1	3	1	1	1	1	1	1					SG4			M						P						Note 12
18	μ-2	1	1	2	1	1	1	1	1	1					SG4									M						Note 13
19	$V_{20H\text{-}2}$	1	1	2	1	1	1	1	1	1					SG4									M						Note 14
20	$V_{20L\text{-}2}$	1	1	2	1	1	1	1	1	1					SG4									M						Note 15
21	V_{3H}	1	1	1	1	1	1	1	1	1		M																		
22	V_{3L}	1	1	1	1	1	1	1	1	1		M			SG9															Note 16
23	V_{2H}	1	1	1	1	1	1	1	1	1			M		SG1															Note 17
24	V_{2L}	1	1	1	1	1	1	1	1	1			M		SG1															Note 18
25	$f_{CLU\text{-}1}$	1	1	1	2	1	1	1	1	1				4.5 V	SG1											P				Note 19
26	$f_{CLL\text{-}1}$	1	1	1	2	1	1	1	1	1				4.5 V	SG1											P				Note 20
27	$f_{CLU\text{-}2}$	1	1	1	2	1	1	1	1	1				4.0 V	SG1											P				Note 21
28	$f_{CLL\text{-}2}$	1	1	1	2	1	1	1	1	1				4.0 V	SG1											P				Note 22

No.	Symbol	Measuring circuit	S1	S2	S3	S4	S5	S6	S7	S8	TP1	TP2	TP3	TP4	TP5	TP6	TP7	TP8	TP9	TP10	TP11	TP12	TP13	TP14	TP15	TP16	TP17	TP18	TP19	Remarks
29	V_{6TH}	1	1	1	2	1	1	1	2	1				M														P		Note 23
30	FC1	1	1	1	1	1	1	1	1	1	(M)				SG_3											M				Note 24
31	FC2	1	1	1	1	1	1	1	1	1	(M)				SG_3											M				Note 24
32	FC3	1	1	1	1	1	1	1	1	1	(M)				SG_3											M				Note 24
33	IM	1	2	1	1	1	1	1	1	1	(M)				SG_5															Note 25
34	DG	1	1	1	1	1	1	1	1	1					SG_1										M					Note 26
35	DP	1	1	1	1	1	1	1	1	1					SG_1										M					Note 27
36	$V_{sync(B)}$	1	1	1	1	1	1	1	1	1					SG_1											M				Note 28
37	$V_{sync(L)}$	1	1	1	1	1	1	1	1	1					SG_9											M				Note 29
38	$SR_{(B)}$	1	1	1	1	1	1	1	1	1					SG_1											M				Note 30
39	$SR_{(L)}$	1	1	1	1	1	1	1	1	1					SG_9											M				Note 31
40	$R_{in(V)}$	2																													
41	$C_{in(V)}$	2																													
42	$V_{ccmin.}$	1	1	1	1	1	1	2	1	1												M								Note 32
43	f_H	1	1	1	1	1	1	2	1	1												M								Note 33
44	f_{PL}	1	1	1	1	1	1	1	1	1					SG_6							M				P				Note 34
45	f_{PH}	1	1	1	1	1	1	1	1	1					SG_6							M				P				Note 35
46	V_{TH}	1	1	1	1	1	1	1	1	1					SG_1											P			M	Note 36
47	μ-s	1	1	1	1	1	1	1	1	1					SG_7									M						Note 37
48	V_{20H-S}	1	1	1	1	1	1	1	1	1					SG_7									M						Note 38
49	V_{20L-S}	1	1	1	1	1	1	1	1	1					SG_7									M						Note 39
50	RF AGC ΔT_a	1	1	1	1	1	1	1	1	1		M			SG_1															Note 40
51	v_{is} SENSE	1	1	1	1	1	1	1	1	1					SG_1	SG_8			M											Note 41
52	$v_{O(S)}$	1	1	1	1	1	1	1	1	1					SG_1	SG_8			M											Note 42
53	$v_{O(H)}$	1	1	1	1	1	1	2	1	1												M								Note 43

Signal Sources

SG1   B/G system, modulation ratio 87.5 %, Stair 10 steps (no chrominance signal)
$V_{ip} = 90$ dBμ, $f_O = 32.7$ MHz, APL = 50 %

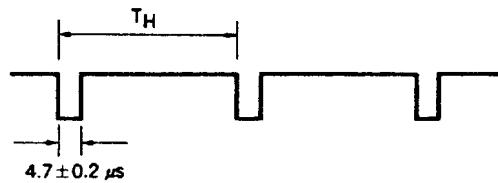SG2   L system, modulation ratio 94 %, white 100 % signal
$V_{ip} = 90$ dBμ, $f_O = 32.7$ MHz

SG3   CW mixed waves
$f_1 = 32.7$ MHz, $V_{ip} = 90$ dBμ
$f_2 = 32.7$ MHz $+ \Delta f$ $V_{ip} = 60$ dBμ
Δf is 0.5 to 10 MHz.

SG4   B/G system, modulation ratio 87.5 % or equivalent, black video signal
$V_{ip} = 90$ dBμ, $f_O = 32.7$ MHz

SG5   CW mixed waves:
$f_1 = 32.7$ MHz, $V_{ip} = 90$ dBμ
$f_2 = 32.106$ MHz, $V_{ip} = 80$ dBμ
$f_3 = 39.2$ MHz, $V_{ip} = 80$ dBμ

SG6   32.7 MHz modulated waves added by the following pulse to L system modulation signal

T_H
4.7 ± 0.2 μs

  — T_H is variable around 64 μs at lock range measurement.
  — The horizontal frequency is 1/TH.

SG7   L system, modulation ratio 94 %, white 100 % video signal
$V_{ip} = 90$ dBμ, $f_O = 32.7$ MHz

SG8   CW wave 38.2 MHz
About mixed waves

25 Ω   25 Ω   25 Ω   25 Ω
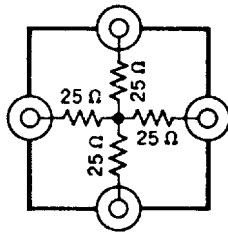
Use the mixer shown on the left for SG3, SG5, and SG6.
Terminate the one remaining pin in SG3 and SG5 with 50 ohms.
⊚ is a BNC connector.

SG9   L system, modulation ratio 94 %, Stair 10 steps
$V_{ip} = 90$ dBμ, $f_O = 32.7$ MHz

NOTES

Note 1: Connect the plus (+) side of the ammeter to TP10 and the minus (−) side to TP11.

Note 2: Adjust VR2 to set TP19 to 0 V, connect SG1 to TP5 (BNC), then measure the amplitude from white 100 % to the leading tip of the sync signal at TP16 with an oscilloscope.

Note 3: Connect SG9 to TP9 (BNC) and measure the amplitude from white 100 % to the leading tip of the sync signal at TP16 with an oscilloscope.

Note 4: Input SG2 to TP5 (BNC) and inputs the TP15 (BNC) output to the PAL noise meter.

Note 5:
  a. Set SG3 as shown below.
     Mixed waves:
     $f_1 = 32.7$ MHz, $V_{ip} = 90$ dBμ
     $f_2 = 33.2$ MHz, $V_{ip} = 60$ dBμ
  b. Measure the 0.5 MHz component at pin 1 of the DUT.
  c. Increase frequency f_2 unitl $(f_1 - f_2)$ at pin 1 of the DUT decreases 3 dB to V_i, then read the frequency.
  d. $BW_{(B)} = f_2 - 32.7$ (MHz)

Note 6: Connect an oscilloscope to TP16. Set the SG9 output to 90 dBμ then adjust the TP16 output to 2 $V_{p\text{-}p}$. Increase the SG9 output from 90 dBμ until the TP16 output decreases 3 dB (approx. 1.4 $V_{p\text{-}p}$). The output level at this time is $V_{ip\ SENSE}$.

Note 7: Similar to Note 6, adjust the TP16 output level, then increase the SG9 output until the TP16 output decreases 1 dB (approx. 1.78 $V_{p\text{-}p}$). The output level at this time is $V_{ip\ MAX}$.

Note 8: Adjust VR2 to set the TP19 voltage to 0 V, input the SG4 signal to TP5 (BNC), and connect an ammeter to TP14. While reading the ammeter, change the SG4 frequency from 27.7 MHz to 37.7 MHz. The AFT sensitivity is defined as shown below on the curve obtained at this time.
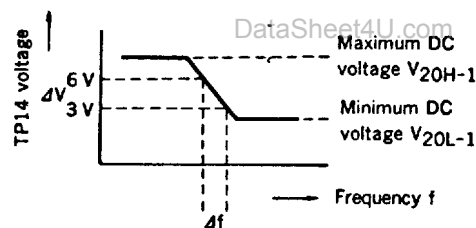
AFT detection sensitivity $\mu\text{-}1 = \dfrac{\Delta V}{\Delta f}$ (mV/kHz)

Note 9: The maximum DC voltage shown in Note 8 is stated as $V_{20H\text{-}1}$.

Note 10: The minimum DC voltage shown in Note 8 is stated as $V_{20L\text{-}1}$.

Note 11: Connect the plus (+) side of the ammeter to TP7 and the minus (−) side to GND.

Note 12: Connect an ammeter to TP8 and TP14 and adjust VR1 to increase the TP8 voltage from the minimum value. V_{5TH} is the TP8 voltage when the TP14 polarity changes.

Note 13: AFT sensitivity measurement procedures are the same as in Note 8. Define μ-2 as follows:

$$\mu\text{-}2 = \frac{\mu\text{-}1}{\text{Measured value}} \times 100 \ (\%)$$

Note 14: Curve when the polarity in Note 8 is reversed. Same as AFT maximum voltage 1.

Note 15: Curve when the polarity in Note 8 is reversed. Same as AFT minimum voltage 1.

Note 16: Input SG9 to TR5 (BNC) and an ammeter to TP3. The TP3 voltage when the SG9 output becomes the maximum capacitance is the IF AGC minimum voltage.

Note 17: Connect SG1 to TR5 (BNC) and an ammeter to pin 4 of the DUT and adjust VR3 to 3.09 V. Connect TP2 to the ammeter and measure the TP2 voltage when the SG1 output becomes 70 dBμV. This voltage is the RF AGC maximum voltage.

Note 18: The TP2 voltage when the SG1 output becomes 90 dBμ in Note 17 is the RF AGC minimum voltage.

Note 19: Connect an oscilloscope to TP16. Adjust VR1 and set the TP4 voltage to 4.5 V, then increase the SG1 frequency while reading the TP16 waveforms until the VCO is unlocked. Decrease the SG1 frequency until the VCO is locked. This frequency is $f_{CLU\text{-}1}$.

Note 20: Decrease the SG1 frequency until VCO is unlocked in Note 19. Then, increase the frequency until the VCO is locked. This frequency is $f_{CLL\text{-}1}$.

Note 21: Set the TP4 voltage to 4.0 V and perform the same steps as in Note 19. The measured value is $f_{CLU\text{-}2}$.

Note 22: Set the TP4 voltage to 4.0 V and perform the same steps as in Note 20. The measured value is $f_{CLL\text{-}2}$.

Note 23: Connect an ammeter to TP4 and an oscilloscope to TP18 and adjust VR1 to decrease the TP4 voltage from the maximum value. The TP4 voltage when the TP18 voltage changes from high to low is the lock detection threshold voltage.

Note 24: Connect SG3 to TP5 (BNC) and observe the Δf signal level of pin 1 of the DUT with a spectrum analyzer. Then, observe the Δf signal level of TP16. The EQ frequency characteristic is the TP16 level minus the level of pin 1 of the DUT.

Note 25: Input SG5 to TP5 (BNC), observe TP16, and adjust VR1 so that the TP16 wave becomes the minimum. The level at pin 1 of the DUT (4.406 MHz level to 2.094 MHz level) is the inter-modulation.

Note 26: Add a chrominance signal in SG1 and input to TP5 (BNC). Connect TP15 (BNC) to a vector scope to measure in DG mode.

Note 27: Observe in DP mode in the same way as in Note 26.

Note 28: Connect S1 to TP5 (BNC) and an oscilloscope to TP16. Adjust VR2 so that the TP19 voltage becomes 0 V. The sync level observed at TP16 at this time is the sync chip level 1.

Note 29: Connect SG9 to TP5 (BNC) and an oscilloscope to TP16. Adjust the TP19 voltage with VR2 so that the TP16 output reaches 2 V$_{p\text{-}p}$. The sync level observed at this time is the sync chip level 2.

11

Note 30: The PAL sync ratio is found by the following expression in Note 28:
(Black level − sync level)/output voltage of pin 16 x 100 (%)

Note 31: The SECAM sync ratio is found by the following expression in Note 29:
(Black level − sync level)/2 x 100 (%)

Note 32: Connect an oscilloscope to TP12 and increase V_{CC} from 0 V. The V_{CC} voltage when the waveform of the TP12 output becomes 2 μs cycles is V_{CC} min.

Note 33: Connect a spectrum analyzer to TP12, read the value, and divide it by 32. This value is the horizontal free-run frequency.

Note 34: Input SG6 to TP5 (BNC), and connect a spectrum analyzer to TP12 and an oscilloscope to TP16. Increase the SG6 cycle T_H until the VCO is unlocked, then decrease until the VCO is locked. Read the spectrum analyzer at this time and divide the read value by 32. The horizontal pull-in range (f_{PL}) is the difference between the obtained value and 15.625 kHz.

Note 35: Connect in the same way as in Note 34. Increase the SG6 cycle T_H until the VCO is unlocked, then decrease until the VCO is locked. Read the spectrum analyzer at this time and divide the read value by 32. The horizontal pull-in range (f_{PH}) is the difference between the obtained value and 15.625 kHz.

Note 36: Connect the oscilloscope to TP16 and an ammeter to TP19. Adjust VR2 to increase the TP19 voltage from 0 V until the TP waveforms are reversed. This TP19 voltage is the G/L switch threshold voltage.

Note 37: Input SG7 to TP5 (BNC) and connect an ammeter to TP14. Measure in the same way as in Note 8.

Note 38: Maximum AFT output voltage when the SG7 frequency is variable in Note 37. Measurement procedures are the same as in Note 9.

Note 39: Minimum AFT output voltage when the SG7 frequency is variable in Note 37. Measurement procedures are the same as in Note 10.

Note 40: Input SG1 to TP5 (BNC) and connect an ammeter to TP2. Change the ambient temperature T_a from −25 °C to 75 °C. The input level displacement required to change the TP2 output level is the RF AGC temperature characteristics.

Note 41: Input SG1 to TP5 (BNC), and connect SG8 to TP6 (BNC) and a spectrum analyzer to TP9. Increase the SG8 signal level until the TP9 output voltage reaches the SIF DET maximum output voltage. Next, decrease the SG8 signal level until the TP9 output voltage decreases 3 dB. The signal level at this time is the SIF DET input sensitivity.

Note 42: Input SG1 to TP5 (BNC), and connect SG8 to TP6 (BNC) and a spectrum analyzer to TP9. Increase the SG8 signal level until the TP9 output voltage is saturated. The voltage at this time is the SIF DET maximum output voltage.

Note 43: Connect an oscilloscope to TP12.

12

Application Circuit Example
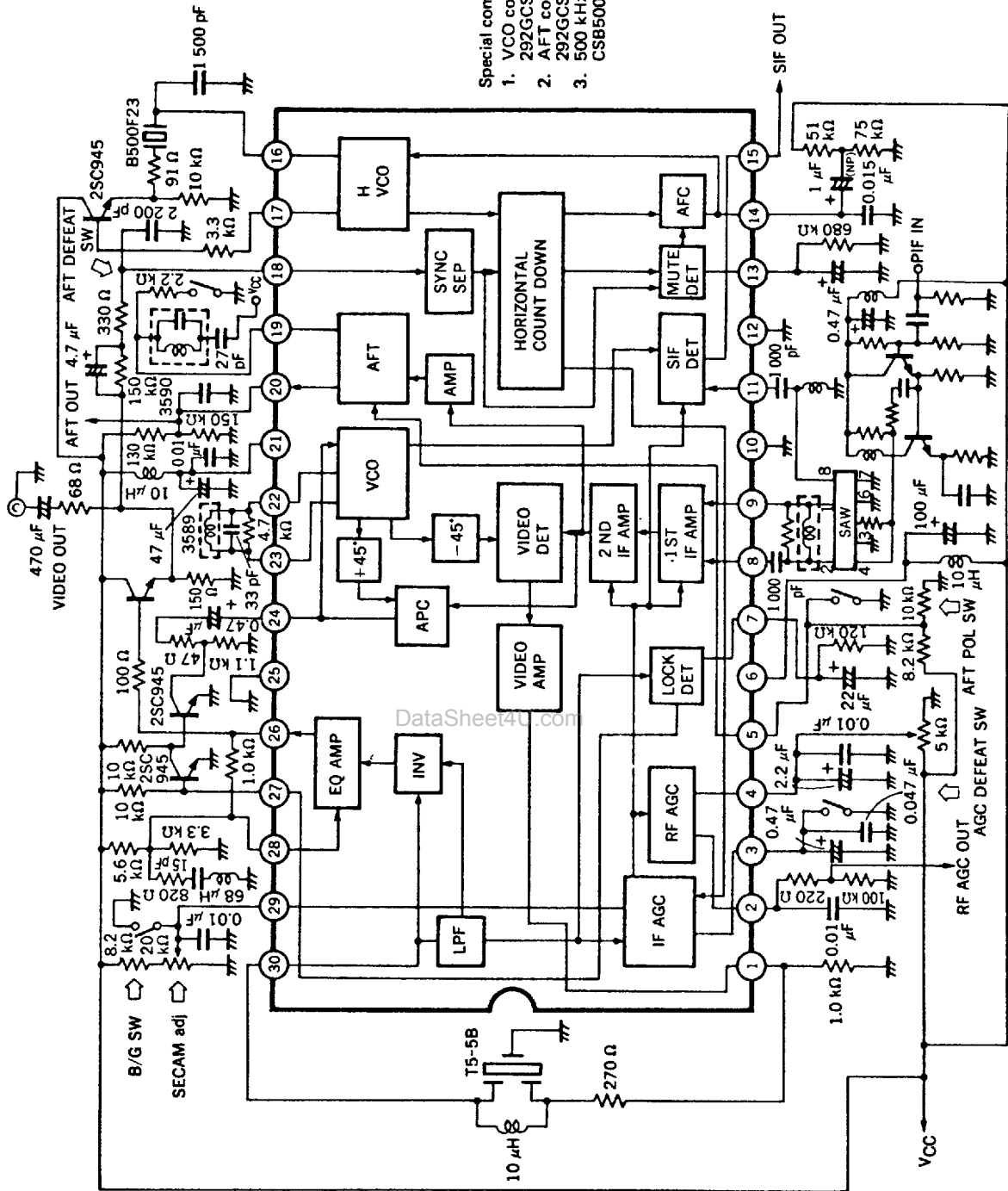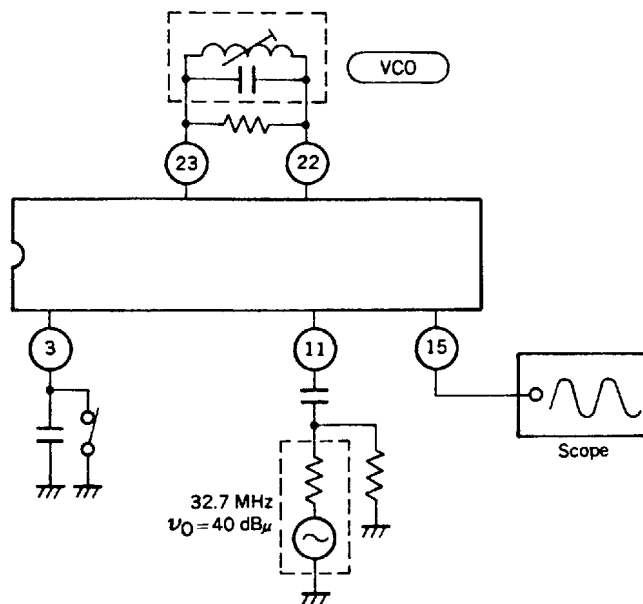
Special components
1. VCO coil (38.9 MHz)
   292GCS-3589BS (TOKO)
2. AFT coil (38.9 MHz)
   292GCS-3590AYC (TOKO)
3. 500 kHz CERALOCK
   CSB500F23 (MURATA)

The application circuit and circuit constants are examples and do not apply to mass production.
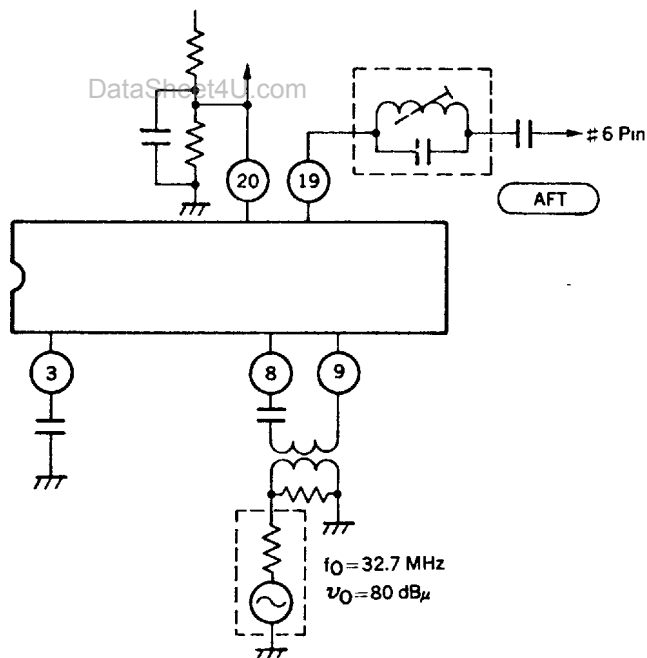
13

Alignment Procedure of VCO coil and AFT coil.

1. VCO

Refer the above figure. The alignment conditions are as followings.

1. Input signal at pin11 : f_o = 32.7 MHz, v_i = 40 dBμ

   Use modulated or un-modulated signal.

2. Connect the pin3 to GND.

On these condition, adjust the VCO coil until the output signal at pin 15 becomes lowest frequency. The output signal at pin15 is beat signal between the input signal at pin11 and VCO signal.
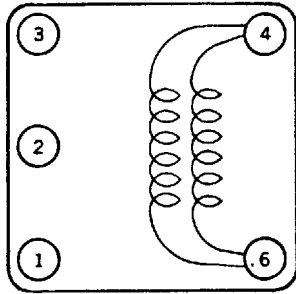
2. AFT

Refer the above figure. The alignment conditions are as followings.

1. Input signal from pin8 and pin 9 : f_o = 32.7 MHz, v_i = 80 dBμ

   Use modulated or un-modulated signal.

On these condition, adjust the AFT coil until the output DC voltage at pin20 becomes 4.5±0.1 V.

14

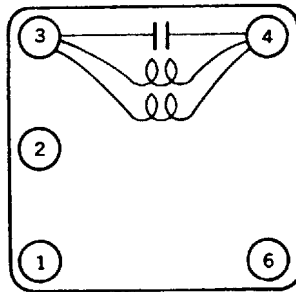**Specification of coil. (7 mm square, 39 MHz)**

1. VCO

Manufacturer	: TOKO
Type Number	: 292GCS-3589BS
Center frequency	: 39 MHz
Q	: 87
Turns pin4 — pin6	: 7T
Wire	: 0.1ϕ 2UEW-SL

2. AFT

Manufacturer	: TOKO
Type Number	: 292GCS-3590
Center frequency	: 39 MHz
Q	: 70
Turns pin4 — pin6	: 4T
Wire	: 0.1ϕ 2UEW-SL

Advice for layout of Print circuit board.

1. Separate the GND wire of pin10 and pin12.
   Pin10 is connected with the GND of SAW filter and pre-amplifier.

2. Capacitor at pin6 is ground to pin12.
   The wire between the capacitor and pin12 must be short as far as possible.

3. The AFT coil must be arranged at the side of pin15 and pin16.
   The wire must be short as far as possible and be kep apart from VCO coil.

4. Case of VCO coil is ground to pin25.

5. Case of AFT coil is ground to pin12.

6. Capacitor at pin21 is ground to pin25.

7. Series capacitor at AFT coil must be connected with pin6.
   To suppress the variation of AFT output voltage at weak signal condition.

8. The collector of transistor at pin17 must be connected with V_{CC} except pin6 and pin21.

16

Pin Description

Pin No.	Pin name	Equivalent circuit	Function
1	VIDEO OUT (4.9 V)		Demodulated video signal output pin. The voltage is approximately 4.9 V at no signal; the level of the leading edge tip of the sync signal is 3.3 V at demodulation; and the video amplitude is 1.4 V_{p-p}.
2	RF AGC OUT (8.1 V)		Output pin of RF AGC control signal used as tuner AGC signal
3	IF AGC FILTER (8.5 V)		IF AGC control voltage smooth pin. This pin is used to set the time constant depending on external capacity.
4	RF AGC DELAY (0 to V_{CC})		RF AGC delay point control input pin

17

Pin No.	Pin name	Equivalent circuit	Function
5	AFT POLARITY (0 to 5 V)		AFT output polarity switch input pin to PIF input frequency. The threshold voltage is 2.7 V and the PIF input frequency to AFT output voltage is positive at high level and negative at low level.
6	V_CC		Power supply pin for AFT, H VCO, and IF/RF AGC. Use at 8 to 10 V (9 V, typ.).
7	LOCK DET FILTER (4.9 V)		Lock detector smooth pin. This pin is used to set the LOCK SW time constant. The input impedance is approximately ·12 k-ohms.
8 9	PIF IN (2.2 V)		PIF signal input pin. The input impedance is approximately 1 k-ohms.
10	GND		GND pin for PIF amplifier SIF DET.

18

| Pin No.	Pin name	Equivalent circuit	Function
11	SIF DET IN (4.0 V)		SIF DET input pin. The input impedance is approximately 2 k-ohms.
12	GND		GND pin for AFT, H/VCO, and RF/IF AGC
13	CONCIDENCE FILTER (0 V)		Filter pin used to detect the horizontal VCO (H/VCO) sync mode. The signal goes low when the horizontal PLL is unlocked.
14	AFC FILTER (5.3 V)		AFC filter pin. Use a 1 μF external electrolytic capacitor with no polarity.
15	SIF DET OUT (7.65 V)		SIF split carrier output pin. The maximum output voltage is approximately 300 mV$_{p-p}$.

Pin No.	Pin name	Equivalent circuit	Function
16	H/OSC IN (3.9 V)		Horizontal VCO oscillation input pin. The input impedance is approximately 2.9 k-ohms.
17	H/OSC OUT (7.2 V)		Horizontal VCO oscillator output pin. The output voltage is 270 mV$_{p-p}$ (typ.).
18	SYNC SEPA IN (6.7 V)		Sync separator input pin. The bias voltage is approximately 6.7 V.
19	AFT COIL (5.4 V)		AFT phase control pin. The opposite side of the capacitor connected with the AFT coil is connected to pin 6 (V$_{CC}$).

Pin No.	Pin name	Equivalent circuit	Function
20	AFT OUT (4.7 V)		AFT output pin. The output voltage is 0.8 to 8 V. The sensitivity is adjustable depending on the external resistor.
21	V_CC		Power supply pin for PIF/PLL VCO APC. For bypass capacitor GND, use the same GND as pin 25.
22 23	VCO COIL (7.8 V)		PLL VCO oscillator coil pin. Set the dumping resistor to 4.7 k-ohms or more.
24	APC FILTER (4.5 V)		PLL VCO control voltage filter pin
25	GND		GND pin for PLL VCO, APC, and SIF DET

21

Pin No.	Pin name	Equivalent circuit	Function
26	EQ VIDEO OUT B/G (5.7 V) L (2.5 V)		Equalizer amplifier output pin. Use the video signal at 3.2 V at the sync edge and the amplitude under 2 V_{p-p}.
27	LOCK SW (OFF)		Pin used to switch the time constant of PLL VCO control voltage filter. The signal goes low impedance when PLL VCO is locked to IF carrier.
28	FEED BACK EQ B/G (4.9 V) L (2.9 V)		Equalizer amplifier blaking input pin. The frequency characteristics are adjustable by Z_f.
29	SECAM LEVEL (0 to 7 V)		Demodulation level control input pin at L system (positive modulation signal) modulation. Apply approximately 4.42 V. Set to 0 V at G/G system modulation. Use this control input pin between 0 to 7 V.

Pin No.	Pin name	Equivalent circuit	Function
30	EQ IN (4.9 V)		Equalizer amplifier input pin. The voltage is 4.9 V at no signal and 3.3 V at the sync edge of the video signal. The amplitude of the video signal is 1.4 V_{p-p}.

30-pin Plastic Shrink DIP (400 mil) External View
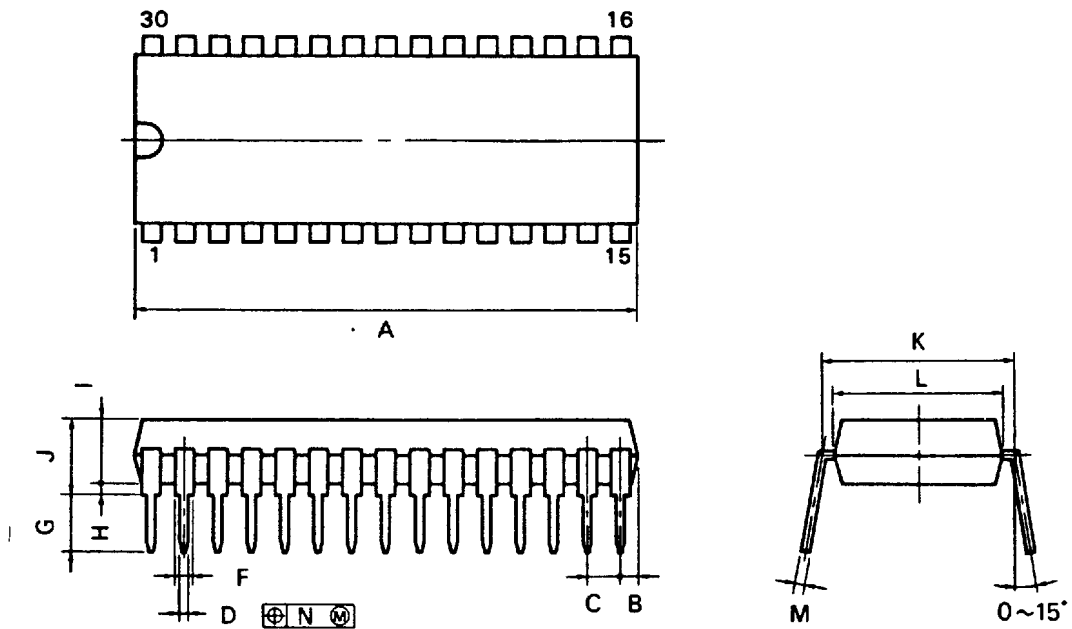
S30C-70-4008

NOTES

1) Each lead centerline is located within 0.17 mm (0.007 inch) of its true position (T.P.) at maximum material condition.

2) Item "K" to center of leads when formed parallel.

ITEM	MILLIMETERS	INCHES
A	28.46 MAX.	1.121 MAX.
B	1.78 MAX.	0.070 MAX.
C	1.778 (T.P.)	0.070 (T.P.)
D	$0.50^{+0.10}_{}$	$0.020^{+0.004}_{-0.005}$
F	0.85 MIN.	0.033 MIN.
G	$3.2^{+0.3}_{}$	$0.126^{+0.012}_{}$
H	0.51 MIN.	0.020 MIN.
I	4.31 MAX.	0.170 MAX.
J	5.08 MAX.	0.200 MAX.
K	10.16 (T.P.)	0.400 (T.P.)
L	8.6	0.339
M	$0.25^{+0.10}_{-0.05}$	$0.010^{+0.004}_{-0.003}$
N	0.17	0.007

24