

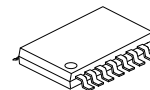
**U74LVC04A****CMOS IC****HEX INVERTERS**■ **DESCRIPTION**

The UTC **U74LVC04A** consists of six independent inverters, it provides the function $Y = \bar{A}$.

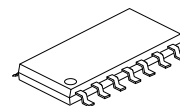
Inputs can be driven from either 3.3V or 5V devices, so the device can be used in a mix 3.3V/5V system.

■ **FEATURES**

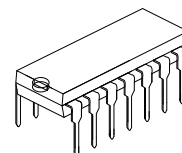
- * Operation Voltage Range: 1.65~3.6V
- * Low Power Dissipation
- * Input accept voltage to 5.5V



TSSOP-14



SOP-14



DIP-14

■ **ORDERING INFORMATION**

Ordering Number		Package	Packing
Lead Free	Halogen Free		
U74LVC04AL-D14-T	U74LVC04AG-D14-T	DIP-14	Tube
U74LVC04AL-S14-R	U74LVC04AG-S14-R	SOP-14	Tape Reel
U74LVC04AL-P14-R	U74LVC04AG-P14-R	TSSOP-14	Tape Reel

U74LVC04AL-D14-T

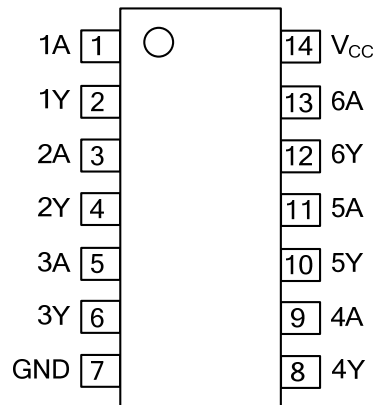
- (1) Packing Type
- (2) Package Type
- (3) Lead Plating

(1) R: Tape Reel, T: Tube

(2) D14: DIP-14, P14: TSSOP-14, S14: SOP-14

(3) G: Halogen Free, L: Lead Free

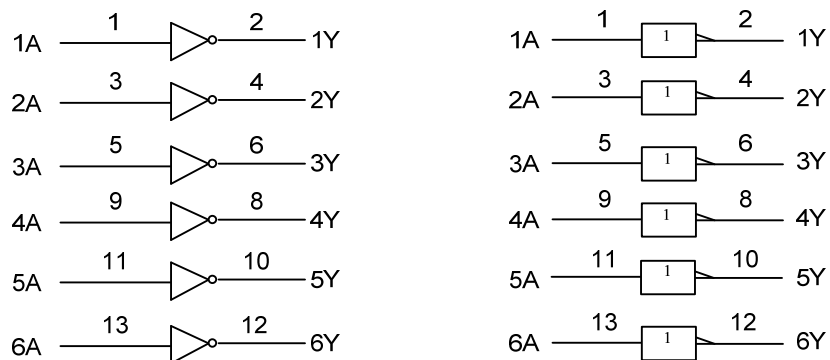
PIN CONFIGURATION



FUNCTION TABLE (each gate)

INPUT	OUTPUT
A	Y
L	H
H	L

LOGIC DIAGRAM (positive logic)



IEC logic symbol

■ ABSOLUTE MAXIMUM RATINGS (unless otherwise specified)

PARAMETER	SYMBOL	RATINGS	UNIT
Supply Voltage	V_{CC}	-0.5~6.5	V
Input Voltage	V_{IN}	-0.5~6.5	V
Output Voltage(active mode)	V_{OUT}	-0.5~ $V_{CC}+0.5$	V
Input Clamp Current($V_{IN}<0$)	I_{IK}	-50	mA
Output Clamp Current($V_{OUT}<0$)	I_{OK}	-50	mA
Output Current	I_{OUT}	± 50	mA
V_{CC} or GND Current	I_{CC}	± 100	mA
Power Dissipation	P_D	500	mW
Derated Above 60°C		5.5	mW/°C
Storage Temperature	T_{STG}	-65 ~ +150	°C

Note: Absolute maximum ratings are those values beyond which the device could be permanently damaged.

Absolute maximum ratings are stress ratings only and functional device operation is not implied.

■ RECOMMENDED OPERATING CONDITIONS

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNIT
Supply Voltage	V_{CC}	Operating	1.65		3.6	V
		Data retention only	1.5			V
Input Voltage	V_{IN}		0		5.5	V
Output Voltage	V_{OUT}		0		V_{CC}	V
Operating Temperature	T_A		-40		125	°C

■ STATIC CHARACTERISTICS ($T_a=25^\circ\text{C}$)

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
High-Level Input Voltage	V_{IH}	$V_{CC}=1.65\text{V}\sim 1.95\text{V}$	$0.65 \times V_{CC}$			V
		$V_{CC}=2.3\text{V}\sim 2.7\text{V}$	1.7			V
		$V_{CC}=2.7\text{V}\sim 3.6\text{V}$	2			V
Low-Level Input Voltage	V_{IL}	$V_{CC}=1.65\text{V}\sim 1.95\text{V}$			$0.35 \times V_{CC}$	V
		$V_{CC}=2.3\text{V}\sim 2.7\text{V}$			0.7	V
		$V_{CC}=2.7\text{V}\sim 3.6\text{V}$			0.8	V
High-Level Output Voltage	V_{OH}	$V_{CC}=1.65\text{V}\sim 3.6\text{V}$, $I_{OH}=-100\mu\text{A}$	V_{CC} -0.2			V
		$V_{CC}=1.65\text{V}$, $I_{OH}=-4\text{mA}$	1.29			V
		$V_{CC}=2.3\text{V}$, $I_{OH}=-8\text{mA}$	1.9			V
		$V_{CC}=2.7\text{V}$, $I_{OH}=-12\text{mA}$	2.2			V
		$V_{CC}=3\text{V}$, $I_{OH}=-12\text{mA}$	2.4			V
		$V_{CC}=3\text{V}$, $I_{OH}=-24\text{mA}$	2.3			V
Low-Level Output Voltage	V_{OL}	$V_{CC}=1.65\text{V}\sim 3.6\text{V}$, $I_{OL}=100\mu\text{A}$			0.1	V
		$V_{CC}=1.65\text{V}$, $I_{OL}=4\text{mA}$			0.24	V
		$V_{CC}=2.3\text{V}$, $I_{OL}=8\text{mA}$			0.3	V
		$V_{CC}=2.7\text{V}$, $I_{OL}=12\text{mA}$			0.4	V
		$V_{CC}=3\text{V}$, $I_{OL}=24\text{mA}$			0.55	V
Input Leakage Current	$I_{I(LEAK)}$	$V_{CC}=3.6\text{V}$, $V_{IN}=5.5\text{V}$ or GND			± 1	μA
Quiescent Supply Current	I_Q	$V_{CC}=3.6\text{V}$, $V_{IN}=V_{CC}$ or GND, $I_{OUT}=0$			1	μA
Additional quiescent Supply Current	ΔI_Q	$V_{CC}=2.7\text{V} \sim 3.6\text{V}$ One input at $V_{CC}-0.6\text{V}$, other inputs at V_{CC} or GND			500	μA
Input Capacitance	C_{IN}	$V_{CC}=3.3\text{V}$, $V_{IN}=V_{CC}$ or GND		5		pF

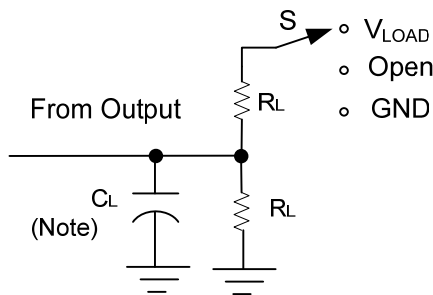
■ DYNAMIC CHARACTERISTICS (Ta=25°C)

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Propagation Delay From Input (A) to Output(Y)	t_{PLH}/t_{PHL}	$V_{CC}=1.8V\pm0.15V$	1	4.1	7.5	ns
		$V_{CC}=2.5V\pm0.2V$	1	3.6	7	ns
		$V_{CC}=2.7V$	1	3	5.3	ns
		$V_{CC}=3.3V\pm0.3V$	1	2.5	4.3	ns

■ OPERATING CHARACTERISTICS (Ta=25°C)

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Power Dissipation Capacitance	Cpd	$V_{CC}=1.8V, f=10MHz$		6		pF
		$V_{CC}=2.5V, f=10MHz$		7		pF
		$V_{CC}=3.3V, f=10MHz$		8		pF

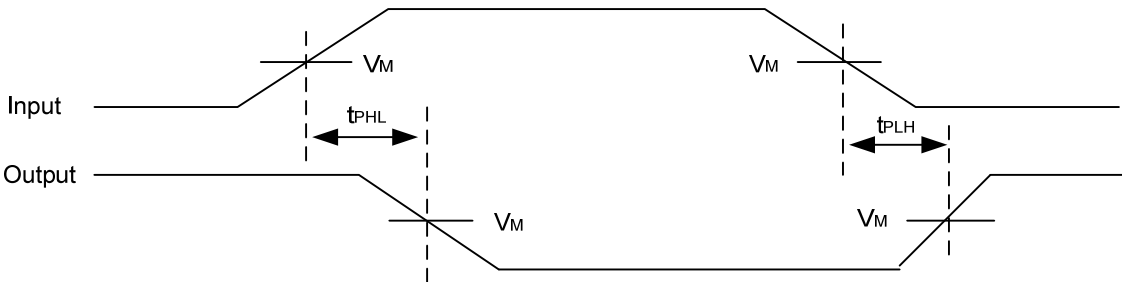
■ TEST CIRCUIT AND WAVEFORMS



TEST	S
t_{PLH}/t_{PHL}	Open
t_{PHZ}/t_{PZH}	GND
t_{PLZ}/t_{PZL}	V_{LOAD}

Note: C_L includes probe and jig capacitance.

V_{CC}	V_{IN}	t_{R}/t_F	V_M	V_{LOAD}	C_L	R_L	V_{Δ}
$1.8V \pm 0.15V$	V_{CC}	$\leq 2ns$	$V_{CC}/2$	$2 \times V_{CC}$	30pF	1K Ω	0.15V
$2.5V \pm 0.2V$	V_{CC}	$\leq 2ns$	$V_{CC}/2$	$2 \times V_{CC}$	30pF	500 Ω	0.15V
2.7V	2.7V	$\leq 2.5ns$	1.5V	6V	50pF	500 Ω	0.3V
$3.3V \pm 0.3V$	2.7 V	$\leq 2.5ns$	1.5V	6V	50pF	500 Ω	0.3V



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