

RJK1028DNS

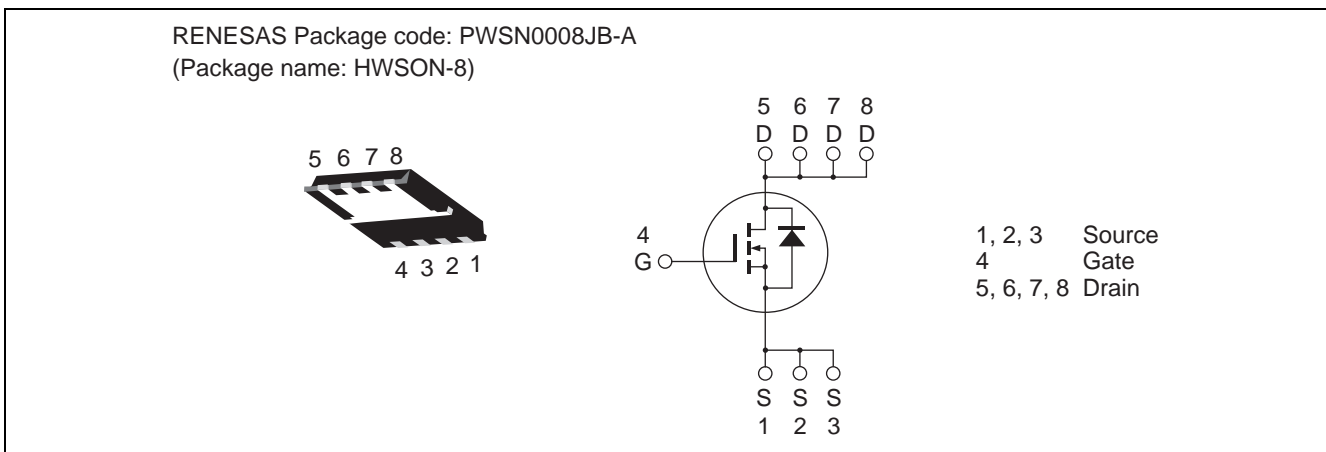
Silicon N Channel Power MOS FET Power Switching

R07DS0195EJ0300
Rev.3.00
Jan 30, 2012

Features

- High speed switching
- Capable of 4.5 V gate drive
- Low drive current
- High density mounting
- Low on-resistance
 $R_{DS(on)} = 125 \text{ m}\Omega$ typ. (at $V_{GS} = 10 \text{ V}$)
- Pb-free
- Halogen-free

Outline



Absolute Maximum Ratings

($T_a = 25^\circ\text{C}$)

Item	Symbol	Ratings	Unit
Drain to source voltage	V_{DSS}	100	V
Gate to source voltage	V_{GSS}	+12, -5	V
Drain current	I_D	4	A
Drain peak current	$I_{D(pulse)}$ ^{Note1}	12	A
Body-drain diode reverse drain current	I_{DR}	4	A
Avalanche current	I_{AP} ^{Note 2}	2	A
Avalanche energy	E_{AR} ^{Note 2}	0.4	mJ
Channel dissipation	P_{ch} ^{Note3}	10	W
Channel to case thermal impedance	θ_{ch-c} ^{Note3}	12.5	$^\circ\text{C}/\text{W}$
Channel temperature	T_{ch}	150	$^\circ\text{C}$
Storage temperature	T_{stg}	-55 to +150	$^\circ\text{C}$

- Notes: 1. $PW \leq 10 \mu\text{s}$, duty cycle $\leq 1\%$
 2. Value at $T_{ch} = 25^\circ\text{C}$, $R_g \geq 50 \Omega$
 3. $T_c = 25^\circ\text{C}$

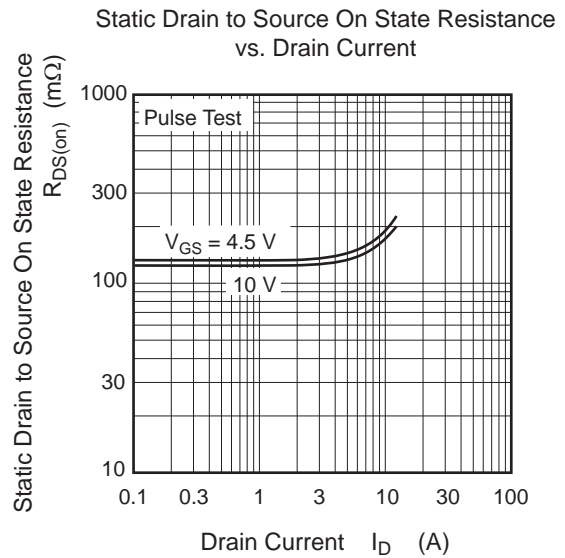
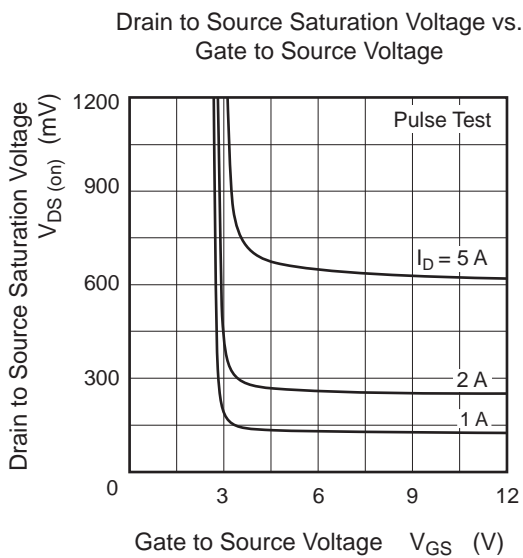
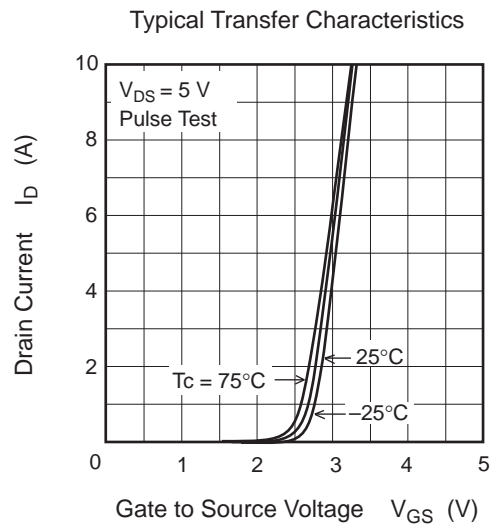
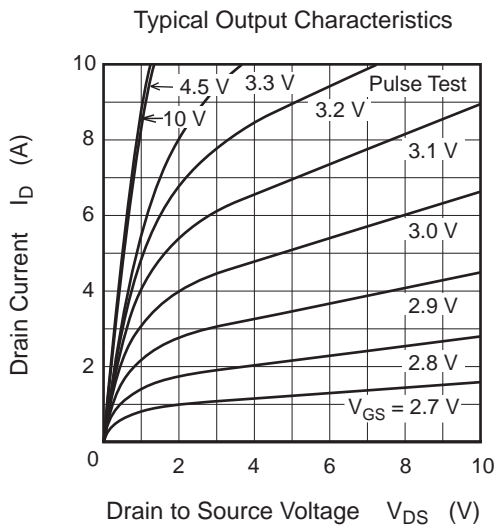
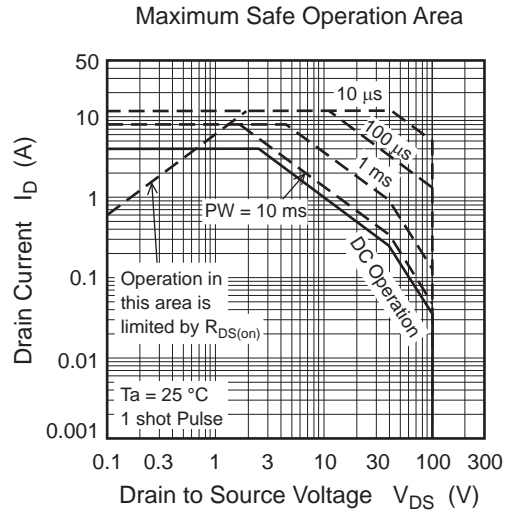
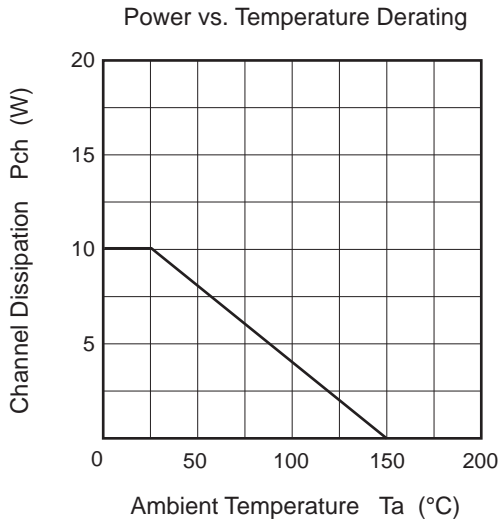
Electrical Characteristics

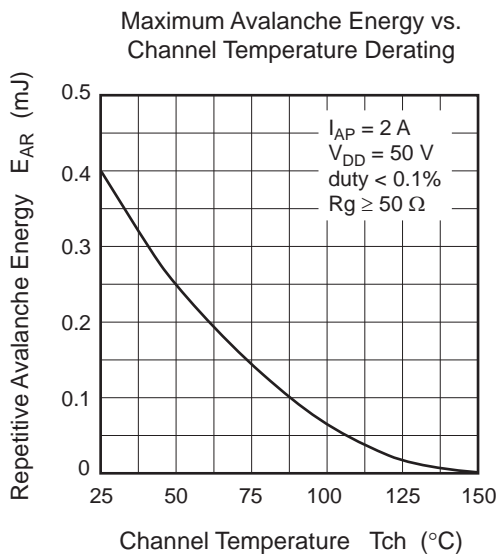
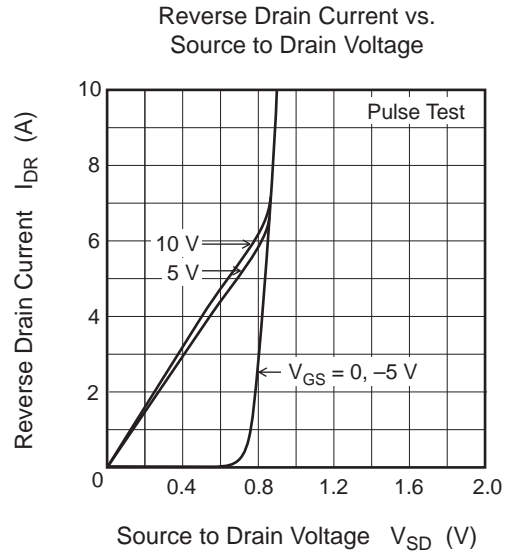
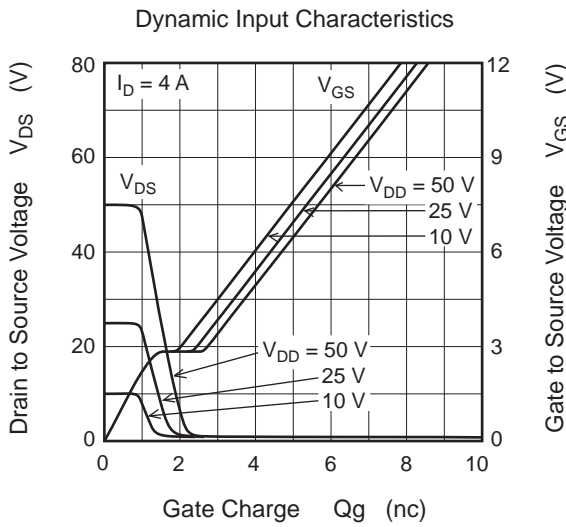
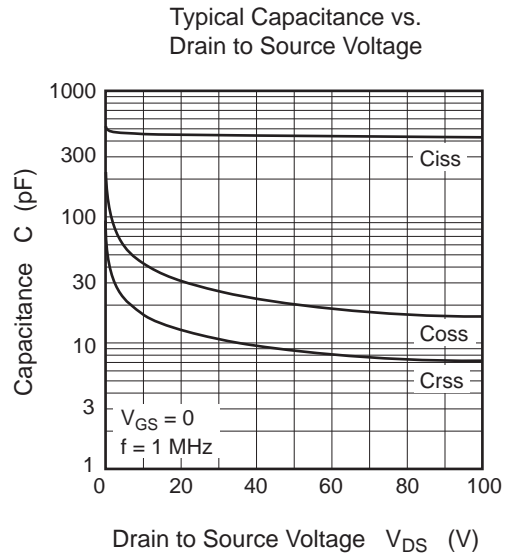
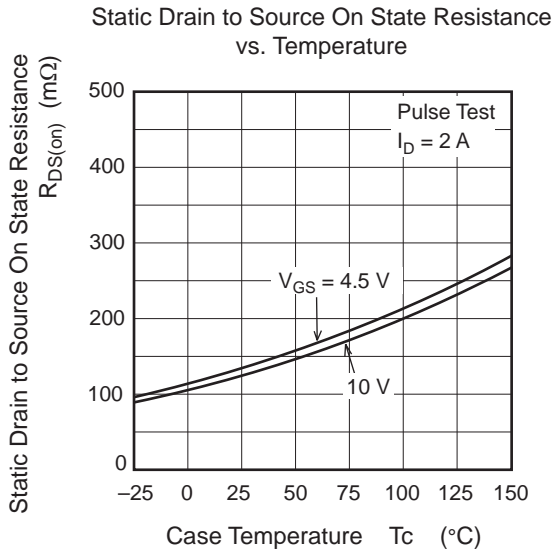
(Ta = 25°C)

Item	Symbol	Min	Typ	Max	Unit	Test Conditions
Drain to source breakdown voltage	$V_{(BR)DSS}$	100	—	—	V	$I_D = 10 \text{ mA}$, $V_{GS} = 0$
Gate to source leak current	I_{GSS}	—	—	± 0.1	μA	$V_{GS} = +12, -5 \text{ V}$, $V_{DS} = 0$
Zero gate voltage drain current	I_{DSS}	—	—	10	μA	$V_{DS} = 100 \text{ V}$, $V_{GS} = 0$
Gate to source cutoff voltage	$V_{GS(off)}$	1.2	—	2.5	V	$V_{DS} = 10 \text{ V}$, $I_D = 1 \text{ mA}$
Static drain to source on state resistance	$R_{DS(on)}$	—	125	165	$\text{m}\Omega$	$I_D = 2 \text{ A}$, $V_{GS} = 10 \text{ V}$ ^{Note4}
	$R_{DS(on)}$	—	135	180	$\text{m}\Omega$	$I_D = 2 \text{ A}$, $V_{GS} = 4.5 \text{ V}$ ^{Note4}
Forward transfer admittance	$ y_{fs} $	—	8.8	—	S	$I_D = 2 \text{ A}$, $V_{DS} = 5 \text{ V}$ ^{Note4}
Input capacitance	C_{iss}	—	450	—	pF	$V_{DS} = 10 \text{ V}$
Output capacitance	C_{oss}	—	42	—	pF	$V_{GS} = 0$
Reverse transfer capacitance	C_{rss}	—	17	—	pF	$f = 1 \text{ MHz}$
Gate Resistance	R_g	—	2.7	—	Ω	
Total gate charge	Q_g	—	3.7	—	nC	$V_{DD} = 50 \text{ V}$
Gate to source charge	Q_{gs}	—	1.5	—	nC	$V_{GS} = 4.5 \text{ V}$
Gate to drain charge	Q_{gd}	—	1.5	—	nC	$I_D = 4 \text{ A}$
Turn-on delay time	$t_{d(on)}$	—	8.3	—	ns	$V_{GS} = 10 \text{ V}$, $I_D = 2 \text{ A}$
Rise time	t_r	—	4.8	—	ns	$V_{DD} \cong 30 \text{ V}$
Turn-off delay time	$t_{d(off)}$	—	35	—	ns	$R_L = 15 \Omega$
Fall time	t_f	—	5.6	—	ns	$R_g = 4.7 \Omega$
Body-drain diode forward voltage	V_{DF}	—	0.82	1.07	V	$I_F = 4 \text{ A}$, $V_{GS} = 0$ ^{Note4}
Body-drain diode reverse recovery time	t_{rr}	—	27	—	ns	$I_F = 4 \text{ A}$, $V_{GS} = 0$ $di_F/dt = 100 \text{ A}/\mu\text{s}$

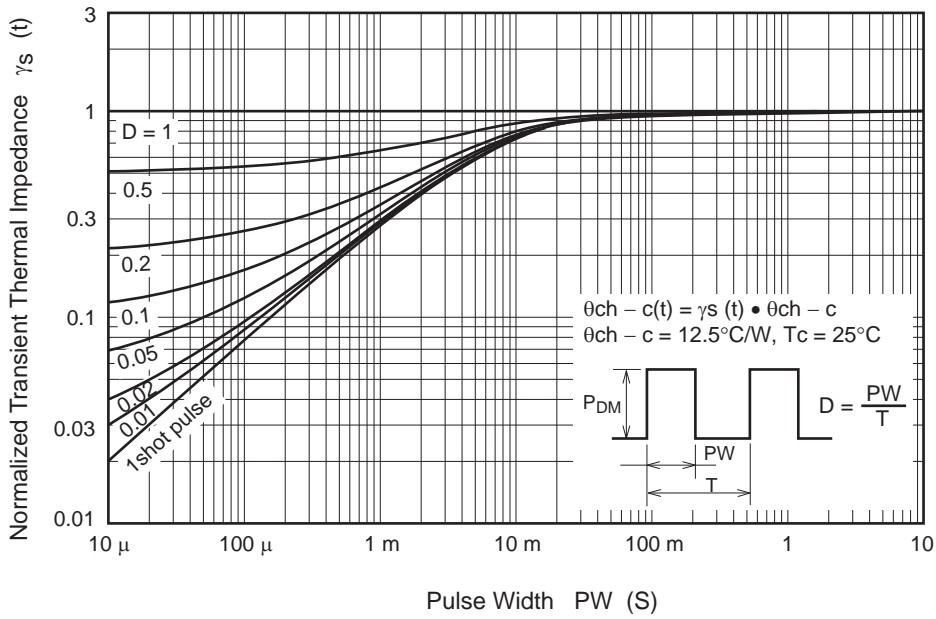
Notes: 4. Pulse test

Main Characteristics

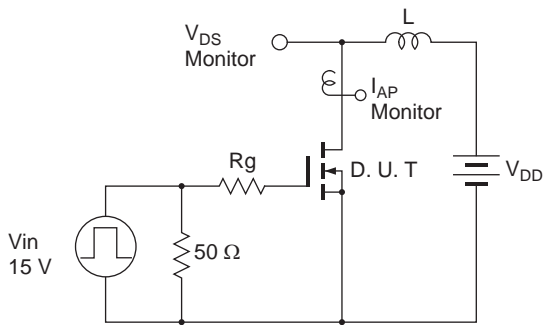




Normalized Transient Thermal Impedance vs. Pulse Width

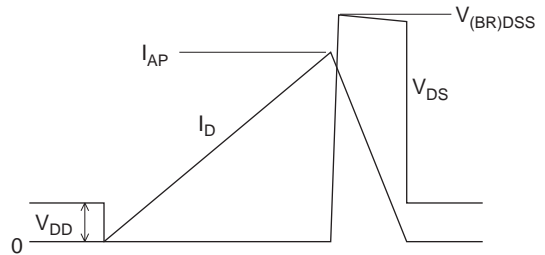


Avalanche Test Circuit

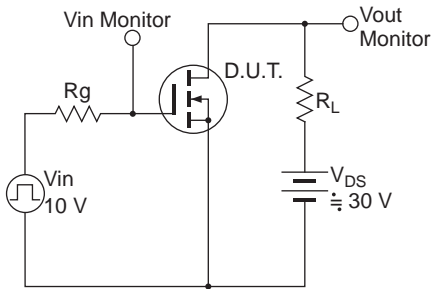


Avalanche Waveform

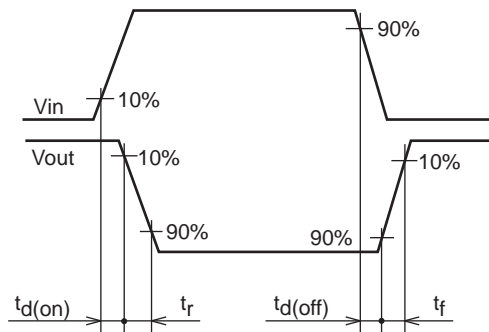
$$E_{AR} = \frac{1}{2} L \cdot I_{AP}^2 \cdot \frac{V_{DSS}}{V_{DSS} - V_{DD}}$$



Switching Time Test Circuit

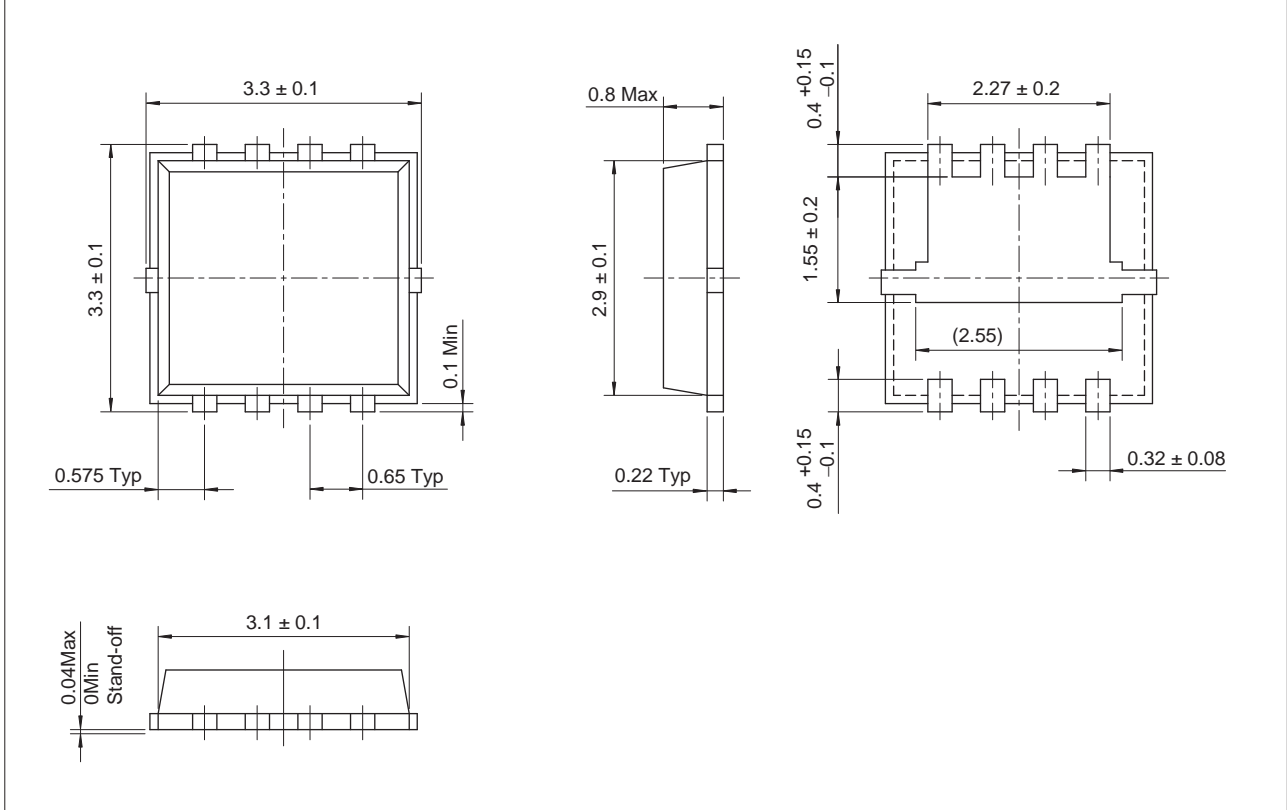


Switching Time Waveform



Package Dimensions

Package Name	JEITA Package Code	RENESAS Code	Previous Code	MASS[Typ.]
HWSO8-8	P-HWSO8-2.9x3.1-0.65	PWSN0008JB-A	—	0.022g



Ordering Information

Orderable Part Number	Quantity	Shipping Container
RJK1028DNS-00-J5	5000 pcs	Taping

Note: The symbol of 2nd "-" is occasionally presented as "#".

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