



Ultrafast, Precision Operational Amplifier

FEATURES

Low Distortion
Small-Signal Bandwidth 200MHz
Full Power Bandwidth 190MHz
Settling: 13ns to 0.1%
Offset Voltage +0.25mV: 3.4V/°C

Offset Voltage ±0.25mV; 3μV/°C Bias Current ±500nA; 20nA/°C

Power Dissipation Independent of Load

APPLICATIONS
Driving Flash Converters
High Speed DACs
Waveform Synthesis
Radar, IF Processors
Baseband and Video Communications
Photodiode Preamps
ATE/Pulse Generators
Imaging/Display Applications

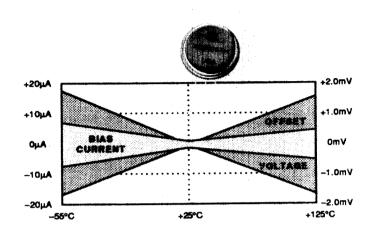
GENERAL DESCRIPTION

The AD9615 is a fast-settling, wide-bandwidth, dc-coupled operational amplifier that offers exceptional dynamic performance with a breakthrough in dc specifications/performance.

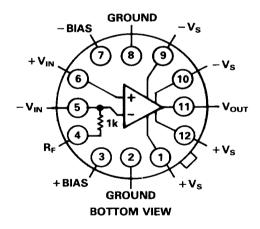
Rise and fall times are 2.6ns. The AD9615 settles to 0.1% in 13ns. With a 20MHz input signal, the 2nd harmonic is -59dBc; with a 1MHz input, the 2nd harmonic is -87dBc. The -3dB bandwidth is 200MHz (G=-5); the full-power bandwidth is 190MHz. Because the AD9615 utilizes current feedback, the bandwidth is independent of gain. Unlike many other current feedback amplifiers, dc accuracy is excellent. The input offset voltage and associated drift are 250 μ V and 3μ V/°C respectively. The inverting and noninverting bias currents are 500nA, drifting at 20nA/°C.

The AD9615 requires $\pm 5\text{V}$ power supplies and employs an innovative current-steering output stage that keeps the total circuit power dissipation essentially constant regardless of output drive. Circuit power dissipation does not increase as the load is increased; the unit can be operated up to $+116^{\circ}\text{C}$ in still air without heat sinking and up to $+125^{\circ}\text{C}$ with airflow.

Flat gain and phase response combine with excellent noise and distortion performance to provide a unity-gain-stable amplifier well suited to drive numerous types of A/Ds. The AD9615 is an excellent choice for driving the newest generation of ultrahigh speed flash converters when system SNR and effective number of bits are important. By limiting the bandwidth, the noise floor and distortion spurs drop so the AD9615 can be used in 14-bit, 2MHz systems.



The AD9615 utilizes discrete transistors with a custom IC fabricated on an Analog Devices advanced bipolar process. The AD9615BH is rated for case temperatures from -25°C to +85°C; the AD9615TH is guaranteed from -55°C to +125°C. Contact the factory for information about 883 grade parts. All units are built and tested in a MIL-STD-1772 certified facility.



AD9615 Functional Block Diagram

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SPECIFICATIONS

DC ELECTRICAL CHARACTERISTICS	$(\pm V_S = \pm 5V; A_V = -5; R_{IN} = 300\Omega; R_F = 1.5k\Omega; R_{LOAD} = 100\Omega$ unless otherwise specified)
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	1	THE MISE SHI	Υ	D0615BL	7 1	1 .	D9615T	ui ²	<u> </u>
	AD9615 AD9615BH¹ Sub- Typical Min/Max @			N N					
Parameter ^{1,2} (Conditions)	Group	@ +25°C	-25°C	+25°C	+85°C	−55°C	+25°C	+125°C	Units
√ Input Offset Voltage	1, 2, 3	±0.25	±1.8	± 1.0	± 1.6	±1.8	± 1.0	±1.6	mV
# Offset Voltage TC ³		±3				±8		± 8	μV/°C
Input Bias Current	-								
√ Inverting/Noninverting	1, 2, 3	±0.5	±8	±2	± 6.2	±8	± 2	± 6.2	μA
Input Bias Current TC ³									
# Inverting/Noninverting		±20				±60		± 60	nA/°C
/ Input Offset Current	1, 2, 3	±1	±8	± 2	± 6.2	±8	± 2	± 6.2	μΑ
Offset Current TC ³		±10	1			±60		± 60	nA/°C
Noninverting		ļ							
Impedance		200				1			kΩ
Capacitance		3.5							pF
✓ Common-Mode Input Range	1, 2, 3	±1.5	±1.4	± 1.25	± 1.1	±1.4	±1.25	± 1.1	v
/ Internal Feedback Resistor (R _E)	1, 2, 3	1500	1481/	1485/	1481/	1481/	1485/	1481/	Ω
(-II)	-,-,-		1519	1515	1519	1519	1515	1519	
# R _F Temperature Coefficient			±25	_	±25	±25	-	±25	ppm/°C
Common-Mode Rejection Ratio (CMRR) ⁴	4, 5, 6	44	≥34	≥38	≥ 36	≥34	≥38	= 36	dB
Common-Mode Sensitivity (CMS) ⁵	', -, -			- 0					1
Referred to Input									
-CMS	4, 5, 6	5	≤10	≲8	≤10	≤10	≤8	≤10	μΑ/V
+CMS	4, 5, 6	5	≤10 ≤10	≤8	≤10 ≤10	=10 ≤10	=8 ≤8	=10 ≤10	μA/V
Output Impedance (dc to 1MHz)	7, 5, 0	0.01	-10	_0	_10	_10	_0	10	Ω
Output Impedance (at to 1MHz) Output Impedance (at 100MHz)	-	0.4/18							Ω/nH
	1, 2, 3	±3.6	≥±3.0	≥±3.0	≥±2.7	≥±3.0	≥±3.0	≥±2.7	V
	1, 2, 3	±45	≥±40	≥±40	$\geq \pm 40$	≥±40	≥±40	$\geq \pm 40$	mA
Output Current (Continuous)		>3.2	≥1.4	≥±40 ≥1.8	≥1.9	≥1.4	≥±40 ≥1.8	≥±40 ≥1.9	ΜΩ
# Open Loop Transimpedance Gain (100Ω Load)	1 2 2	i	≥1.4 ≤72	≥1.6 ≤68	≥1.9 ≤72	≤1.4 ≤72	≥1.6 ≤68	≥1.9 ≤72	mA
+ Supply Current (+5V) ⁶	1, 2, 3	65	≤72 ≤76	≤08 ≤72	≤72 ≤76	≤72 ≤76	≤08 ≤72	≤72 ≤76	l .
✓ – Supply Current (−5V) ⁶	1, 2, 3	69	1			į.			mA
Power Consumption ⁶	1.5.	670	≤735	≤700 > 40	≤735 > 40	≤735	≤700 ≈ 40	≤735 ≈ 40	mW
Power Supply Rejection Ratio $(\Delta V_S = 0.5V)^4$	4, 5, 6	49	≥40	≥ 40	≥40	≥40	≥40	≥40	dB
√ Power Supply Sensitivity (PSS) ⁷									
Referred to Input				- 4					
$-PSS (\Delta - V_S = 0.5V)$	4, 5, 6	3	≤6	≤6	≤6 < 0	≤6	≤6 <0	≤6	μA/V
$+PSS (\Delta + V_S = 0.5V)$	4, 5, 6	3	≤8	≤8	≤8	≤8	≤8	≤8	μA/V
AC ELECTRICAL CHARACTERI	20172	$(\pm V_s = \pm $	5V; A _V =	-5; R _{IN}	$=300\Omega$	$R_{\rm F}=1.3$	5k Ω ; R $_{ extsf{L}0}$	_{PAD} = 100 €	2
	T	unless ot	T	•		T			I
$\sqrt{\text{Bandwidth } (-3dB) (V_{OUT} = 2V \text{ p-p})}$	9, 10, 11	>200	≥150	≥150	≥130	≥150	≥150	\geq 130	MHz
# Full Power Bandwidth ($V_{OUT} = 4V \text{ p-p}$;									
$R_L = 50\Omega$)		>190	≥140	≥140	≥120	≥140	\geq 140	≥ 120	MHz
Slew Rate $(V_{OUT} = 4V p-p)$		1400							V/µs
Amplitude of Peaking:									
$\sqrt{\text{dc to } 75\text{MHz} (V_{OUT} = 2\text{V p-p})}$	9, 10, 11	0	0.2	0.2	0.4	0.2	0.2	0.4	dB
$\sqrt{}$ >75MHz ($V_{OUT} = 2V p-p$)	9, 10, 11	0	≤0.5	≤0.6	≤1.6	≤0.5	≤0.6	≤1.6	₫B
$\sqrt{\text{Gain Roll-Off }(50\text{MHz; V}_{\text{OUT}} = 2\text{V p-p})}$	9, 10, 11	≤0.2	≤0.5	≤0.5	≤0.5	≤0.5	≤0.5	≤0.5	dB
Phase Nonlinearity (dc to 80MHz)		1							degree
Rise/Fall Time ($V_{OUT} = 3V \text{ Step}$)		2	≤2.5	≤2.5	≤2.7	≤2.5	≤2.5	≤2.7	ns
Settling Time to 1% ($V_{OUT} = 1.5V$ Step)		8	≤14	≤14	≤14	≤14	≤14	≤14	ns
Settling Time to 0.1% ($V_{OUT} = 3V$ Step;									
$R_L = 50\Omega$)		13	≤18	≤18	≤18	≤18	≤18	≤18	ns
Overshoot Amplitude ($V_{OUT} = 3V \text{ Step}$)		5							%
Overdrive Recovery to 1% (2 × FS; 50ns)									
Positive Rail to Linear Region		20							ns
Negative Rail to Linear Region		50							ns
# Propagation Delay		2.6	≤3.1	≤3.1	≤3.3	≤3.1	≤3.1	≤3.3	ns
$\sqrt{}$ 2nd Harmonic Distortion (f = 20MHz;	9, 10, 11	62	≥54	=5.1 ≥54	5.5 ≥49	≥54	=5.1 ≥54	 ≥ 4 9	dB
$V_{OUT} = 2V p-p$	-, -, -, -1		1						
VOUT - 2 V P-P)	l	1	1						

		Sub-	AD9615 Typical	AD9615BH¹ Min/Max @		AD9615TH ² Min/Max @				
	Parameter ^{1,2} (Conditions)	Group	@ +25°C	−25°C	+25°C	+85°C	−55°C	+25°C	+125°C	Units
#	3rd Harmonic Distortion (f = 20MHz; V _{OUT} = 2V p-p)		65	≥58	≥58	≥53	≥58	≥58	≥53	dB
\vee	Total Harmonic Distortion ($f = 20MHz$; $V_{OUT} = 2V p-p$)	9, 10, 11	60	≥53	≥53	≥48	≥53	≥53	≥48	dB
#	Noise Voltage (5MHz to 200MHz)		1.5	≤2.0	≤2.0	≤2.5	≤2.0	≤2.0	≤2.5	nV/√Hz
#	Noise Current (5MHz to 200MHz)		15	≤18	≤18	≤22	≤18	≤18	≤22	pA/√Hz
#	Equivalent Integrated Input Noise (5MHz to 200MHz)		34	≤42	≤42	≤55	≤42	≤42	≤55	μV
OT	HER INFORMATION									
(rmal Impedance, Case to Ambient, $\theta_{\text{CA}}^{8,9}$ Still Air; No Heat Sink) rmal Impedance, Case to Ambient, $\theta_{\text{CA}}^{8,9}$		50	Manage de la constante de la c						°C/W
,	600 LFPM Air; No Heat Sink)		30							°C/W
(BF (Mean Time Between Failures) $\Gamma_{\text{CASE}} = 70^{\circ}\text{C}$; Ground Fixed; er MIL-HDBK-217D)		2.38× 10 ⁶	MAX PROPERTY OF THE PROPERTY O						hours

NOTES

100% tested (See Notes 1 and 2).

Specification guaranteed by design; not tested

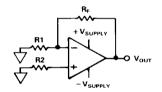
¹AD9615BH parameters preceded by a check (\(\circ\) are tested at +25°C ambient temperature; performance is guaranteed over the industrial case temperature range $(-25^{\circ}C$ to $+85^{\circ}C$).

²AD9615TH parameters preceded by a check (\(\chi\)) are tested at -55°C case, +25°C ambient and +125°C case temperatures. Contact factory about units processed to MIL-STD-883. Subgroup information applies only to 883 parts.

Offset voltage, bias current and offset current TCs are guaranteed over the respective temperature ranges.

 4 CMRR and PSRR apply only for stated conditions; $\Delta VS = 0.5V$.

⁵CMS values can be used to determine the CMRR for specific gain settings according to the following worst case relationships:



$$\begin{split} \Delta V_{OUT} &= [-CMS] \, (R_F) \, [\Delta V_{CM}] \, + \, [+CMS] \, [R2] \, \bigg[\, 1 \, + \, \frac{R_F}{R1} \, \bigg] \, [\Delta V_{CM}] \\ &\quad \text{where } \Delta V_{CM} \, = \, \Delta - V_{SUPPLY} \, = \, \Delta + V_{SUPPLY} \\ &\quad CMRR \, = \, -20 \, LOG \, \bigg[\, \frac{\Delta V_{OUT}}{(\Delta V_{CM})} \, \bigg] \end{split}$$

⁶Supply current and power dissipation are for quiescent operation (V_{IN} = 0V). A proprietary output stage assures total circuit power dissipation does not increase as a function of output current and R_{LOAD}. (See Thermal Considerations text.)

PSS values can be used to determine the PSRR for specific gain settings according to the following worst case relationships (See diagram in 5):

$$\begin{split} \Delta V_{OUT} &= \text{[-PSS]}\left[R_{\text{F}}\right] \left[\Delta V_{\text{SUPPLY}}\right] + \text{[+PSS]}\left[R2\right] \left[1 + \frac{R_{\text{F}}}{R1}\right] \left[\Delta V_{\text{SUPPLY}}\right] \\ &\text{where } \Delta V_{\text{SUPPLY}} &= \Delta - V_{\text{SUPPLY}} \text{ or } \Delta + V_{\text{SUPPLY}} \\ &\text{PSRR} &= -20 \text{ LOG}\left[\frac{\Delta V_{\text{OUT}}}{\left(1 + \frac{R_{\text{F}}}{R1}\right) \left(\Delta V_{\text{SUPPLY}}\right)}\right] \end{split}$$

⁸Recommended maximum junction temperature is +165°C.

⁹Bottom of unit raised approximately 0.125" (3.2mm) above copper-clad board.

Specifications subject to change without notice.

EXPLANATION FOR GROUP A MILITARY SUBGROUPS

Subgroup 1 - Static tests at +25°C.

(10% PDA calculated against Subgroup 1 for high-rel

versions.)

Subgroup 2 - Static tests at maximum rated temperature.

Subgroup 3 - Static tests at minimum rated temperature.

Subgroup 4 - Dynamic tests at +25°C.

Subgroup 5 - Dynamic tests at maximum rated temperature.

Subgroup 6 - Dynamic tests at minimum rated termperature.

Subgroup 7 - Functional tests at +25°C.

Subgroup 8 - Functional tests at maximum and minimum rated temperatures.

Subgroup 9 - Switching tests at +25°C.

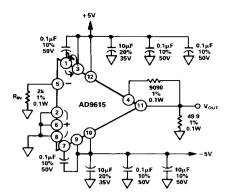
Subgroup 10 - Switching tests at maximum rated temperature.

Subgroup 11 - Switching tests at minimum rated temperature.

Subgroup 12 - Periodically sample tested.

ABSOLUTE MAXIMUM RATINGS

Supply Voltages $(\pm V_S)$ $\pm 6V$
Analog Input
Continuous Output Current
Operating Temperature Range (Case)
AD9615BH
AD9615TH
Power Dissipation See Thermal Model
Junction Temperature
Storage Temperature Range65°C to +150°C
Lead Temperature (Soldering, 10sec.)+300°C



This microcircuit is covered by Technology Group (I.) per MIL-M-38

AD9615 Life Test/Burn-In Circuit

OUTLINE DIMENSIONSDimensions shown in inches and (mm).

BOTTOM VIEW

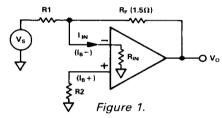
TO-8 STYLE CAN PINS ARE GOLD PLATED

THEORY OF OPERATION

The advantages of using the transimpedance AD9615 operational amplifier instead of a conventional high speed op amp are based on the difference in the way the two types of amplifiers operate.

The AD9615 operational amplifier uses current feedback, rather than the voltage feedback common to traditional amplifiers. Current feedback amplifiers provide significantly more bandwidth at given gain settings than traditional amplifiers do.

Both types are similar in terms of setting gain and calculating noise, but there is a major difference in the input stages. Traditionally, conventional amplifiers have two high impedance inputs. Within the AD9615, however, the inputs are connected



across a unity gain buffer, causing the noninverting input to be high impedance and the inverting input to be low impedance.

Under normal operating conditions, the inverting input current is very small. The AD9615 operation is similar to a traditional amplifier in that the voltage between the input terminals and the bias currents are, ideally, zero.

Closed-loop bandwidth (CLBW) of the AD9615 is first-order independent of its closed loop gain (G). Its transfer function can be expressed as:

$$rac{V_O}{V_S} \cong rac{G}{rac{R_F}{T_{(S)}} \left[1 + rac{R_{IN}}{R_1}
ight] + 1}$$

Where

 R_F is the internal feedback resistor ($R_F = 1.5k$)

RI is the gain-setting input resistor T(s) is the open loop transimpedance gain as a function of frequency (s) and is independent of gain-setting resistors

$$T(s) = -V_{O}(s)/I_{IN}(s)$$

 $G = -R_F /R1$ (closed-loop gain)

 $R_{\rm IN}$ is the open-loop input impedance (typically 18 in the 100-200~MHz band).

When closed-loop gain is greatly increased, CLBW is only slightly diminished because of the low input impedance of R_{IN} . The ratio of CLBW for a specified gain to CLBW at G=0 $(R1\rightarrow \infty)$ can be determined using the following relationship:

$$\frac{CLBW(G=x)}{CLBW(G=0)} \cong \frac{1}{\left(1 - \frac{R_{IN}}{R_F}G\right)} = \frac{1}{(1 - 0.012G)}$$

As an example, when G = -20, the CLBW will be 80% of the CLBW when G = 0 (typically 215MHz).

In the AD9615, R_F is internal and has a value of $1.5k\Omega$; this design helps reduce the effect of stray capacitances and makes it easier to apply the amplifier. The low input impedance at the inverting input means all of the input signal voltage is impressed across R1; this causes a direct voltage-to-current conversion to take place.

Using only the feedback resistor within the unit means AD9615 gain can be set by varying only R1. Changing the value of the feedback resistor is covered below.

APPLYING THE AD9615 OP AMP

When applying the AD9615 op amp, there are certain precautions which must be observed to protect the unit from damage:

- Shorting any power supply to the output will destroy the device
- Shorting the output to ground will destroy the device; no internal protection is included.

The noninverting input of the AD9615 operational amplifier requires that it be driven from a low impedance source, or connected to a low impedance point when used in the inverting mode. Driving this input from a high impedance source will diminish ac performance.

NOISE AND DC CONSIDERATIONS

When calculating the noise and dc error reflected to the output of the AD9615, the difference in impedance at the inverting and noninverting inputs must be considered. With this exception, the calculations are similar to those for standard differential input operational amplifiers.

The gain-setting and input resistors (see Figure 1), the specified inverting bias current (I_B-) , noninverting bias current (I_B+) , and input offset voltage (V_{OS}) can be used to determine the output offset voltage using the following equation:

$$V_O = -(I_B -)(R_F) + (I_B +)(R_2) \left(1 + \frac{R_F}{R_1}\right) \pm V_{OS} \left(1 + \frac{R_F}{R_1}\right)$$

For low noise and optimum frequency performance, bias-setting resistor R2 should be bypassed, or the noninverting input should be connected to ground.

See the AD9615 Inverting Operation and AD9615 Noninverting

Operation figures. When operating in the noninverting mode, R2 $(R_{MATCH}||R_{IN})$ should be $\leq 50\Omega$.

Approximate rms output noise voltage can be determined by using the graph entitled Noise Spectral Density vs. Frequency along with the equation shown below*. Based on the AD9615 Inverting Operation sketch:

$$V_O = (\sqrt{BW}) (\sqrt{4kTR_F(1-G) + V_n^2(1-G)^2 + I_n^2R_F^2})$$

Where

V_n = noise voltage spectral density

 $I_p =$ noise current spectral density

BW = noise bandwidth (Hz)

 $G = closed-loop gain = -R_F/R1$

 $R_F = feedback resistor (\Omega)$

 $k = Boltzmann's Constant = 1.381 \times 10^{-23} J/K$

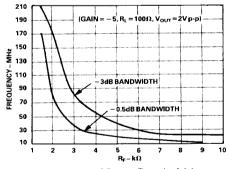
T = absolute temperature (degrees Kelvin)

Using External Feedback Resistors

The internal 1.5k feedback resistor (R_F) for the AD9615 was chosen for optimum ac performance at most gain settings. By including the resistor inside the package, parasitic capacitance is minimized, thus reducing peaking and extending the bandwidth. In some situations it is desirable to operate with an external feedback resistor (low capacitance, low inductance resistors such as part number PR8351 from Precision Resistive Products are necessary to optimize ac response). Care must be taken to understand the effects of the change on the dynamic performance of the AD9615.

Increasing R_F

The value of the feedback resistor controls the location of the closed-loop dominant pole. As the feedback resistor is increased, the bandwidth for a given gain setting decreases. Conversely, if $R_{\rm F}$ is reduced, the bandwidth increases, phase margin diminishes, possibly resulting in instability. Care must be taken to prevent oscillations induced by lower value feedback resistors; however, bandwidth can be extended in higher gain settings by utilizing a lower value $R_{\rm F}$.



Effect of R_F on Bandwidth

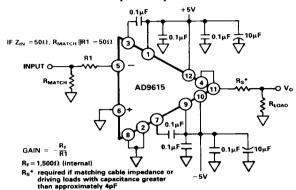
Low-reactance external feedback resistors should be used to optimize ac performance. To minimize the effective shunt capacitance in the feedback loop, two or more resistors can be used in series to obtain higher values of $R_{\rm F}$. Using the internal feedback resistor in series with an external resistor is advisable in some applications (where resistor tempco cancellation is not required).

SUGGESTED LAYOUT

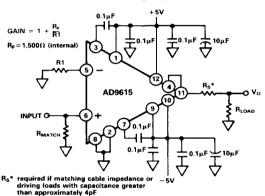
Good layout practices are always crucial to realize the full potential of the AD9615. A large ground plane is strongly recommended. The ground plane provides a low impedance path for

all power supply and signal currents and suppresses EMI.

Ceramic $0.1\mu F$ decoupling capacitors should be placed as close as possible (preferably less than 0.1'') to the specified pins shown in the following diagrams. The $(10\mu F)$ tantalum capacitors for additional decoupling of each power supply should be placed within one inch of their specified pins.



AD9615 Inverting Operation



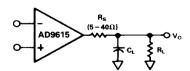
AD9615 Noninverting Operation

Run lengths must be kept as short as possible; if the signal path must be longer than two or three inches, use terminated coaxial cable and/or microstrip techniques. Impedance mismatches will cause signal reflections and system distortion. Parasitic capacitance associated with ZIF (and other) device sockets will severely degrade the performance of the AD9615; if sockets must be used, individual pin sockets for each lead are strongly encouraged.

Output impedance of the driving source should equal $R_{MATCH} \| R1$ (inverting mode) or R_{MATCH} (noninverting mode). A suggested layout is shown on the last page of this data sheet.

LOAD CONSIDERATIONS

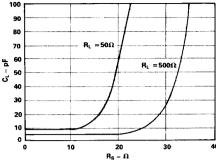
The best high-frequency performance of the AD9615 is achieved when total output capacitance (C_L) is minimized. Realistically, this is not always possible (as when driving flash converters); but performance can be improved if a series resistor is used at the output of the amplifier, as shown below.



Isolating Capacitive Loads

^{*}Assumes source (driving) resistance = 0.

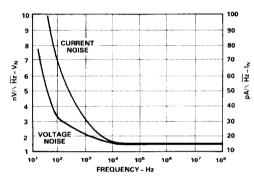
A series isolation resistor will be required for driving capacitive loads >8pF (if $R_L = 50$) and >4pF (if $R_L = 500$).



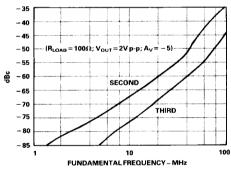
Output Capacitance vs. Compensation

AD9615 PERFORMANCE

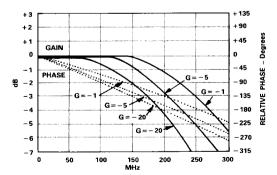
The following graphs and drawings provide additional information on the performance of the AD9615 operational amplifier. The data shown are based on typical characteristics.



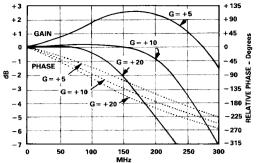
Noise Spectral Density vs. Frequency



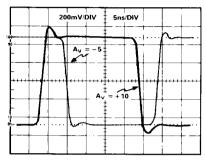
Harmonic Distortion vs. Frequency



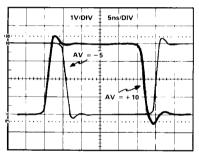
Gain and Phase vs. Frequency - Inverting



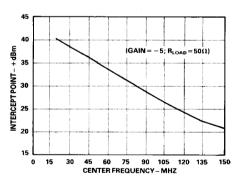
Gain and Phase vs. Frequency - Noninverting



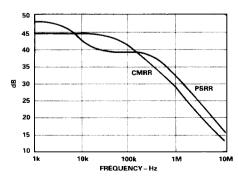
Small-Signal Pulse Response



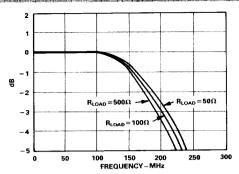
Large-Signal Pulse Response



3rd Order Two-Tone Intermod Intercept



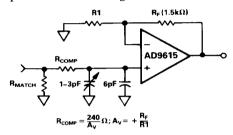
AD9615 CMRR and PSRR



Bandwidth vs. R_{LOAD} ($A_V = -5$)

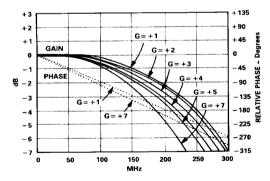
NONINVERTING LOW GAINS

Because of parasitic capacitance on the inverting input, peaking is an inherent result when operating the AD9615 in noninverting low gain configurations ($A_V \le +8$). Peaking response can be eliminated by connecting a low-pass RC network to the noninverting input node. See the diagram below.



Gain/Frequency Noninverting Compensation

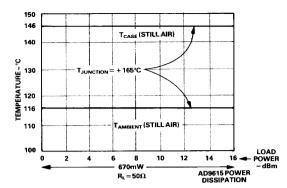
In the circuit, a 6pF capacitor should be used in parallel with a 1-3pF variable capacitor. The variable component should be adjusted until the desired frequency response is obtained. The diagram below illustrates the results. (See graph of uncompensated gain vs. frequency for comparison.)



Gain vs. Frequency, Compensated - Noninverting

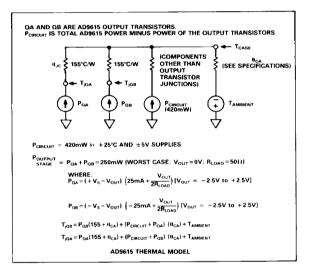
AD9615 THERMAL CONSIDERATIONS

The following chart illustrates an important characteristic of the AD9615 amplifier. A proprietary design feature of the output stage assures that power dissipation and case temperature remain constant regardless of the amount of output power delivered by the amplifier. The AD9615 power dissipation remains approximately constant when driving resistive loads between 50Ω and 150Ω , in marked contrast to most conventional operational amplifiers in which heavier loads mean more power dissipation, higher case temperatures and less reliability.



Temperature/Power Dissipation vs. Output Power/Load

This unique feature means that no heat sinking is required in still air at ambient temperatures as high as +116°C; with air flow of 500 LFPM, the device can be operated to +125°C before heat sinking is necessary.

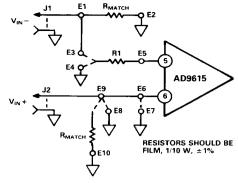


AD9615 LAYOUT INFORMATION

The suggested layout of the AD9615 shown as follows is based on the proven performance of the AD9611/AD9615 Evaluation Board. The user is urged to use a similar layout when incorporating the amplifier into the system in which it will operate. Evaluation boards are available from Analog Devices; the AD9615 and AD9611 evaluation boards are identical.

In the layout, resistors are film; 0.1W; $\pm 1\%$; 50ppm. Capacitors C1 and C2 are tantalum; $10\mu F$; 20%; 35V. C3–C8 are ceramic; $0.1\mu F$; 20%; 50V. Connectors J1–J3 are Amphenol BNC type; pin sockets are available from Amp as part number 6-330808-3 (open end).

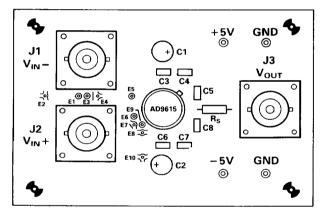
The input connections shown below are based on the layout of the evaluation board. Refer to earlier figures (inverting operation and noninverting operation) for schematic details.



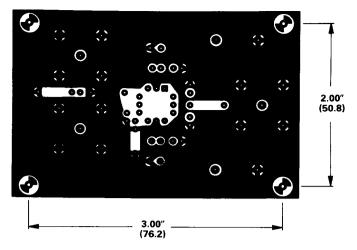
Suggested Layout Input Connections

Operating Mode	Connect	Between
Inverting	R _{MATCH}	E1 and E2
	R1	E3 and E5
	Strap Strap	E6 andE7
	Strap	E8 and E9
Noninverting	R1	E4 and E5
	R_{MATCH}	E9 and E10

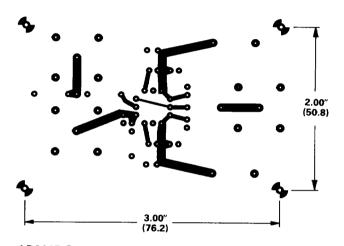
Table II



AD9615 Suggested Layout Component Side, Viewed from Top



AD9615 Suggested Layout Component Side (Top) Viewed from Top



AD9615 Suggested Layout Solder Side (Bottom) Viewed from Top