



UTC4013

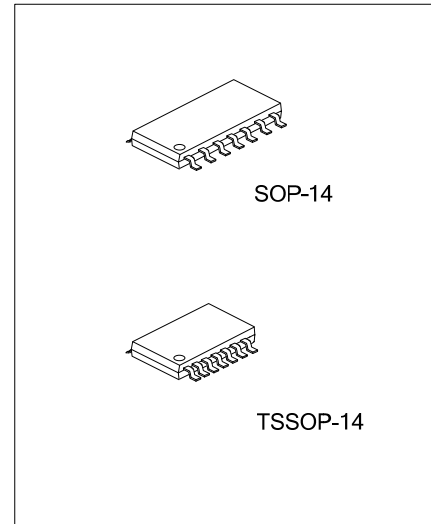
Preliminary

CMOS IC

DAUL D-TYPE FLIP-FLOP

DESCRIPTION

The UTC4013 is a dual D-type flip-flop which has two independent circuits and each flip-flop features independent data, set, reset, and clock inputs and outputs. The input level applied to DATA input are transferred to Q and \bar{Q} output by rising edge of the clock pulse. When SET input is "H", and RESET input is "L", outputs become Q="H" and \bar{Q} ="L". When SET input is "L" and RESET input is "H", outputs become Q="L" and \bar{Q} ="H". When both SET input and RESET input are at "H", outputs become Q="H" and \bar{Q} ="H".



FEATURES

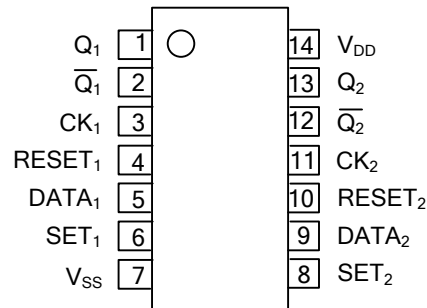
- * Power supply voltage 3V to 18V
- * Maximum Input Current of 1uA at 18V Over Full Package Temperature
- * Maximum quiescent supply current is 4μA

ORDERING INFORMATION

Ordering Number		Package	Packing
Lead Free	Halogen Free		
UTC4013L-S14-R	UTC4013G-S14-R	SOP-14	Tape Reel
UTC4013L-P14-R	UTC4013G-P14-R	TSSOP-14	Tape Reel

<p>UTC4013L-S14-R</p> <p>(1) Packing Type (2) Package Type (3) Lead Free</p>	<p>(1) R: Tape Reel (2) S14: SOP-14, P14: TSSOP-14 (3) G: Halogen Free, L: Lead Free</p>
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■ PIN CONFIGURATION

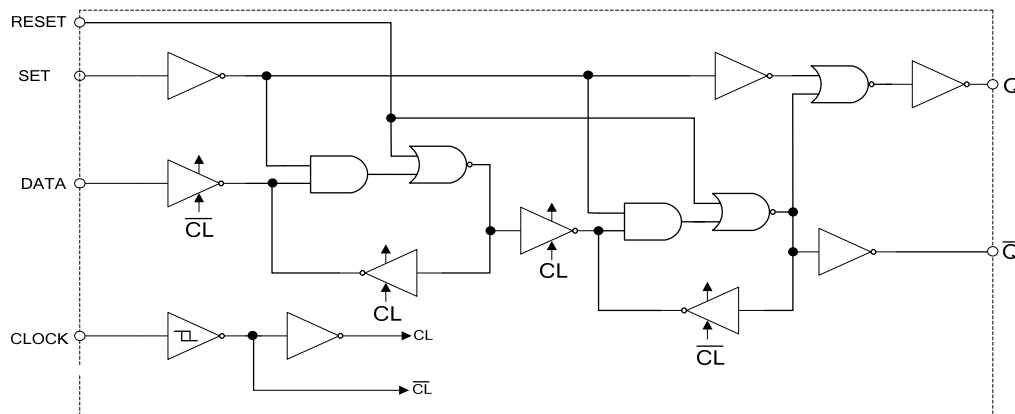


■ FUNCTION TABLE

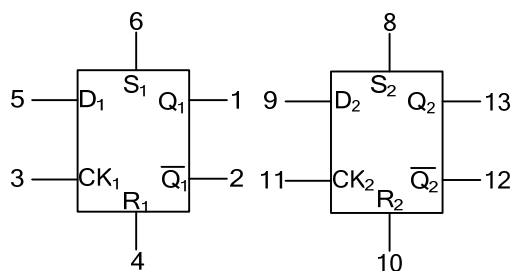
INPUTS				OUTPUTS	
RESET	SET	DATA	CK*	Q _{n+1}	\bar{Q}_{n+1}
L	H	-	-	H	L
H	L	-	-	L	H
H	H	-	-	H	H
L	L	L		L	H
L	L	H		H	L
L	L	-		No Change	No Change

Note: - : Don't care
* : Level Change

■ LOGIC DIAGRAM



■ BLOCK DIAGRAM



■ ABSOLUTE MAXIMUM RATING ($T_A = 25^\circ\text{C}$, unless otherwise specified)

PARAMETER	SYMBOL	RATINGS	UNIT
DC Supply Voltage	V_{DD}	$V_{SS}-0.5$ to $V_{SS}+20$	V
Input Voltage	V_{IN}	$V_{SS}-0.5$ to $V_{DD}+0.5$	V
Output Voltage	V_{OUT}	$V_{SS}-0.5$ to $V_{DD}+0.5$	V
DC Input Current	I_{IN}	± 10	mA
Power Dissipation	P_D	500	mW
Operation Temperature	T_{OPR}	-40 ~ +85	$^\circ\text{C}$
Storage Temperature	T_{STG}	-65 ~ +150	$^\circ\text{C}$

Note: Absolute maximum ratings are those values beyond which the device could be permanently damaged.

Absolute maximum ratings are stress ratings only and functional device operation is not implied.

■ RECOMMENDED OPERATING CONDITIONS ($V_{SS}=0, T_A=25^\circ\text{C}$)

PARAMETER	SYMBOL	RATINGS	UNIT
DC Supply Voltage	V_{DD}	3 ~ 18	V
Input Voltage	V_{IN}	0 ~ V_{DD}	V

■ D.C. CHARACTERISTICS ($V_{SS}=0, T_A=25^\circ\text{C}$)

PARAMETER		SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Input Voltage	High	V_{IH}	$V_{OUT}=0.5\text{V}, 4.5\text{V}; V_{DD}=5\text{V}, I_{OUT} < 1\mu\text{A}$	3.5	2.75		V
			$V_{OUT}=1.0\text{V}, 9.0\text{V}; V_{DD}=10\text{V}, I_{OUT} < 1\mu\text{A}$	7.0	5.5		
			$V_{OUT}=1.5\text{V}, 13.5\text{V}; V_{DD}=15\text{V}, I_{OUT} < 1\mu\text{A}$	11.0	8.25		
	Low	V_{IL}	$V_{OUT}=0.5\text{V}, 4.5\text{V}; V_{DD}=5\text{V}, I_{OUT} < 1\mu\text{A}$		2.25	1.5	
			$V_{OUT}=1.0\text{V}, 9.0\text{V}; V_{DD}=10\text{V}, I_{OUT} < 1\mu\text{A}$		4.50	3.0	
			$V_{OUT}=1.5\text{V}, 13.5\text{V}; V_{DD}=15\text{V}, I_{OUT} < 1\mu\text{A}$		6.75	4.0	
Output Voltage	High	V_{OH}	$V_{IN}=V_{SS}, V_{DD}; I_{OUT} < 1\mu\text{A}; V_{DD}=5\text{V}$	4.95	5.00		V
			$V_{IN}=V_{SS}, V_{DD}; I_{OUT} < 1\mu\text{A}; V_{DD}=10\text{V}$	9.95	10.00		
			$V_{IN}=V_{SS}, V_{DD}; I_{OUT} < 1\mu\text{A}; V_{DD}=15\text{V}$	14.95	15.00		
	Low	V_{OL}	$V_{IN}=V_{SS}, V_{DD}; I_{OUT} < 1\mu\text{A}; V_{DD}=5\text{V}$		0.00	0.05	
			$V_{IN}=V_{SS}, V_{DD}; I_{OUT} < 1\mu\text{A}; V_{DD}=10\text{V}$		0.00	0.05	
			$V_{IN}=V_{SS}, V_{DD}; I_{OUT} < 1\mu\text{A}; V_{DD}=15\text{V}$		0.00	0.05	
Input Current	High	I_{IH}	$V_{IH}=18\text{V}, V_{DD}=18\text{V}$		10^{-5}	0.1	uA
	Low	I_{IL}	$V_{IL}=0\text{V}, V_{DD}=18\text{V}$		-10^{-5}	-0.1	
Output Current	High	I_{OH}	$V_{OH}=4.6, V_{IN}=V_{SS}, V_{DD}; V_{DD}=5\text{V}$	-0.51	-1.0		mA
			$V_{OH}=2.5, V_{IN}=V_{SS}, V_{DD}; V_{DD}=5\text{V}$	-2.10	-4.0		
			$V_{OH}=9.5, V_{IN}=V_{SS}, V_{DD}; V_{DD}=10\text{V}$	-1.30	-2.2		
			$V_{OH}=13.5, V_{IN}=V_{SS}, V_{DD}; V_{DD}=15\text{V}$	-3.40	-9.0		
	Low	I_{OL}	$V_{OL}=0.4, V_{IN}=V_{SS}, V_{DD}; V_{DD}=5\text{V}$	0.51	1.2		
			$V_{OL}=0.5, V_{IN}=V_{SS}, V_{DD}; V_{DD}=10\text{V}$	1.30	3.2		
$V_{OL}=1.5, V_{IN}=V_{SS}, V_{DD}; V_{DD}=15\text{V}$			3.40	12.0			
Quiescent Supply Current		I_{DD}	$V_{IN}=V_{SS}, V_{DD}(\text{Note}); V_{DD}=5\text{V}$		0.002	1	uA
			$V_{IN}=V_{SS}, V_{DD}(\text{Note}); V_{DD}=10\text{V}$		0.004	2	
			$V_{IN}=V_{SS}, V_{DD}(\text{Note}); V_{DD}=15\text{V}$		0.008	4	

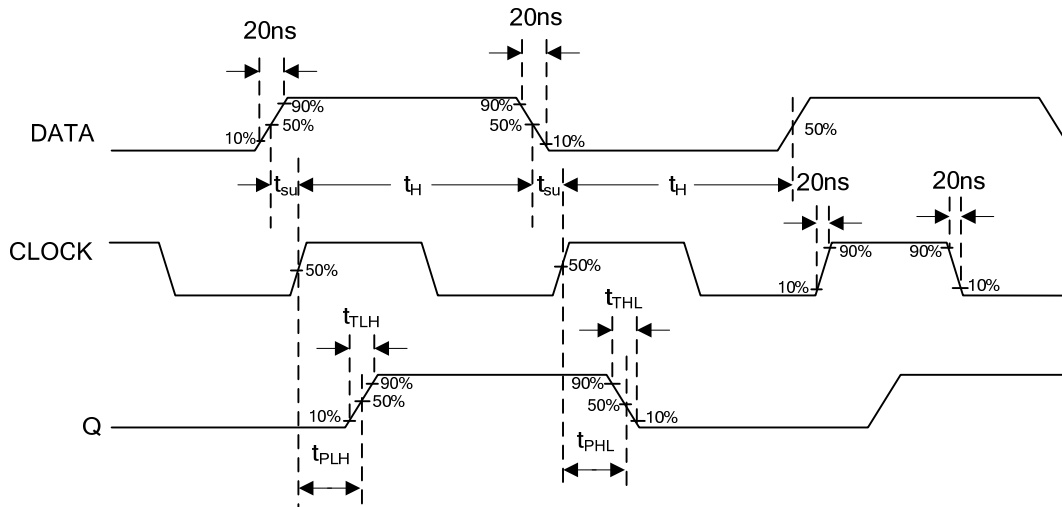
Note: All valid input combinations.

■ A.C. CHARACTERISTICS ($V_{SS}=0$, $T_A=25^\circ\text{C}$, $C_L=50\text{pF}$)

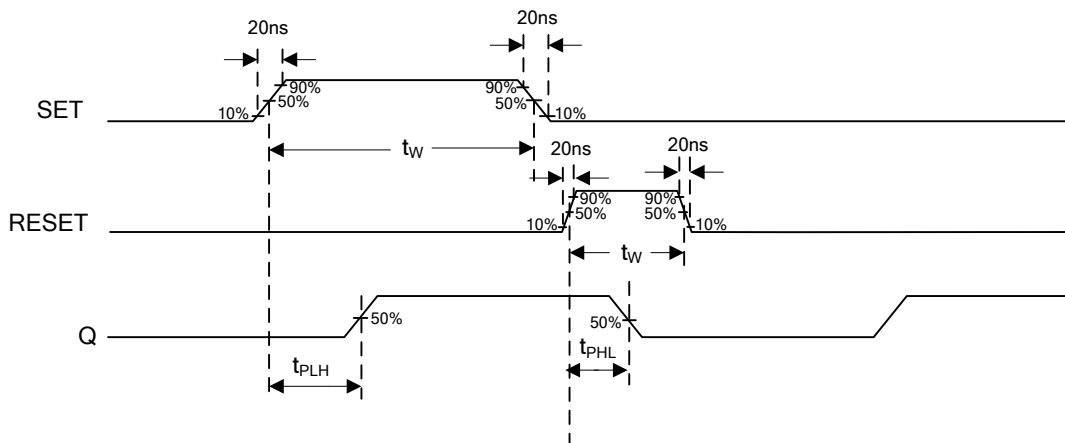
PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT	
Output Transition Time	Low to High	t_{TLH}	VDD=5V		70	200	ns
		VDD=10V		35	100		
		VDD=15V		30	80		
	High to Low	t_{THL}	VDD=5V		70	200	
		VDD=10V		35	100		
		VDD=15V		30	80		
Propagation Delay Time (CK – Q, \bar{Q})	t_{pLH}	VDD=5V		130	300	ns	
		VDD=10V		65	130		
		VDD=15V		50	90		
Propagation Delay Time (SET, RESET – Q, \bar{Q})	t_{pLH}	VDD=5V		110	300		ns
		VDD=10V		50	130		
		VDD=15V		40	90		
	t_{pHL}	VDD=5V		110	300		
		VDD=10V		50	130		
		VDD=15V		40	90		
Max. Clock Frequency	f_{CL}	VDD=5V	3.5	8.0		MHz	
		VDD=10V	8.0	16.0			
		VDD=15V	12.0	20.0			
Max. Clock Input Rise Time	t_{rCL}	VDD=5V	No Limit			μs	
		VDD=10V					
		VDD=15V					
Max. Clock Input Fall Time	t_{fCL}	VDD=5V	No Limit			μs	
		VDD=10V					
		VDD=15V					
Min. Pulse Width (SET, RESET)	t_w	VDD=5V		60	180	ns	
		VDD=10V		30	80		
		VDD=15V		25	50		
Min. Clock Pulse Width	t_w	VDD=5V		60	140		
		VDD=10V		30	60		
		VDD=15V		25	40		
Min. Set-up Time (DATA - CK)	t_{su}	VDD=5V			40	ns	
		VDD=10V			20		
		VDD=15V			15		
Min. Hold Time (DATA-CK)	t_H	VDD=5V		20	40		
		VDD=10V		10	20		
		VDD=15V		6	15		
Min. Removal Time (SET, RESET-CK)	t_{rem}	VDD=5V			40		
		VDD=10V			20		
		VDD=15V			15		
Input Capacitance	C_{IN}			5	7.5	pF	

■ PARAMETER MEASUREMENT INFORMATION

1. DATA-CLOCK, Q



2. SET-RESET, Q



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