SY88216L

3.3V, 2.5Gbps Burst Mode Laser Driver

General Description

The SY88216L is a single supply 3.3V burst mode laser driver for A-PON, B-PON, EPON, GE-PON, and G-PON applications with data rates from 155Mbps up to 2.5Gbps. The driver can deliver modulation current up to 85mA, and provides a high compliance voltage that makes it suitable for high-current operation with the laser DC-coupled to it.

All support documentation can be found on Micrel's web site at: www.micrel.com.

Features

- 2.4V minimum laser compliance voltage
- Operation up to 2.5Gbps
- Fast burst mode enable/disable delay
- Modulation current up to 85mA
- Bias current up to 70mA
- Infinite bias current hold time between bursts
- Safety features
- Power monitoring
- Available in 24-pin (4mm x 4mm) QFN package

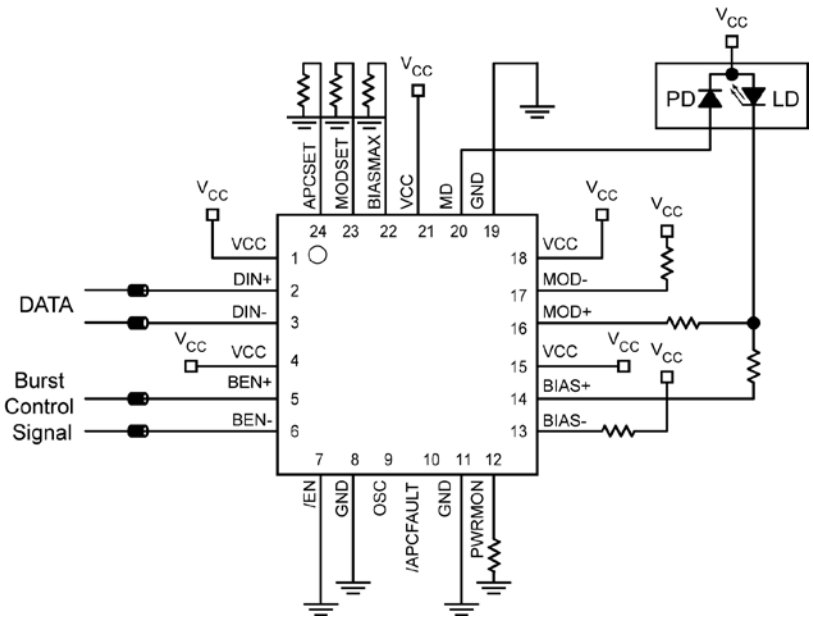
Applications

- Multi-rate burst mode applications: A-PON, B-PON, G-PON, E-PON, GE-PON

Markets

- Fiber-to-the-Premises (FTTP): Fiber-to-the-Home (FTTH), Fiber-to-the-Business (FTTB)
- FTTC (Fiber-to-the-Curb)

Typical Application



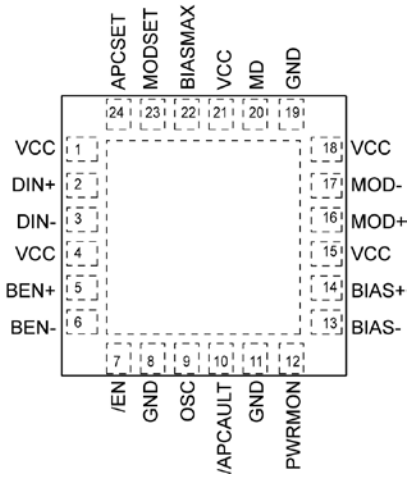
Ordering Information[1]

Part Number	Package Type	Operating Range	Package Marking	Lead Finish
SY88216LMG	QFN-24	Industrial	216L with Pb-Free bar-line indicator	NiPdAu Pb-Free
SY88216LMGTR[2]	QFN-24	Industrial	216L with Pb-Free bar-line indicator	NiPdAu Pb-Free

Notes:

1. Contact factory for die availability. Dice are guaranteed at T_A = +25°C, DC Electrical only.
2. Tape and Reel.

Pin Configuration



24-Pin QFN

Pin Description

Pin Number	Pin Name	Pin Function
2	DIN+	Non-inverting input data. Internally terminated with 50Ω to a reference voltage.
3	DIN-	Inverting input data. Internally terminated with 50Ω to a reference voltage.
5	BEN+	Non-inverting burst enable. Accepts any input, single-ended or differential: TTL/CMOS, LVPECL, CML, LVDS, HSTL, and SSTL. BEN requires an external termination. See Figure 2.
6	BEN-	Inverting burst enable. Accepts any input, single-ended or differential: TTL/CMOS, LVPECL, CML, LVDS, HSTL, and SSTL. BEN requires an external termination. See Figure 2.
7	/EN	Active low TTL/CMOS. Internally pulled-up. Pull-down with a 22kΩ or lower resistance or apply a low level signal (<0.8 V) to enable bias and modulation. Keep floating or apply a high level (>2 V) to disable.
9	OSC	Internal oscillator setting option. Install a 0Ω resistor from this pin to VCC or leave it open to set the frequency. Refer to the frequency table.
10	/APCFAULT	Indicates APC failure when low. Active low TTL/CMOS.
12	PWRMON	Power Monitor. Provides a current which is proportional to the sum of bias current and half of modulation current. Install a resistor between this pin and GND to convert that current to a voltage.
13	BIAS-	Inverting laser bias current output. Pull-up to VCC with a resistor.
14	BIAS+	Non-inverting laser bias current output, sources current when BEN is high. Connect to the cathode of the laser through a resistor.
16	MOD+	Non-inverted modulation current output. Provides modulation current when input data is positive.
17	MOD-	Inverted modulation current output. Provides modulation current when input data is negative.
20	MD	Input from the laser monitoring photodiode. Connect to the anode of the photodiode for APC operation.
22	BIASMAX	Install a resistor between this pin and GND to set the maximum bias current for the closed loop operation. The APC loop controls the bias current up to the level of BIASMAX. When the bias current reaches the maximum value set through this pin, the driver continues to sink a current equal to this maximum. For open loop operations, this pin sets the bias current.
23	MODSET	Modulation current setting and control. The modulation current is set by installing an external resistor from this pin-to-ground or using a current source.
24	APCSET	Bias current setting and control. The bias current is set by installing an external resistor from this pin to ground or using a current source. Connect a 50K resistor-to-GND for open loop operation.
8, 11,19	GND	Ground. Ground and exposed pad must be connected to the plane of the most negative potential.
1, 4, 15, 18, 21	VCC	Supply Voltage. Bypass with a 0.1µF//0.01µF low ESR capacitor as close to VCC pin as possible.

Truth Table

DIN+	DIN-	/EN	MOD+[1]	MOD-	Laser Output[2]
L	H	L	H	L	L
H	L	L	L	H	H
X	X	H	H	L	L

Notes:

1. I_{MOD} = 0 when MOD+ = H.
2. Assuming that the laser is tied to MOD+.

Oscillator Frequency

OSC	Frequency (MHz)
Open	25
VCC	50

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Absolute Maximum Ratings[1]

Supply Voltage (V_{CC}) ..... –0.5V to +4.0V
CML Input Voltage (V_{IN}) ..... V_{CC}–1.2V to V_{CC}+0.5V
TTL Control Input Voltage (V_I) ..... 0V to V_{CC}+0.3V
Lead Temperature (soldering, 20sec.) ..... +260°C
Storage Temperature (T_s) ..... –65°C to +150°C

Operating Ratings[2]

Supply Voltage (V_{CC}) ..... +3.0V to +3.6V
Ambient Temperature (T_A) ..... –40°C to +85°C
Package Thermal Resistance[3]
QFN
(θ_{JA}) Still-air ..... 75°C/W
(ψ_{JB}) ..... 30°C/W

DC Electrical Characteristics

T_A = –40°C to +85°C and V_{CC} = +3.0V to +3.6V. Unless otherwise noted, typical values are V_{CC} = +3.3V, T_A = 25°C, I_{MOD} = 25mA, I_{BIAS} = 20mA.

Symbol	Parameter	Condition	Min	Typ	Max	Units
I_{CC}	Power Supply Current	Modulation and Bias currents excluded		55	95[4]	mA
V_{MOD_MIN}	Minimum Voltage Required at the Driver Output, MOD+ and MOD-, for Proper Operation		0.6			V
V_{BIAS_MIN}	Minimum Voltage Required at the Driver Output, BIAS+ and BIAS-, for Proper Operation		0.8			V
I_{BIAS}	Bias-ON Current	Voltage at Bias pin ≥ 0.8V	1		70	mA
I_{BIAS_OFF}	Bias-OFF Current	Current at BIAS pin when /EN is high or BEN is low			150	µA
R_{IN}	Input Resistance at DIN+ and DIN-	Single ended	42.5	50	57.5	Ω
$V_{DIFF-IN}$ (DIN)	Differential Input Voltage Swing		100		2400	mV_{PP}
V_{IL} (/EN)	/EN Input Low				0.8	V
V_{IH} (/EN)	/EN Input High		2			V
V_{OL}	/APCFAULT Output Low	I_{OL} = 2mA			0.5	V
I_{OH}	/APCFAULT Output Leakage	V_{OH} = V_{CC}			100	µA
BEN+, BEN-	Burst Mode Enable Signal	Single Ended		0.8		V
V_{IH} (BEN)	High Voltage	BEN+, BEN-			V_{CC} + 0.3	V
V_{IL} (BEN)	Low Voltage	BEN+, BEN-	-0.3			V
V_{IN} (BEN)	Input Voltage Swing	BEN+, BEN-	100			mV
$V_{DIFF-IN}$ (BEN)	Differential Input Voltage Swing	BEN+, BEN-	200			mV_{PP}
V_{PWRMON}	Maximum Voltage at PWRMON Pin		1.25			V
I_{MD}	Current Range at MD Pin		50		1500	µA

Notes:

1. Permanent device damage may occur if absolute maximum ratings are exceeded. This is a stress rating only and functional operation is not implied at conditions other than those detailed in the operational sections of this data sheet. Exposure to absolute maximum ratings conditions for extended periods may affect device reliability.
2. The data sheet limits are not guaranteed if the device is operated beyond the operating ratings.
3. Package Thermal Resistance assumes exposed pad is soldered (or equivalent) to the devices most negative potential on the PCB. ψ_{JB} uses a 4-layer and θ_{JA} in still air unless otherwise stated.
4. I_{CC} = 95mA for worst-case conditions with I_{MOD} = 85mA, I_{BIAS} = 70mA, T_A = +85°C, V_{CC} = 3.6.

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AC Electrical Characteristics

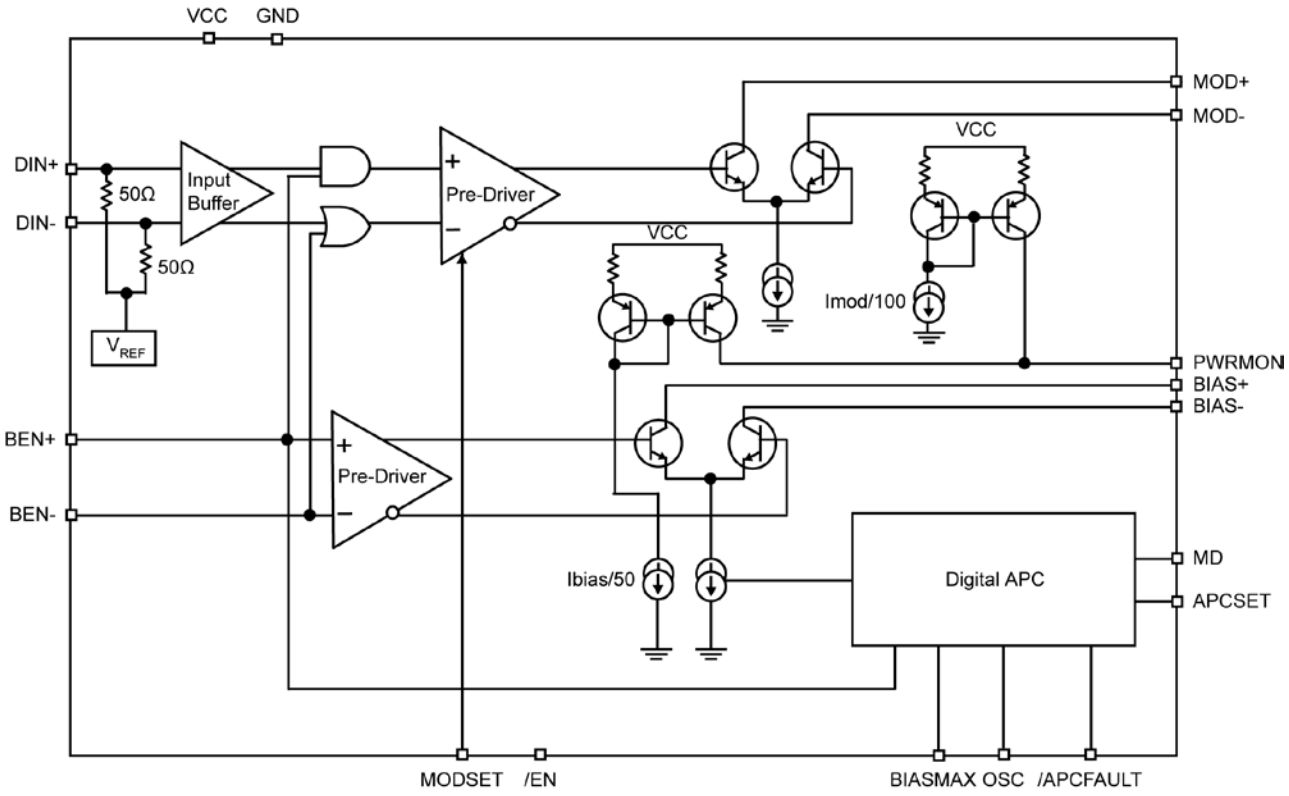
T_A = –40°C to +85°C and V_{CC} = +3.0V to +3.6V. Unless otherwise noted, typical values are V_{CC} = +3.3V, T_A = 25°C, I_{MOD} = 25mA, I_{BIAS} = 20mA.

Symbol	Parameter	Condition	Min	Typ	Max	Units
	Data Rate	NRZ	0.155		2.5	Gbps
I_{MOD}	Modulation Current[5]	AC-coupled	10		85	mA
		DC-coupled, Voltage at MOD Pin ≥0.6V	10		70[6]	mA
I_{MOD_OFF}	Modulation OFF Current	Current at MOD+ when /EN is High or BEN is High			150	µA
		Current at MOD- when /EN is High or BEN is Low			150	µA
t_r	Output Current Rise Time	20% to 80%, I_{MOD} = 60mA		60	85	ps
t_f	Output Current Fall Time	20% to 80%, I_{MOD} = 60mA		60	85	ps
Jitter	Total Jitter[7]	155Mbps			30	ps_{PP}
		622Mbps			30	
		1.25Gbps			30	
		2.5Gbps			30	
t_{INIT}	APC Loop Initialization Time	Power up with /En Low and BEN High			12	µs
		/EN Changes from High to Low with Power ON and BEN High			10	µs
		BEN Changes from Low to High with Power ON and /EN Low			2.5	ns
	Burst Enable Delay[8, 9]				2.5	ns
	Burst Disable Delay[8, 10]				2	ns
	Burst ON-Time	155Mbps	1.9			µs
		622Mbps	720			ns
		1.25Gbps	576			ns
		2.5Gbps	576			ns
	Burst OFF-Time	155Mbps	1.9			µs
		622Mbps	720			ns
		1.25Gbps	576			ns
		2.5Gbps	576			ns

Notes:

5. Load = 15Ω.
6. Assuming V_{CC} = 3.0V, Laser bandgap voltage = 1V, laser package inductance = 1nH, laser equivalent series resistor = 5 Ω, and damping resistor = 10Ω.
7. Total jitter is measured using 2^7 – 1 PRBS pattern.
8. Measured with a laser equivalent resistive load.
9. Burst Enable Delay is measured as the time between the instant when the BEN+ signal going from low to high reaches 50% of its amplitude and the instant at which the modulation current or the bias current (whichever takes longer) reaches 90% of its final value.
10. Burst Disable Delay is measured as the time between the instant when the BEN+ signal going from high to low reaches 50% of its amplitude and the instant at which the modulation current or the bias current (whichever takes longer) goes below 10% of its final value.

Functional Diagram



Detailed Functional Description

The SY88216L burst mode laser driver is comprised from a fast modulator, a fast bias circuit, and a digital APC loop that allows for fast laser turn-ON time. The modulator is comparable to a fast continuous mode modulator that turns ON in the nanosecond range. The bias circuit has a differential pair at the output to allow for fast turn-ON time. Both modulator and bias differential pairs can be enabled for burst operation by applying a high level signal at BEN+ pin and a low level signal at BEN- pin.

The driver features a power monitoring function.

BIAS and Modulation Setting

Bias and modulation currents are set by installing resistors from APCSET (pin24)-to-ground and from MODSET (pin23)-to-ground respectively or by applying a negative current at those pins. I_{BIAS} variation versus R_{APCSET} resistor, I_{BIAS} variation versus $R_{BIASMAX}$ resistor, and I_{MOD} variation versus R_{MODSET} resistor are shown on Page 8.

BIASMAX

A resistor between the BIASMAX pin and ground sets the maximum bias the driver can sink. At normal operation, the bias current tracks the laser optical power through the laser monitoring photodiode and the APC loop to compensate for any power deviation from the nominal value set at the start of operation using APCSET. If any failure occurs (laser or photodiode degradation, open feedback circuit etc.) the APC loop keeps increasing the bias current in an effort to compensate for the low power indication, the bias current will then stop increasing when it reaches BIASMAX value and continue to operate at that maximum value and APCFAULT asserted.

BIASMAX also controls the bias current when the circuit is operating in the open loop mode.

APC Loop Function

At start up, with the driver enabled and burst mode enabled, the laser turns ON within a few microseconds and its back facet monitoring photodiode starts to generate a photocurrent proportional to the optical power. The photocurrent is fed back to the MD pin on the driver where it's converted to a voltage. The conversion voltage is compared to APCSET on the driver. At equilibrium, the feedback voltage equals the APCSET voltage and the laser optical power reaches its nominal value. If the laser power deviates from its nominal value, the APC loop brings it back to its nominal setting. After everything is settled to its nominal value and the BEN changes from high to low to disable the burst mode, the instantaneous bias current value is latched until BEN switches from low to high again. Then the bias and modulation output stages turn ON and the bias stays equal to the stored value until the feedback from the monitoring photodiode reaches the APCSET value and the APC closed loop starts to regulate the laser power.

APC Loop Failure

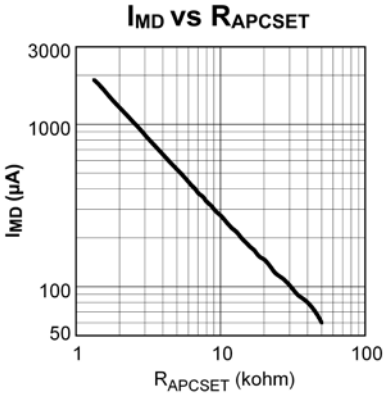
The APCFAULT is asserted Low if the bias current reaches BIASMAX or if the APC loop counter reaches its minimum or its maximum counts.

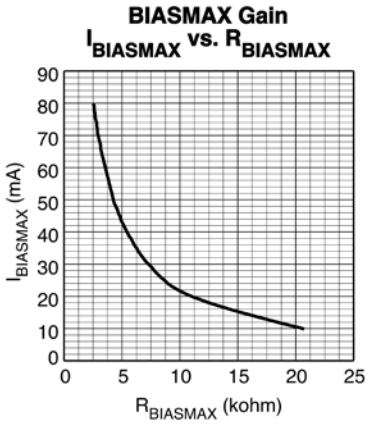
Interfacing the Driver with the Laser Diode

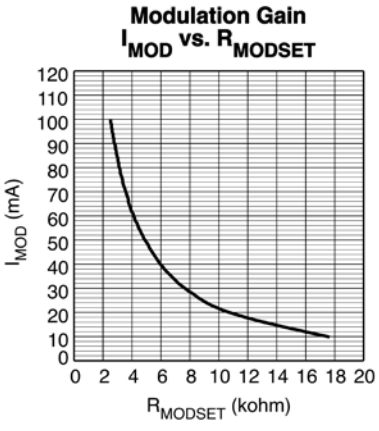
As shown on the "Typical Application" drawing, MOD+ pin is connected to the laser cathode through a 10Ω resistor and MOD- pin is connected to VCC with a 15Ω resistor equivalent to 10Ω (damping resistor) in series with the laser (equivalent resistor of 5Ω). The laser can be driven differentially by connecting MOD- to the anode of the laser through 15Ω (15Ω pull-up removed) and isolating the anode of the laser from VCC with an inductor.

To meet the stringent laser turn-ON time, per BPON/GPON/EPON spec, the bias (BIAS+ pin) must be connected to the cathode of the laser through a resistor not an inductor as in continuous mode. BIAS- pin is pulled-up to VCC.

Typical Characteristics







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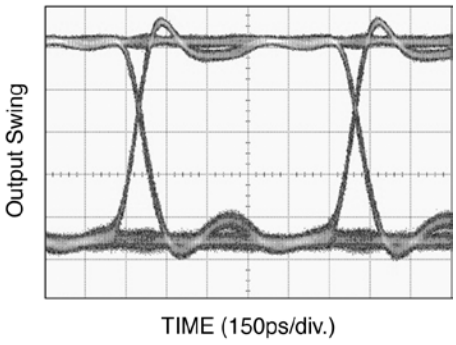
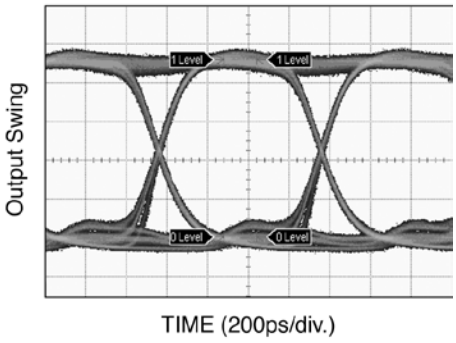
Functional Characteristics

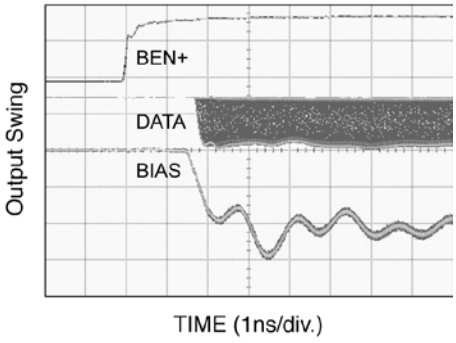
Electrical Eye Diagram @1.25Gbps



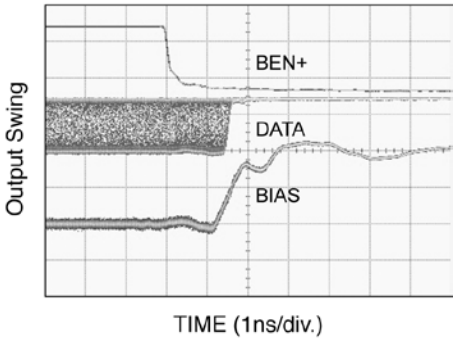
Optical Eye Diagram @1.25Gbps with 2.3G Filter



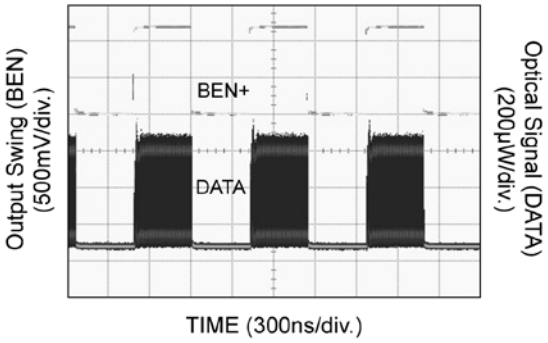
Modulation and Bias Turn-On



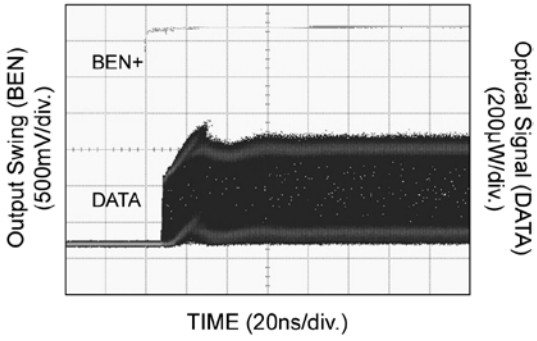
Modulation and Bias Turn-Off



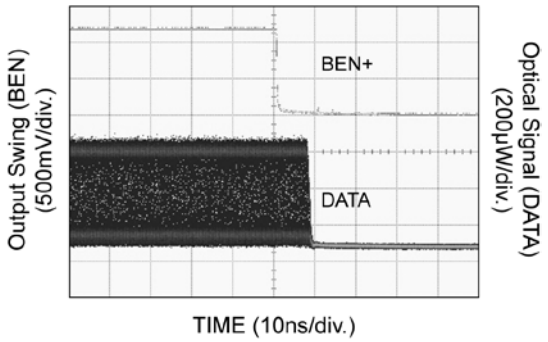
Burst Mode Operation with a Laser



Laser Turn-On



Laser Turn-Off



Input and Output Stages

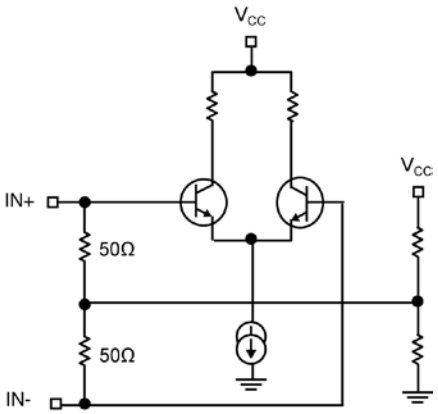


Figure 1a. Simplified Input Stage

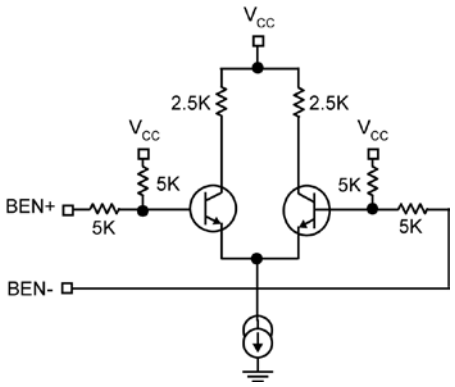


Figure 1b. Simplified BEN Input Stage

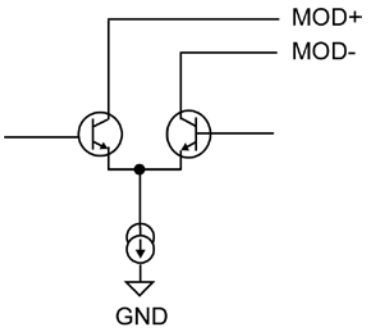


Figure 1c. Simplified Output Stage

Interfacing DIN and BEN Inputs to Different Logic Drivers

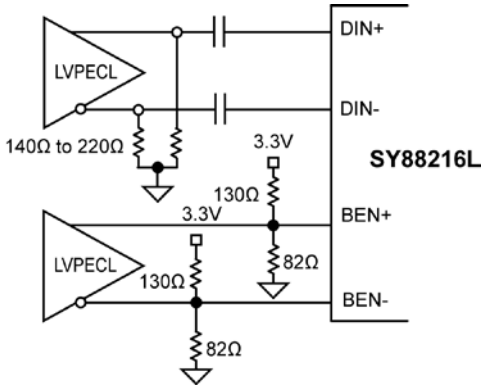


Figure 2a. Driving DIN and BEN with PECL Outputs

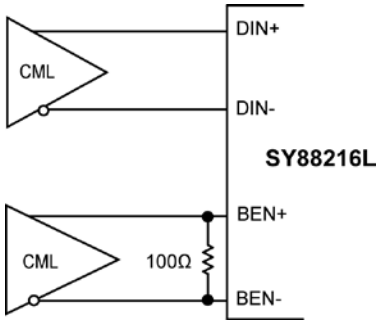


Figure 2b. Driving DIN and BEN with CML Outputs

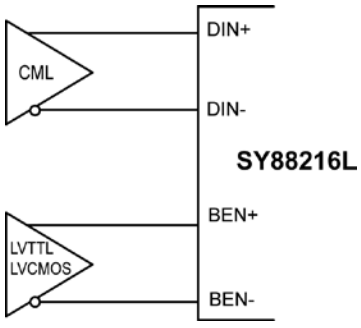


Figure 2c. Driving BEN with LVTTL/LCMOS Outputs

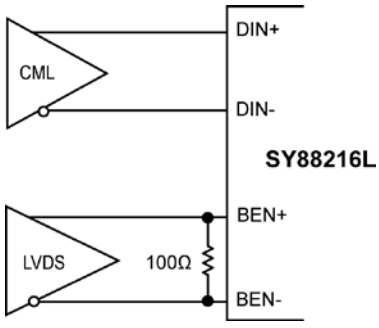


Figure 2d. Driving BEN with LVDS Outputs

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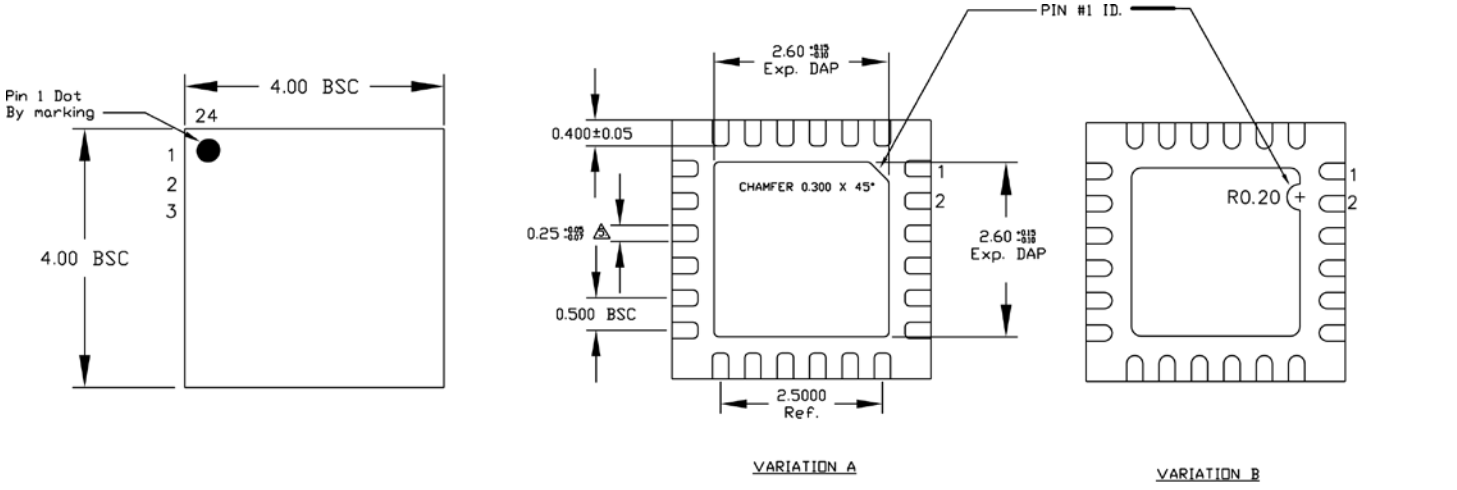
Package Information



NOTE:
1. ALL DIMENSIONS ARE IN MILLIMETERS.
2. MAX. PACKAGE WARPAGE IS 0.05 mm.
3. MAXIMUM ALLOWABE BURRS IS 0.076 mm IN ALL DIRECTIONS.
4. PIN #1 ID ON TOP WILL BE LASER/INK MARKED.
5. DIMENSION APPLIES TO METALIZED TERMINAL AND IS MEASURED BETWEEN 0.20 AND 0.25 mm FROM TERMINAL TIP.
6. APPLIED ONLY FOR TERMINALS.
7. APPLIED FOR EXPOSED PAD AND TERMINALS.

24-Pin (3mm x 3mm) QFN

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