300MHz Low Distortion, Low Noise Differential Amplifier/ ADC Driver (A_V = 20dB)

FEATURES

- 300 MHz –3dB Bandwidth
- Fixed Gain of 20dB
- Low Distortion:
  51dBm OIP3, –81dBc HD3 (20MHz, $2V_{P-P}$)
- Low Noise:
  12.4dB NF, e_n = 1.9nV/$\sqrt{Hz}$ (20MHz)
- Differential Inputs and Outputs
- Additional Filtered Outputs
- Adjustable Output Common Mode Voltage
- DC- or AC-Coupled Operation
- Minimal Support Circuitry Required
- Small 0.75mm Profile 16-Lead 3mm × 3mm QFN Package

APPLICATIONS

- Differential ADC Driver for:
  Imaging
  Communications
- Differential Driver/Receiver
- Single Ended to Differential Conversion
- Differential to Single Ended Conversion
- Level Shifting
- IF Sampling Receivers
- SAW Filter Interfacing/Buffering

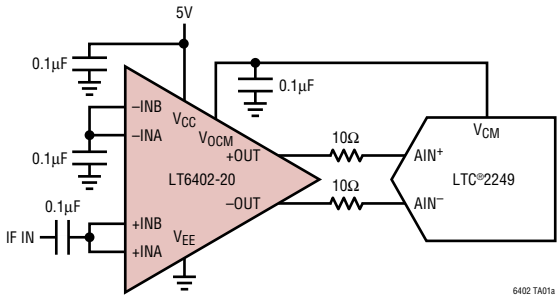
DESCRIPTION

The LT®6402-20 is a low distortion, low noise differential amplifier/ADC driver for use in applications from DC to 300MHz. The LT6402-20 has been designed for ease of use, with minimal support circuitry required. Exceptionally low input-referred noise and low distortion (with either single-ended or differential inputs) make the LT6402-20 an excellent solution for driving high speed 12-bit and 14-bit ADCs. In addition to the normal unfiltered outputs (+OUT and –OUT), the LT6402-20 has a built-in 75MHz differential low pass filter and an additional pair of filtered outputs (+OUTFILTERED, –OUTFILTERED) to reduce external filtering components when driving high speed ADCs. The output common mode voltage is easily set via the V_{OCM} pin, eliminating an output transformer or AC-coupling capacitors in many applications.

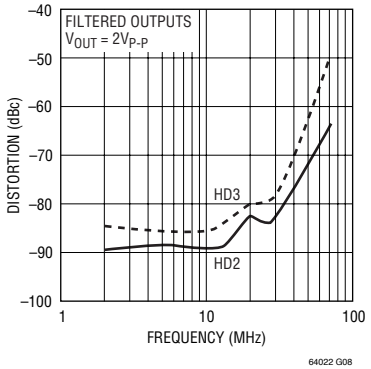
The LT6402-20 is designed to meet the demanding requirements of communications transceiver applications. It can be used as a differential ADC driver, a general-purpose differential gain block, or in other applications requiring differential drive. The LT6402-20 can be used in data acquisition systems required to function at frequencies down to DC.

The LT6402-20 operates on a 5V supply and consumes 30mA. It comes in a compact 16-lead 3mm × 3mm QFN package and operates over a –40°C to 85°C temperature range.

TYPICAL APPLICATION



Distortion vs Frequency, Differential Input, No R_{LOAD}

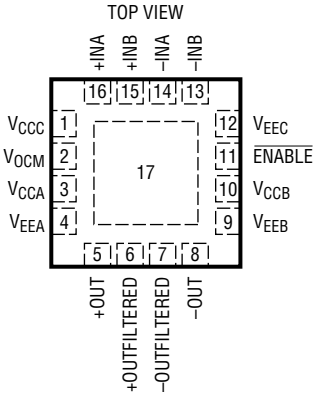


ABSOLUTE MAXIMUM RATINGS

(Note 1)

Total Supply Voltage ($V_{CCA}/V_{CCB}/V_{CCC}$ to $V_{EEA}/V_{EEB}/V_{EEC}$) 5.5V
Input Current (+INA, –INA, +INB, –INB, V_{OCM}, $\overline{ENABLE}$).....±10mA
Output Current (Continuous)
+OUT, –OUT .....±100mA
+OUTFILTERED, –OUTFILTERED.....±30mA
Output Short Circuit Duration (Note 2) ..... Indefinite
Operating Temperature Range (Note 3) ... –40°C to 85°C
Specified Temperature Range (Note 4) .... –40°C to 85°C
Storage Temperature Range..... –65°C to 125°C
Junction Temperature ..... 125°C
Lead Temperature Range (Soldering 10 sec) ..... 300°C

PACKAGE/ORDER INFORMATION



UD PACKAGE
16-LEAD (3mm × 3mm) PLASTIC QFN
T_{JMAX} = 125°C, θ_{JA} = 68°C/W, θ_{JC} = 4.2°C/W
EXPOSED PAD IS V_{EE} (PIN 17)
MUST BE SOLDERED TO THE PCB

ORDER PART NUMBER	UD PART MARKING*
LT6402CUD-20	LCBC
LT6402IUD-20	LCBC

Order Options Tape and Reel: Add #TR
Lead Free: Add #PBF Lead Free Tape and Reel: Add #TRPBF
Lead Free Part Marking: http://www.linear.com/leadfree/

Consult LTC Marketing for parts specified with wider operating temperature ranges.
*The temperature grade is identified by a label on the shipping container.

DC ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C. V_{CCA} = V_{CCB} = V_{CCC} = 5V, V_{EEA} = V_{EEB} = V_{EEC} = 0V, $\overline{ENABLE}$ = 0.8V, +INA shorted to +INB (+IN), –INA shorted to –INB (–IN), V_{OCM} = 2.2V, Input common mode voltage = 2.2V, no R_{LOAD} unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
Input/Output Characteristics (+INA, +INB, –INA, –INB, +OUT, –OUT, +OUTFILTERED, –OUTFILTERED)							
GDIFF	Gain	Differential (+OUT, –OUT), V_{IN} = ±160mV Differential	●	18.9	20	20.9	dB
$V_{SWINGMIN}$		Single-Ended +OUT, –OUT, +OUTFILTERED, –OUTFILTERED, V_{IN} = ±600mV Differential	 ●		0.25	0.35 0.5	V V
$V_{SWINGMAX}$		Single-Ended +OUT, –OUT, +OUTFILTERED, –OUTFILTERED, V_{IN} = ±600mV Differential	 ●	3.4 3.3	3.6		V V
$V_{SWINGDIFF}$	Output Voltage Swing	Differential (+OUT, –OUT), V_{IN} = ±600mV Differential	 ●	6.1 5.6	7		V_{P-P} V_{P-P}
I_{OUT}	Output Current Drive		●	±30	±35		mA
V_{OS}	Input Offset Voltage		 ●	–6.5 –10	1	6.5 10	mV mV
TCV_{OS}	Input Offset Voltage Drift	T_{MIN} to T_{MAX}	●		2.5		µV/°C

DC ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C. V_{CCA} = V_{CCB} = V_{CCC} = 5V, V_{EEA} = V_{EEB} = V_{EEC} = 0V, $\overline{ENABLE}$ = 0.8V, +INA shorted to +INB (+IN), –INA shorted to –INB (–IN), V_{OCM} = 2.2V, Input common mode voltage = 2.2V, no R_{LOAD} unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
I_{VRMIN}	Input Voltage Range, MIN	Single-Ended	●			0.9	V
I_{VRMAX}	Input Voltage Range, MAX	Single-Ended	●	3.9			V
R_{INDIFF}	Input Resistance		●	77	100	122	Ω
C_{INDIFF}	Input Capacitance				1		pF
CMRR	Common Mode Rejection Ratio	Input Common Mode 0.9V to 3.9V	●	45	70		dB
$R_{OUTDIFF}$	Output Resistance				0.3		Ω
$C_{OUTDIFF}$	Output Capacitance				0.8		pF
Common Mode Voltage Control (V_{OCM} Pin)							
GCM	Common Mode Gain	Differential (+OUT, –OUT), V_{OCM} = 1.2V to 3.6V Differential (+OUT, –OUT), V_{OCM} = 1.4V to 3.4V	 ●	0.9 0.9	1	1.1 1.1	V/V V/V
V_{OCMMIN}	Output Common Mode Voltage Adjustment Range, MIN		 ●			1.2 1.4	V V
V_{OCMMAX}	Output Common Mode Voltage Adjustment Range, MAX	Single-Ended	 ●	3.6 3.4			V V
V_{OSCM}	Output Common Mode Offset Voltage	Measured from V_{OCM} to Average of +OUT and –OUT		–30	4	30	mV
I_{BIASCM}	V_{OCM} Input Bias Current		●		5	15	µA
R_{INCM}	V_{OCM} Input Resistance		●	0.8	3		MΩ
C_{INCM}	V_{OCM} Input Capacitance				1		pF
$\overline{ENABLE}$ Pin							
V_{IL}	$\overline{ENABLE}$ Input Low Voltage		●			0.8	V
V_{IH}	$\overline{ENABLE}$ Input High Voltage		●	2			V
I_{IL}	$\overline{ENABLE}$ Input Low Current	$\overline{ENABLE}$ = 0.8V	●			0.5	µA
I_{IH}	$\overline{ENABLE}$ Input High Current	$\overline{ENABLE}$ = 2V	●		1	3	µA
Power Supply							
V_S	Operating Range		●	4	5	5.5	V
I_S	Supply Current	$\overline{ENABLE}$ = 0.8V	●	24	30	37	mA
$I_{SDISABLED}$	Supply Current (Disabled)	$\overline{ENABLE}$ = 2V	●		250	500	µA
PSRR	Power Supply Rejection Ratio	4V to 5.5V	●	55	90		dB

AC ELECTRICAL CHARACTERISTICS

T_A = 25°C, V_{CCA} = V_{CCB} = V_{CCC} = 5V, V_{EEA} = V_{EEB} = V_{EEC} = 0V, $\overline{ENABLE}$ = 0.8V, +INA shorted to +INB (+IN), –INA shorted to –INB (–IN), V_{OCM} = 2.2V, Input common mode voltage = 2.2V, no R_{LOAD} unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Input/Output Characteristics						
–3dBBW	–3dB Bandwidth	20mV$_{P-P}$ Differential (+OUT, –OUT)	200	300		MHz
0.1dBBW	Bandwidth for 0.1dB Flatness	20mV$_{P-P}$ Differential (+OUT, –OUT)		30		MHz
0.5dBBW	Bandwidth for 0.5dB Flatness	20mV$_{P-P}$ Differential (+OUT, –OUT)		80		MHz
SR	Slew Rate	3.2V$_{P-P}$ Differential (+OUT, –OUT)		400		V/µs
$t_{s1\%}$	1% Settling	1% Settling for a 1V$_{P-P}$ Differential Step (+OUT, –OUT)		8		ns
t_{ON}	Turn-On Time			100		ns
t_{OFF}	Turn-Off Time			1		µs
Common Mode Voltage Control (V_{OCM} Pin)						
–3dBBW$_{CM}$	Common Mode Small-Signal –3dB Bandwidth	0.1V$_{P-P}$ at V_{OCM}, Measured Single-Ended at +OUT and –OUT		200		MHz
SR$_{CM}$	Common Mode Slew Rate	1.3V to 3.4V Step at V_{OCM}		250		V/µs
Noise/Harmonic Performance Input/Output Characteristics						
10MHz Signal						
	Second/Third Harmonic Distortion	2V$_{P-P}$ Differential (+OUTFILTERED, –OUTFILTERED)		–85		dBc
		2V$_{P-P}$ Differential (+OUT, –OUT)		–85		dBc
	Third-Order IMD	2V$_{P-P}$ Differential Composite (+OUTFILTERED, –OUTFILTERED), f1 = 9.5MHz, f2 = 10.5MHz		–93		dBc
OIP3$_{10M}$	Output Third-Order Intercept	Differential (+OUTFILTERED, –OUTFILTERED), f1 = 9.5MHz, f2 = 10.5MHz (Note 5)		49.5		dBm
NF	Noise Figure	Measured Using DC954A Demo Board		12.3		dB
e_{n10M}	Input Referred Noise Voltage Density			1.85		nV/√Hz
	1dB Compression Point	R_L = 100Ω (Note 5)		19.5		dBm
20MHz Signal						
	Second/Third Harmonic Distortion	2V$_{P-P}$ Differential (+OUTFILTERED, –OUTFILTERED)		–81		dBc
		2V$_{P-P}$ Differential (+OUT, –OUT)		–81		dBc
	Third-Order IMD	2V$_{P-P}$ Differential Composite (+OUTFILTERED, –OUTFILTERED), f1 = 19.5MHz, f2 = 20.5MHz		–96		dBc
		2V$_{P-P}$ Differential Composite (+OUT, –OUT), R_L = 400Ω, f1 = 19.5MHz, f2 = 20.5MHz		–91		dBc
OIP3$_{20M}$	Output Third-Order Intercept	Differential (+OUTFILTERED, –OUTFILTERED), f1 = 19.5MHz, f2 = 20.5MHz (Note 5)		51		dBm
NF	Noise Figure	Measured Using DC954A Demo Board		12.4		dB
e_{n20M}	Input Referred Noise Voltage Density			1.9		nV/√Hz
	1dB Compression Point	R_L = 100Ω (Note 5)		18		dBm

AC ELECTRICAL CHARACTERISTICS

T_A = 25°C, V_{CCA} = V_{CCB} = V_{CCC} = 5V, V_{EEA} = V_{EEB} = V_{EEC} = 0V, $\overline{ENABLE}$ = 0.8V, +INA shorted to +INB (+IN), –INA shorted to –INB (–IN), V_{OCM} = 2.2V, Input common mode voltage = 2.2V, no R_{LOAD} unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
25MHz Signal						
	Second/Third Harmonic Distortion	$2V_{P-P}$ Differential (+OUTFILTERED, –OUTFILTERED)		–80		dBc
		$2V_{P-P}$ Differential (+OUT, –OUT)		–80		dBc
	Third-Order IMD	$2V_{P-P}$ Differential Composite (+OUTFILTERED, –OUTFILTERED), f1 = 24.5MHz, f2 = 25.5MHz		–86		dBc
		$2V_{P-P}$ Differential Composite (+OUT, –OUT), R_L = 400Ω, f1 = 24.5MHz, f2 = 25.5MHz		–84		dBc
$OIP3_{25M}$	Output Third-Order Intercept	Differential (+OUTFILTERED, –OUTFILTERED), f1 = 24.5MHz, f2 = 25.5MHz (Note 5)		46		dBm
NF	Noise Figure	Measured Using DC954A Demo Board		12.5		dB
e_{n25M}	Input Referred Noise Voltage Density			1.9		nV/√Hz
	1dB Compression Point	R_L = 100Ω (Note 5)		16.6		dBm

Note 1: Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. Exposure to any Absolute Maximum Rating condition for extended periods may affect device reliability and lifetime.

Note 2: As long as output current and junction temperature are kept below the Absolute Maximum Ratings, no damage to the part will occur.

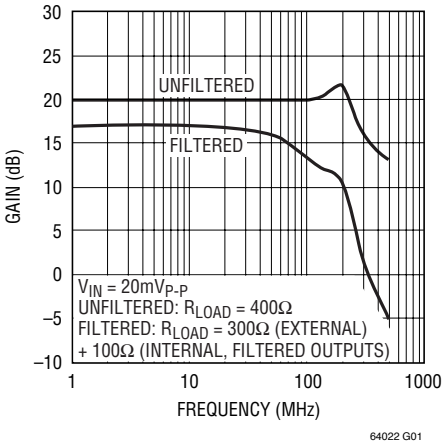
Note 3: The LT6402 is guaranteed functional over the operating temperature range of –40°C to 85°C.

Note 4: The LT6402C is guaranteed to meet specified performance from 0°C to 70°C. It is designed, characterized and expected to meet specified performance from –40°C and 85°C but is not tested or QA sampled at these temperatures. The LT6402I is guaranteed to meet specified performance from –40°C to 85°C.

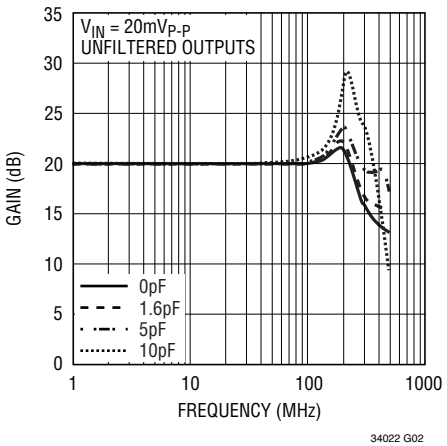
Note 5: Since the LT6402-20 is a feedback amplifier with low output impedance, a resistive load is not required when driving an ADC. Therefore, typical output power is very small. In order to compare the LT6402-20 with typical g_m amplifiers that require 50Ω output loading, the LT6402-20 output voltage swing driving an ADC is converted to OIP3 and P1dB as if it were driving a 50Ω load.

TYPICAL PERFORMANCE CHARACTERISTICS

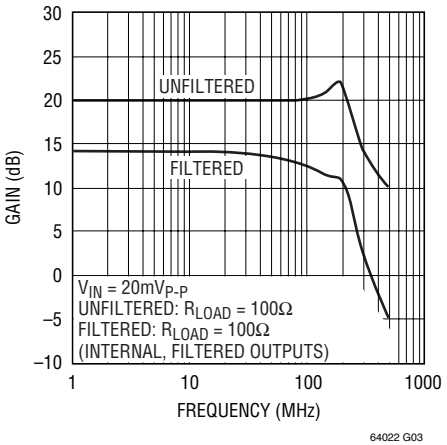
Frequency Response
R_{LOAD} = 400Ω



Frequency Response vs
C_{LOAD}, R_{LOAD} = 400Ω

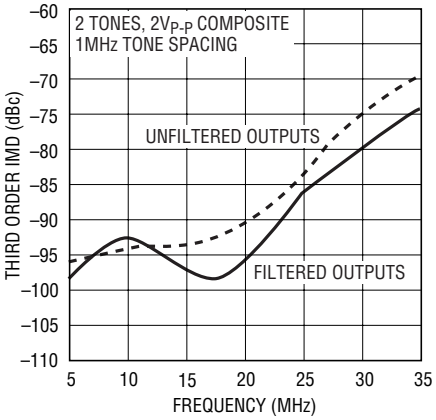


Frequency Response
R_{LOAD} = 100Ω

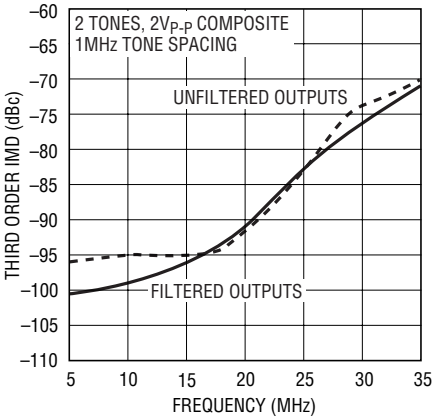


TYPICAL PERFORMANCE CHARACTERISTICS

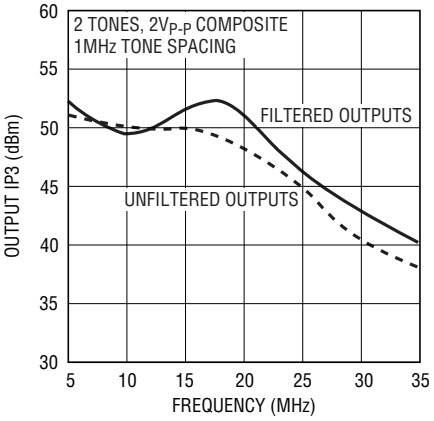
Third Order Intermodulation Distortion vs Frequency Differential Input, No R_{LOAD}



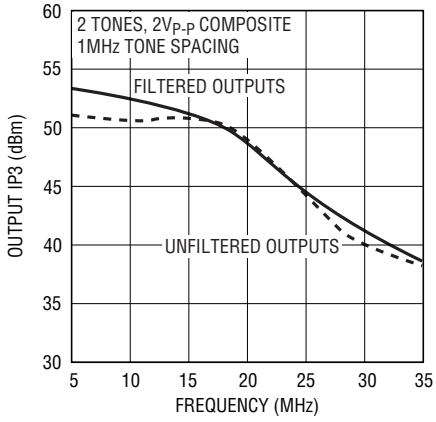
Third Order Intermodulation Distortion vs Frequency Differential Input, R_{LOAD} = 400Ω



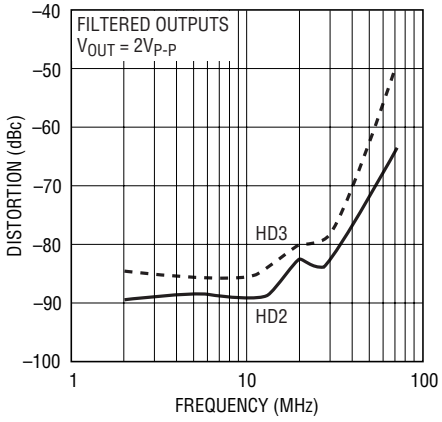
Output Third Order Intercept vs Frequency, Differential Input, No R_{LOAD}



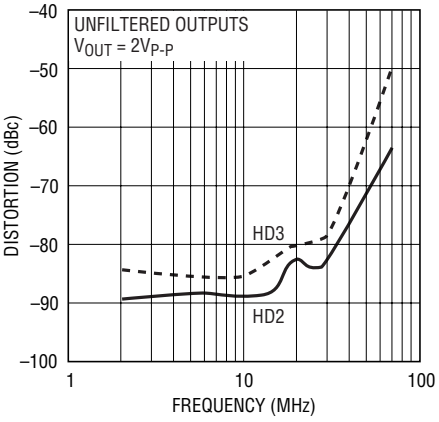
Output Third Order Intercept vs Frequency, Differential Input, R_{LOAD} = 400Ω



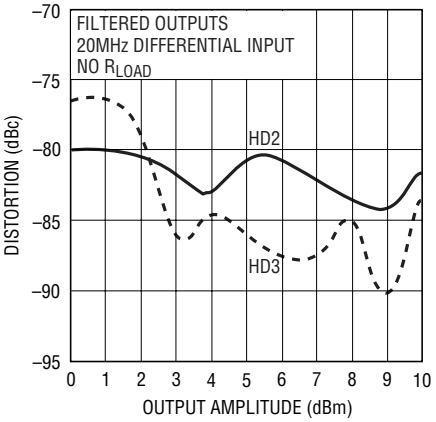
Distortion vs Frequency, Differential Input, No R_{LOAD} (Filtered)



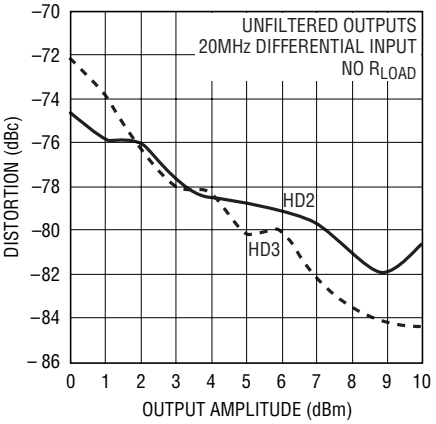
Distortion vs Frequency, Differential Input, No R_{LOAD} (Unfiltered)



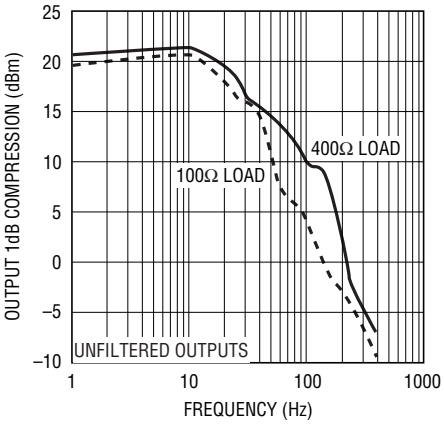
Distortion vs Output Amplitude 20MHz Differential Input, No R_{LOAD} (Filtered)



Distortion vs Output Amplitude 20MHz Differential Input, No R_{LOAD} (Unfiltered)

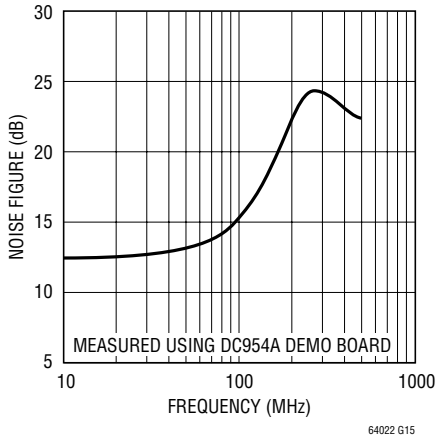


Output 1dB Compression vs Frequency

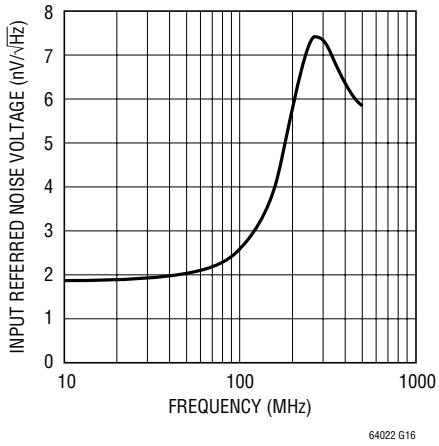


TYPICAL PERFORMANCE CHARACTERISTICS

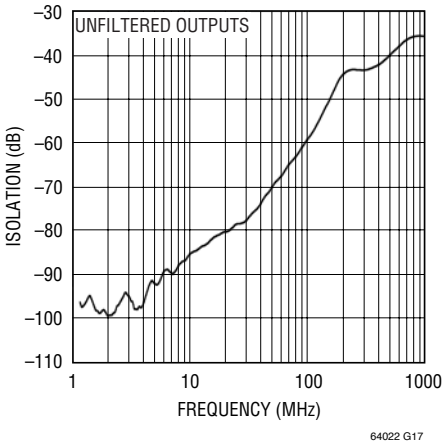
Noise Figure vs Frequency



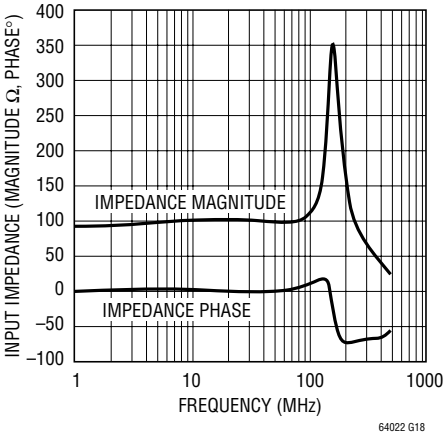
Input Referred Noise Voltage vs Frequency



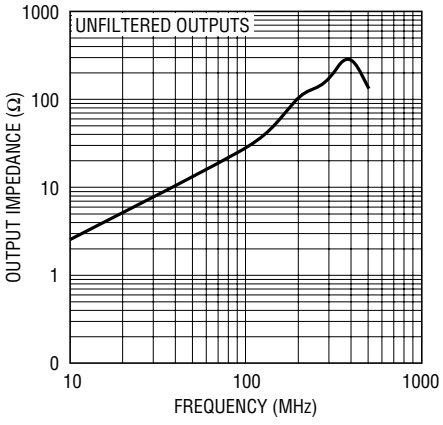
Isolation vs Frequency



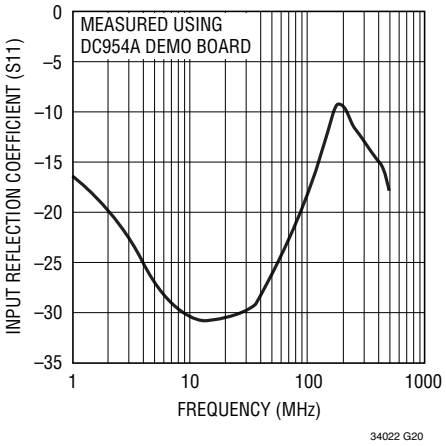
Differential Input Impedance vs Frequency



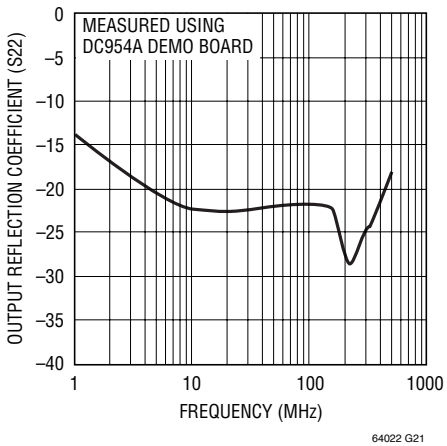
Differential Output Impedance vs Frequency



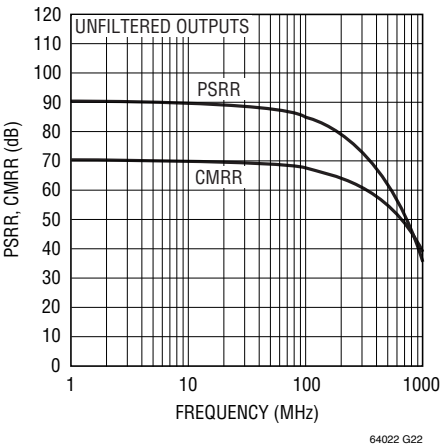
Input Reflection Coefficient vs Frequency



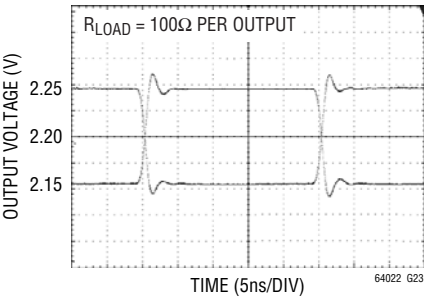
Output Reflection Coefficient vs Frequency



PSRR, CMRR vs Frequency

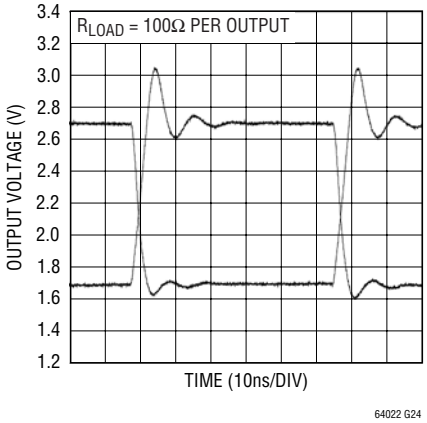


Small-Signal Transient Response

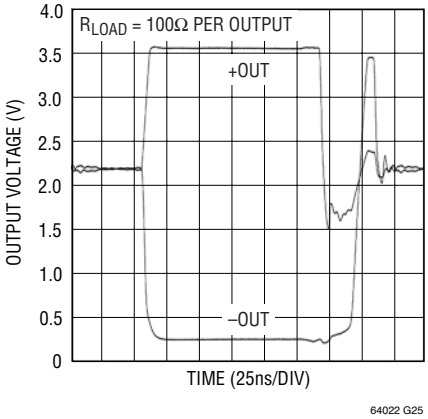


TYPICAL PERFORMANCE CHARACTERISTICS

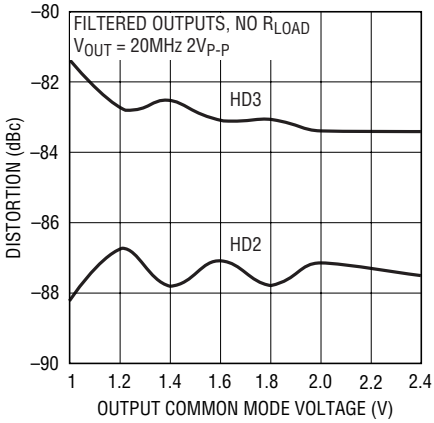
Large-Signal Transient Response



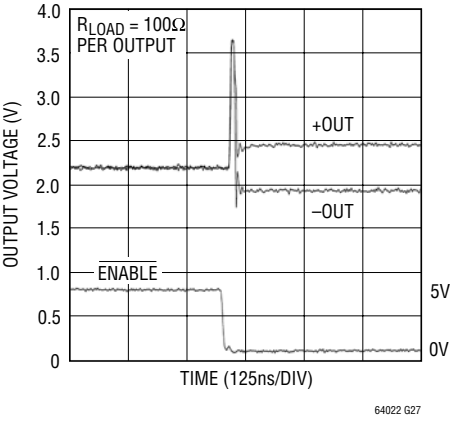
Overdrive Recovery Time



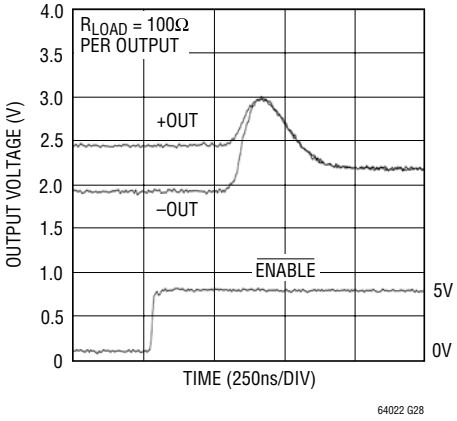
Distortion vs Output Common Mode Voltage LT6402-20 Driving LTC2249 14-Bit ADC



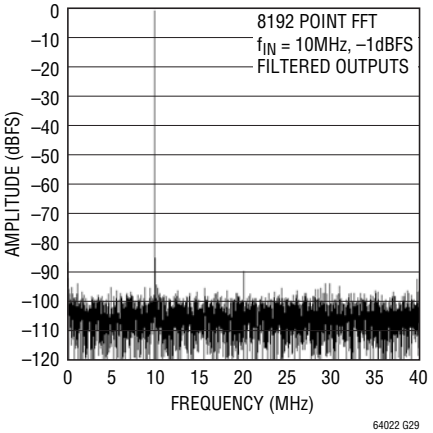
Turn-On Time



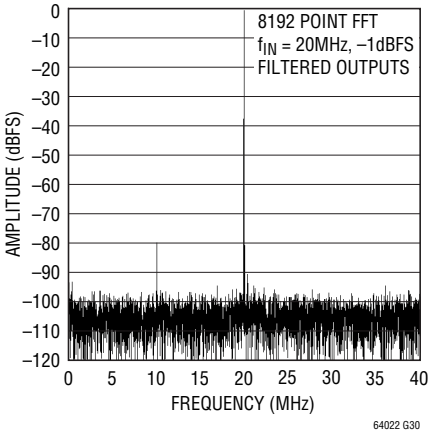
Turn-Off Time



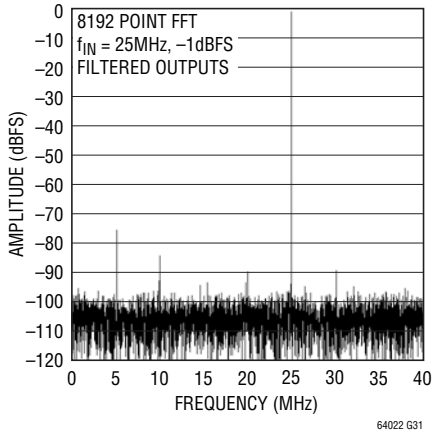
10MHz 8192 Point FFT, LT6402-20 Driving LTC2249 14-Bit ADC



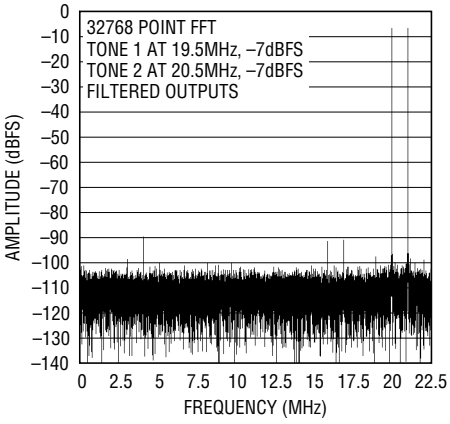
20MHz 8192 Point FFT, LT6402-20 Driving LTC2249 14-Bit ADC



25MHz 8192 Point FFT, LT6402-20 Driving LTC2249 14-Bit ADC



20MHz 2-Tone 32768 Point FFT, LT6402-20 Driving LTC2249 14-Bit ADC



PIN FUNCTIONS

V_{OCM} (Pin 2): This pin sets the output common mode voltage. Without additional biasing, both inputs bias to this voltage as well. This input is high impedance.

V_{CCA}, V_{CCB}, V_{CCC} (Pins 3, 10, 1): Positive Power Supply (Normally Tied to 5V). All three pins must be tied to the same voltage. Bypass each pin with 1000pF and 0.1µF capacitors as close to the package as possible. Split supplies are possible as long as the voltage between V_{CC} and V_{EE} is 5V.

V_{EEA}, V_{EEB}, V_{EEC} (Pins 4, 9, 12): Negative Power Supply (Normally Tied to Ground). All three pins must be tied to the same voltage. Split supplies are possible as long as the voltage between V_{CC} and V_{EE} is 5V. If these pins are not tied to ground, bypass each pin with 1000pF and 0.1µF capacitors as close to the package as possible.

+OUT, –OUT (Pins 5, 8): Outputs (Unfiltered). These pins are high bandwidth, low-impedance outputs. The DC output voltage at these pins is set to the voltage applied at V_{OCM}.

+OUTFILTERED, –OUTFILTERED (Pins 6, 7): Filtered Outputs. These pins add a series 50Ω resistor from the unfiltered outputs and three 14pF capacitors. Each output has 14pF to V_{EE}, plus an additional 14pF between each pin (See the Block Diagram). This filter has a –3dB bandwidth of 75MHz.

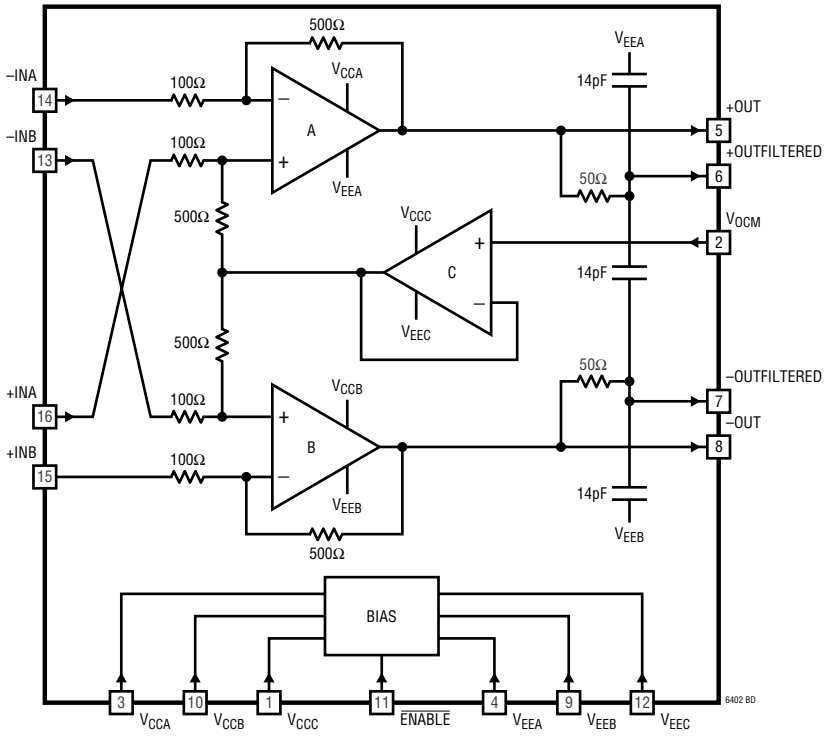
$\overline{\text{ENABLE}}$ (Pin 11): This pin is a TTL logic input referenced to the V_{EEC} pin. If low, the LT6402 is enabled and draws typically 30mA of supply current. If high, the LT6402 is disabled and draws typically 250µA.

+INA, +INB (Pins 15, 16): Positive Inputs. These pins are normally tied together. These inputs may be DC- or AC-coupled. If the inputs are AC-coupled, they will self-bias to the voltage applied to the V_{OCM} pin.

–INA, –INB (Pins 14, 13): Negative Inputs. These pins are normally tied together. These inputs may be DC- or AC-coupled. If the inputs are AC-coupled, they will self-bias to the voltage applied to the V_{OCM} pin.

Exposed Pad (Pin 17): Tie the pad to V_{EEC} (Pin 12). If split supplies are used, DO NOT tie the pad to ground.

BLOCK DIAGRAM



APPLICATIONS INFORMATION

Circuit Description

The LT6402-20 is a low noise, low distortion differential amplifier/ADC driver with:

- –3dB bandwidth
  DC to 300MHz
- Fixed gain independent of R_{LOAD}
  10V/V (20dB)
- Differential input impedance
  100Ω
- Low output impedance
- Built-in, user adjustable output filtering
- Requires minimal support circuitry

Referring to the block diagram, the LT6402-20 uses a closed-loop topology which incorporates 3 internal amplifiers. Two of the amplifiers (A and B) are identical and drive the differential outputs. The third amplifier is used to set the output common mode voltage. Gain and input impedance are set by the 500Ω and 100Ω resistors in the internal feedback network. Output impedance is low, determined by the inherent output impedance of amplifiers A and B, and further reduced by internal feedback.

The LT6402-20 also includes built-in single-pole output filtering. The user has the choice of using the unfiltered outputs, the filtered outputs (75MHz –3dB lowpass), or modifying the filtered outputs to alter frequency response by adding additional components. Many lowpass and bandpass filters are easily implemented with just one or two additional components.

The LT6402-20 has been designed to minimize the need for external support components such as transformers or AC-coupling capacitors. As an ADC driver, the LT6402-20 requires no external components except for power-supply bypass capacitors. This allows DC-coupled operation for applications that have frequency ranges including DC. At the outputs, the common mode voltage is set via the V_{OCM} pin, allowing the LT6402-20 to drive ADCs directly. No output AC-coupling capacitors or transformers are needed. At the inputs, signals can be differential or single-ended with virtually no difference in performance. Furthermore, DC levels at the inputs can be set independently of the output common mode voltage. These input characteristics often eliminate the need for an input transformer and/or AC-coupling capacitors.

Input Impedance and Matching Networks

Calculation of the input impedance of the LT6402-20 is not straightforward from examination of the block diagram because of the internal feedback network. In addition, the input impedance when driven differentially is different than when driven single-ended.

	Differential	Single-Ended
LT6402-20	100Ω	85.9Ω

For single-ended 50Ω applications, a 121Ω shunt matching resistor to ground will result in the proper input termination (Figure 1). For differential inputs there are several termination options. If the input source is 50Ω differential, then the input matching can be accomplished by either a 100Ω shunt resistor across the inputs (Figure 3), or equivalent 49.9Ω shunt resistors on each of the inputs to ground (Figure 2). If additional AC gain is desired, an impedance ratio transformer can also be used to better match impedances.

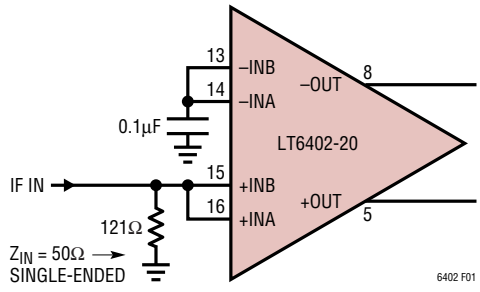


Figure 1. Input Termination for Single-Ended 50Ω Input Impedance

APPLICATIONS INFORMATION

Single-Ended to Differential Operation

The LT6402-20's performance with single-ended inputs is comparable to its performance with differential inputs. This excellent single-ended performance is largely due to the internal topology of the LT6402-20. Referring to the block diagram, if the +INA and +INB pins are driven with a single-ended signal (while –INA and –INB are tied to AC ground), then the +OUT and –OUT pins are driven differentially without any voltage swing needed from amplifier C. Single-ended to differential conversion using more conventional topologies suffers from performance limitations due to the common mode amplifier.

Driving ADCs

The LT6402-20 has been specifically designed to interface directly with high speed Analog to Digital Converters (ADCs). In general, these ADCs have differential inputs, with an input impedance of 1kΩ or higher. In addition, there is generally some form of lowpass or bandpass filtering just prior to the ADC to limit input noise at the ADC, thereby improving system signal to noise ratio. Both the unfiltered and filtered outputs of the LT6402-20 can easily drive the high impedance inputs of these differential ADCs. If the filtered outputs are used, then cutoff frequency and the type of filter can be tailored for the specific application if needed.

Wideband Applications (Using the +OUT and –OUT Pins)

In applications where the full bandwidth of the LT6402-20 is desired, the unfiltered output pins (+OUT and –OUT) should be used. They have a low output impedance; therefore, gain is unaffected by output load. Capacitance in excess of 5pF placed directly on the unfiltered outputs results in additional peaking and reduced performance. When driving an ADC directly, a small series resistance is recommended between the LT6402-20's outputs and the ADC inputs (Figure 4). This resistance helps eliminate any resonances associated with bond wire inductances of either the ADC inputs or the LT6402-20's outputs. A value between 10Ω and 25Ω gives excellent results.

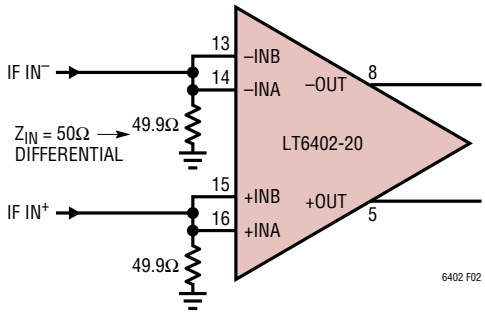


Figure 2. Input Termination for Differential 50Ω Input Impedance

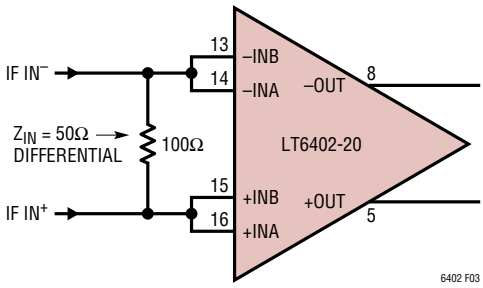


Figure 3. Alternate Input Termination for Differential 50Ω Input Impedance

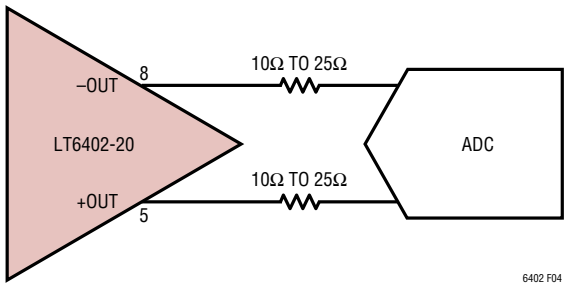


Figure 4. Adding Small Series R at LT6402 Output

APPLICATIONS INFORMATION

Filtered Applications (Using the +OUTFILTERED and –OUTFILTERED Pins)

Filtering at the output of the LT6402-20 is often desired to provide either anti-aliasing or improved signal to noise ratio. To simplify this filtering, the LT6402-20 includes an additional pair of differential outputs (+OUTFILTERED and –OUTFILTERED) which incorporate an internal lowpass filter network with a –3dB bandwidth of 75MHz (Figure 5). These pins each have an output impedance of 50Ω. Internal capacitances are 14pF to V_{EE} on each filtered output, plus an additional 14pF capacitor connected differentially between the two filtered outputs. This resistor/capacitor combination creates filtered outputs that look like a series 50Ω resistor with a 42pF capacitor shunting each filtered output to AC ground, giving a –3dB bandwidth of 75MHz.

The filter cutoff frequency is easily modified with just a few external components. To increase the cutoff frequency, simply add 2 equal value resistors, one between +OUT and +OUTFILTERED and the other between –OUT and –OUTFILTERED (Figure 6). These resistors are in parallel with the internal 50Ω resistor, lowering the overall resistance and increasing filter bandwidth. To double the filter bandwidth, for example, add two external 50Ω resistors to lower the series resistance to 25Ω. The 42pF of capacitance remains unchanged, so filter bandwidth doubles.

To decrease filter bandwidth, add two external capacitors, one from +OUTFILTERED to ground, and the other from –OUTFILTERED to ground. A single differential capacitor connected between +OUTFILTERED and –OUTFILTERED can also be used, but since it is being driven differentially it will appear at each filtered output as a single-ended capacitance of twice the value. To halve the filter bandwidth, for example, two 42pF capacitors could be added (one from each filtered output to ground). Alternatively one 21pF capacitor could be added between the filtered outputs, again halving the filter bandwidth. Combinations of capacitors could be used as well; a three capacitor

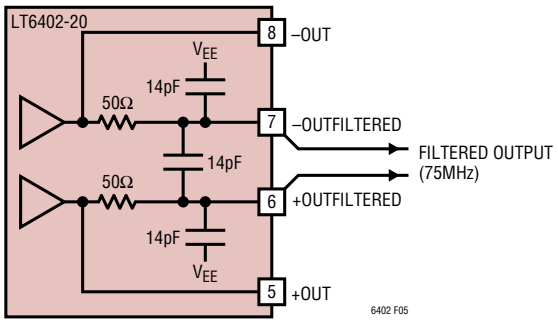


Figure 5. LT6402-20 Internal Filter Topology –3dB BW ≈75MHz

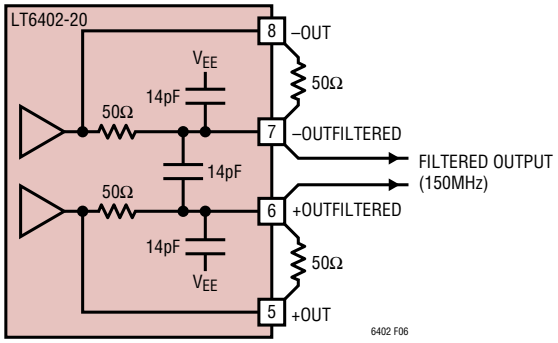


Figure 6. LT6402-20 Internal Filter Topology Modified for 2x Filter Bandwidth (2 External Resistors)

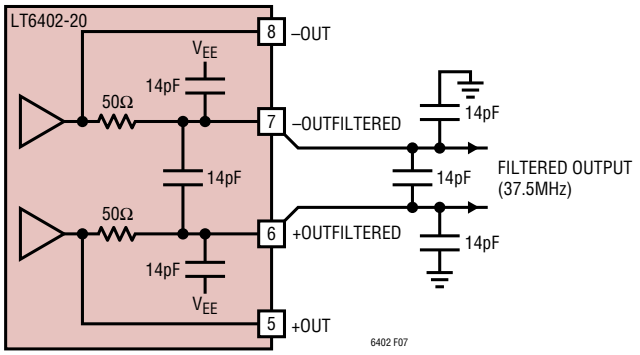


Figure 7. LT6402-20 Internal Filter Topology Modified for 1/2x Filter Bandwidth (3 External Capacitors)

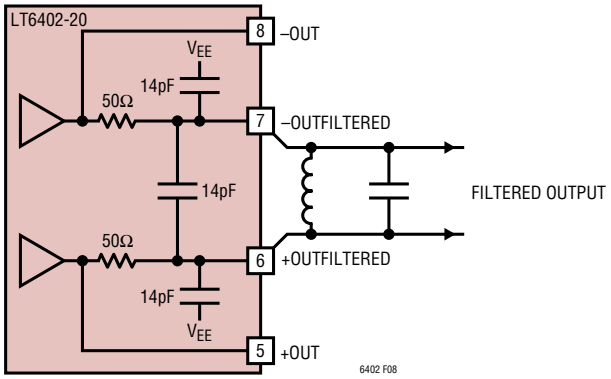


Figure 8. LT6402-20 Output Filter Modified for Bandpass Filtering (1 External Inductor, 1 External Capacitor)

APPLICATIONS INFORMATION

solution of 14pF from each filtered output to ground plus a 14pF capacitor between the filtered outputs would also halve the filter bandwidth (Figure 7).

Bandpass filtering is also easily implemented with just a few external components. An additional 560pF and 62nH, each added differentially between +OUTFILTERED and –OUTFILTERED creates a bandpass filter with a 26MHz center frequency, –3dB points of 23MHz and 30MHz, and 1.6dB of insertion loss (Figure 8).

Output Common Mode Adjustment

The LT6402-20's output common mode voltage is set by the V_{OCM} pin. It is a high-impedance input, capable of setting the output common mode voltage anywhere in a range from 1.1V to 3.6V. Bandwidth of the V_{OCM} pin is typically 200MHz, so for applications where the V_{OCM} pin is tied to a DC bias voltage, a 0.1µF capacitor at this pin is recommended. For best distortion performance, the voltage at the V_{OCM} pin should be between 1.8V and 2.6V.

When interfacing with most ADCs, there is generally a V_{OCM} output pin that is at about half of the supply voltage of the ADC. For 5V ADCs such as the LTC17XX family, this V_{OCM} output pin should be connected directly (with the addition of a 0.1µF capacitor) to the input V_{OCM} pin of the LT6402-20. For 3V ADCs such as the LTC22XX families, the LT6402-20 will function properly using the 1.65V from the ADC's V_{CM} reference pin, but improved Spurious Free Dynamic Range (SFDR) and distortion performance can be achieved by level-shifting the LTC22XX's V_{CM} reference voltage up to at least 1.8V. This can be accomplished as shown in Figure 9 by using a resistor divider between the LTC22XX's V_{CM} output pin and V_{CC} and then bypassing the LT6402-20's V_{OCM} pin with a 0.1µF capacitor. For a common mode voltage above 1.9V, AC coupling capacitors are recommended between the LT6402-20 and LTC22XX ADCs because of the input voltage range constraints of the ADC.

Large Output Voltage Swings

The LT6402-20 has been designed to provide the $3.2V_{P-P}$ output swing needed by the LTC1748 family of 14-bit low-noise ADCs. This additional output swing improves system SNR by up to 4dB.

Input Bias Voltage and Bias Current

The input pins of the LT6402-20 are internally biased to the voltage applied to the V_{OCM} pin. No external biasing resistors are needed, even for AC-coupled operation. The input bias current is determined by the voltage difference between the input common mode voltage and the V_{OCM} pin (which sets the output common mode voltage). For example, if the inputs are tied to 2.5V with the V_{OCM} pin at 2.2V, then a total input bias current of 1mA will flow into the LT6402-20's +INA and +INB pins. Furthermore, an additional input bias current totaling 1mA will flow into the –INA and –INB inputs.

Application (Demo) Boards

The DC954A Demo Board has been created for stand-alone evaluation of the LT6402-20 with either single-ended or differential input and output signals. As shown, it accepts a single-ended input and produces a single-ended output so that the LT6402-20 can be evaluated using standard laboratory test equipment. For more information on this Demo Board, please refer to the layout and schematic diagrams found later in this data sheet.

There are also additional demo boards available that combine the LT6402-20 with a variety of different Linear Technology ADCs. Please contact the factory for more information on these demo boards.

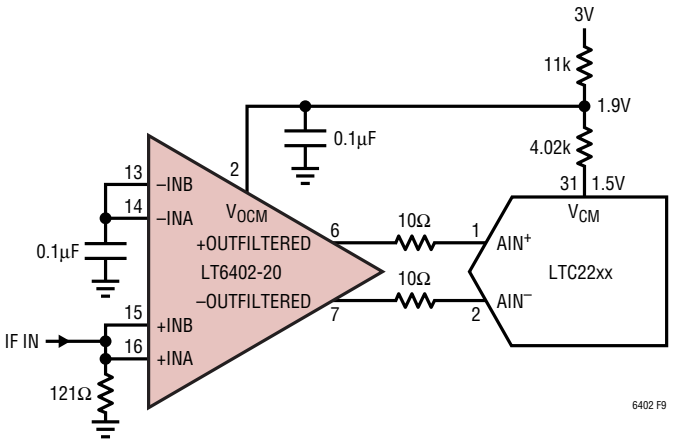
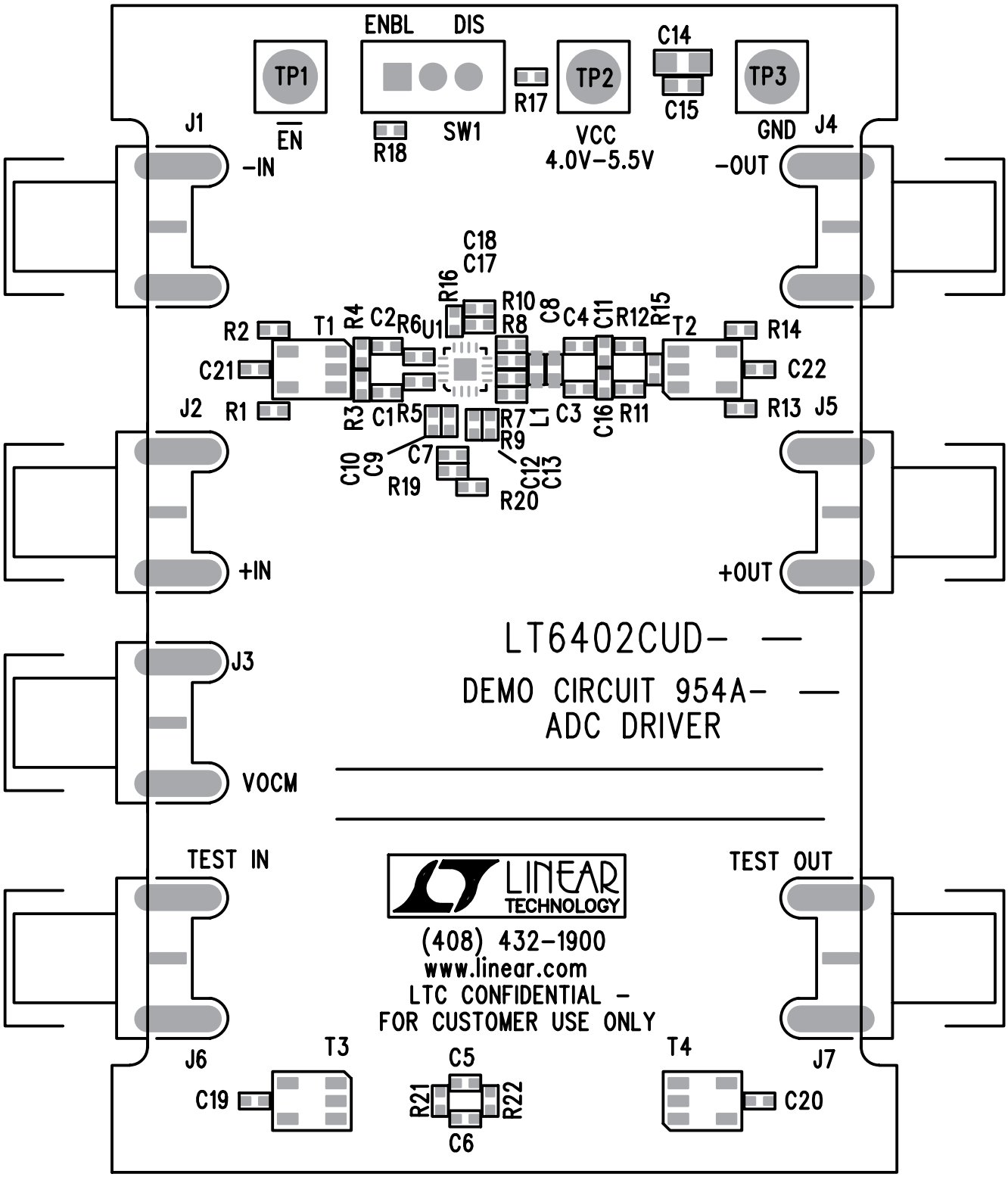


Figure 9. Level Shifting 3V ADC V_{CM} Voltage for Improved SFDR

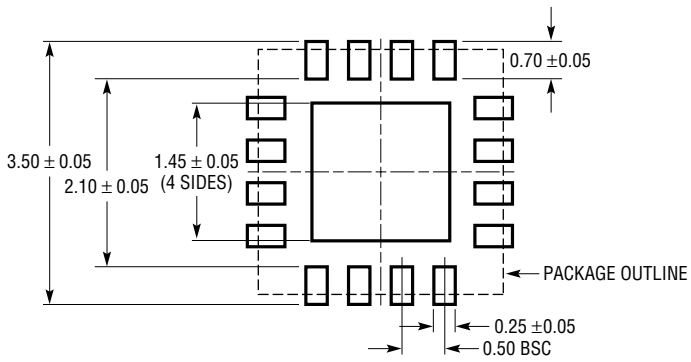
TYPICAL APPLICATION



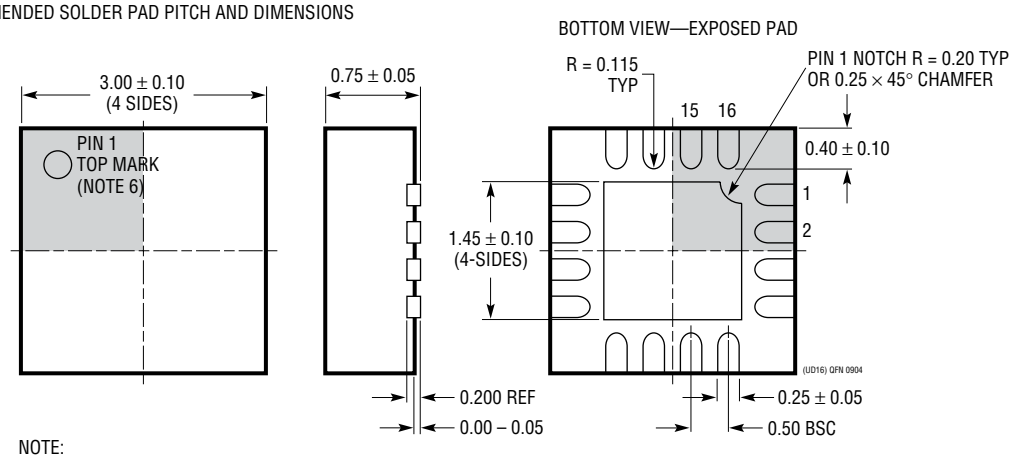
Top Silkscreen

PACKAGE DESCRIPTION

UD Package
16-Lead Plastic QFN (3mm × 3mm)
(Reference LTC DWG # 05-08-1691)



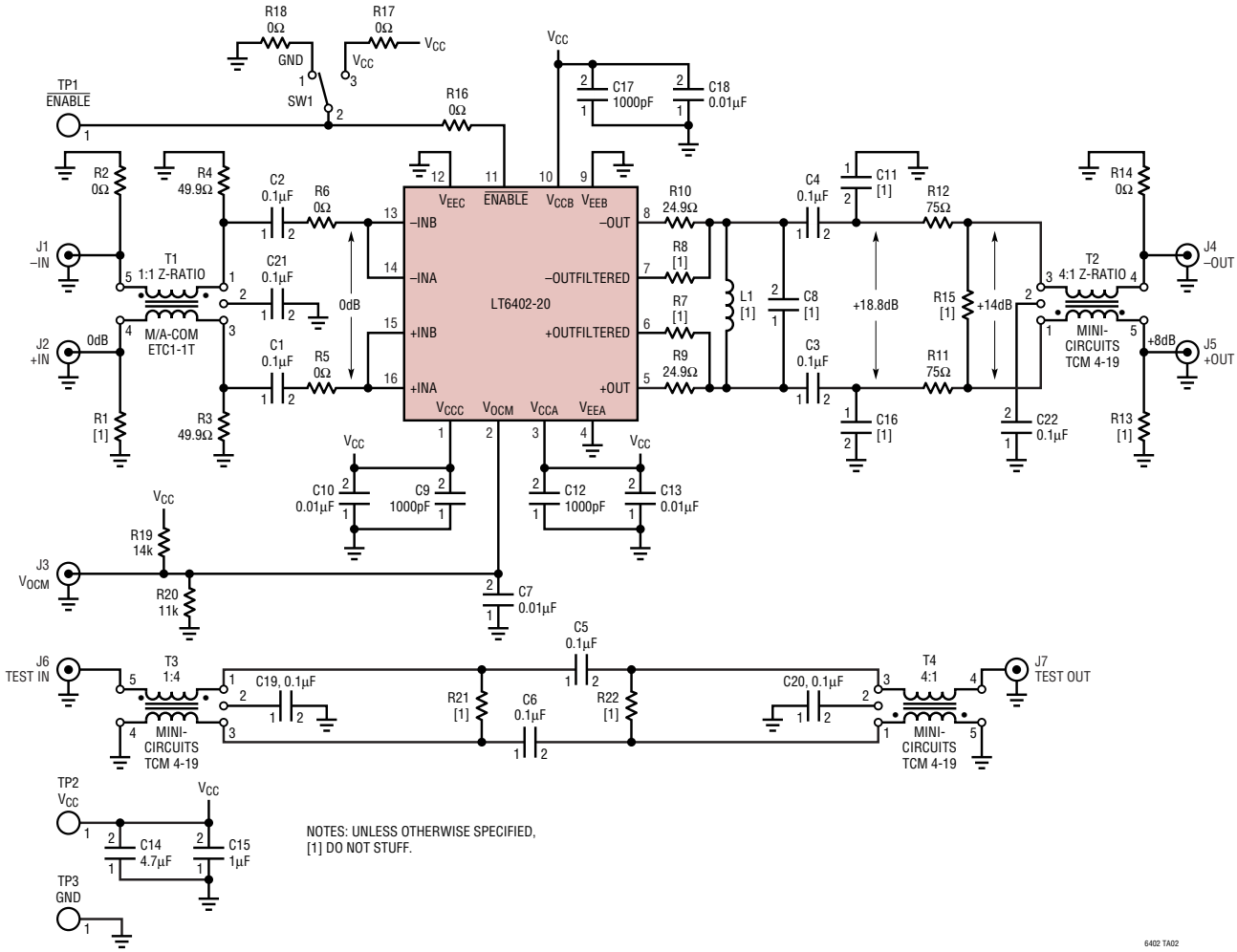
RECOMMENDED SOLDER PAD PITCH AND DIMENSIONS



NOTE:
1. DRAWING CONFORMS TO JEDEC PACKAGE OUTLINE MO-220 VARIATION (WEED-2)
2. DRAWING NOT TO SCALE
3. ALL DIMENSIONS ARE IN MILLIMETERS
4. DIMENSIONS OF EXPOSED PAD ON BOTTOM OF PACKAGE DO NOT INCLUDE MOLD FLASH. MOLD FLASH, IF PRESENT, SHALL NOT EXCEED 0.15mm ON ANY SIDE
5. EXPOSED PAD SHALL BE SOLDER PLATED
6. SHADED AREA IS ONLY A REFERENCE FOR PIN 1 LOCATION ON THE TOP AND BOTTOM OF PACKAGE

TYPICAL APPLICATION

Demo Circuit DC954A Schematic (AC Test Circuit)



RELATED PARTS

PART NUMBER	DESCRIPTION	COMMENTS
LT1993-2	800MHz Differential Amplifier/ADC Driver	A_V = 2V/V, NF = 12.3dB, OIP3 = 38dBm at 70MHz
LT1993-4	900MHz Differential Amplifier/ADC Driver	A_V = 4V/V, NF = 14.5dB, OIP3 = 40dBm at 70MHz
LT1993-10	700MHz Differential Amplifier/ADC Driver	A_V = 10V/V, NF = 12.7dB, OIP3 = 40dBm at 70MHz
LT5514	Ultralow Distortion IF Amplifier/ADC Driver	Digitally Controlled Gain Output IP3 47dBm at 100MHz
LT6600-5	Very Low Noise Differential Amplifier and 5MHz Lowpass Filter	82dB S/N with 3V Supply, SO-8 Package
LT6600-10	Very Low Noise Differential Amplifier and 10MHz Lowpass Filter	82dB S/N with 3V Supply, SO-8 Package
LT6600-20	Very Low Noise Differential Amplifier and 20MHz Lowpass Filter	76dB S/N with 3V Supply, SO-8 Package
LT6402-6	300MHz Differential Amplifier/ADC Driver	A_V = 6dB, e_n = 3.8nV/$\sqrt{Hz}$ at 20MHz, 150mV
LT6402-12	300MHz Differential Amplifier/ADC Driver	A_V = 12dB, e_n = 2.6nV/$\sqrt{Hz}$ at 20MHz, 150mV
LT6411	650MHz Differential ADC Driver/Dual Selectable Gain Amplifier	3300V/µs Slew Rate, 16mA Current Consumption, Selectable Gain: A_V = –1, +1, +2

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