# 64K X24641 8K x 8 Bit

## 400 KHz 2-Wire Serial E²PROM

### FEATURES

- **1.8V to 3.6V, 2.5V to 5.5V and 4.5V to 5.5V Power Supply Operation**
- **Low Power CMOS**
  - **—Active read current less than 1mA**
  - **—Active write current less than 3mA**
  - **—Standby current less than 1µA**
- **400KHz Fast Mode 2-Wire Serial Interface**
  - **—Down to 1.8V**
  - **—Schmitt trigger input noise suppression**
  - **—Output slope control for ground bounce noise elimination**
- **Internally Organized 8K x 8**
- **32 Byte Page Write Mode**
  - **—Minimizes total write time per byte**
- **Hardware Write Protect**
- **Bidirectional Data Transfer Protocol**
- **Self-Timed Write Cycle**
  - **—Typical Write Cycle Time of 5ms**
- **High Reliability**
  - **—Endurance: 1,000,000 cycles**
  - **—Data retention: 100 years**
- **8-Lead SOIC**

### DESCRIPTION

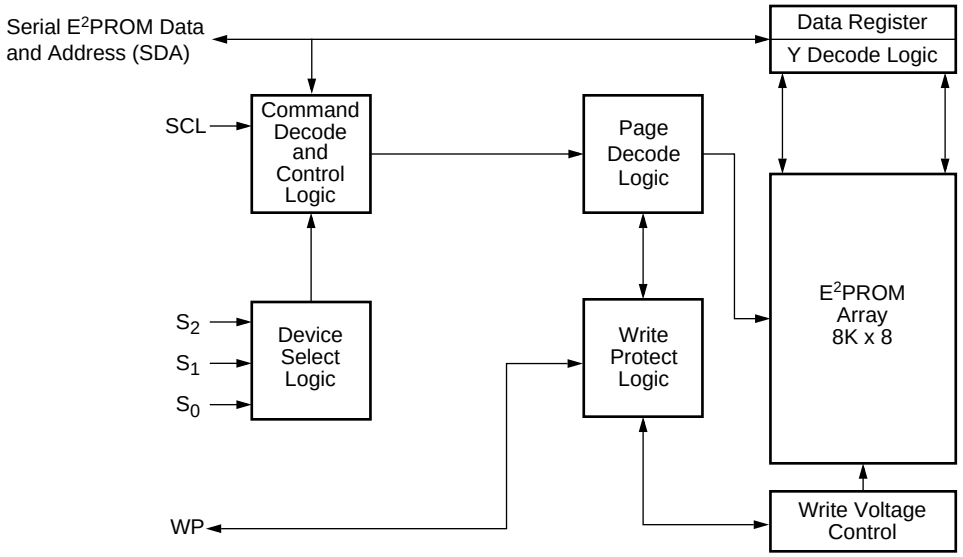
The X24641 is a CMOS Serial E²PROM Memory, internally organized 8K x 8. The device features a serial interface and software protocol allowing operation on a simple two wire bus. The bus operates at 400KHz all the way down to 1.8V.

Three device select inputs ($S_0$–$S_2$) allow up to eight devices to share a common two wire bus.

Hardware Write Protection is provided through a Write Protect (WP) input pin on the X24641. When the WP pin is HIGH, the upper quadrant of the Serial E²PROM array is protected against any nonvolatile write attempts.

Xicor Serial E²PROM Memories are designed and tested for applications requiring extended endurance. Inherent data retention is greater than 100 years.

### BLOCK DIAGRAM



## PIN DESCRIPTIONS

### Serial Clock (SCL)

The SCL input is used to clock all data into and out of the device.

### Serial Data (SDA)

SDA is a bidirectional pin used to transfer data into and out of the device. It is an open drain output and may be wire-ORed with any number of open drain or open collector outputs.

An open drain output requires the use of a pull-up resistor. For selecting typical values, refer to the Pull-up resistor selection graph at the end of this data sheet.

### Device Select ($S_0$, $S_1$, $S_2$)

The device select inputs ($S_0$, $S_1$, $S_2$) are used to set the first three bits of the 8-bit slave address. This allows up to eight devices to share a common bus. These inputs can be static or actively driven. If used statically they must be tied to $V_{SS}$ or $V_{CC}$ as appropriate. If actively driven, they must be driven with CMOS levels.

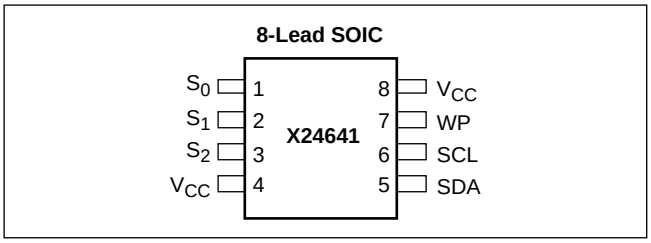
### Write Protect (WP)

The Write Protect input controls the Hardware Write Protect feature. When held LOW, Hardware Write Protection is disabled and the device can be written normally. When this input is held HIGH, Write Protection is enabled, and nonvolatile writes are disabled to the upper quadrant of the $E^2$PROM array.

## PIN NAMES

| Symbol | Description |
|---|---|
| $S_0$, $S_1$, $S_2$ | Device Select Inputs |
| SDA | Serial Data |
| SCL | Serial Clock |
| WP | Write Protect |
| $V_{SS}$ | Ground |
| $V_{CC}$ | Supply Voltage |

## PIN CONFIGURATION




## DEVICE OPERATION

The device supports a bidirectional, bus oriented protocol. The protocol defines any device that sends data onto the bus as a transmitter, and the receiving device as the receiver. The device controlling the transfer is a master and the device being controlled is the slave. The master will always initiate data transfers, and provide the clock for both transmit and receive operations. Therefore, the device will be considered a slave in all applications.

### Clock and Data Conventions

Data states on the SDA line can change only during SCL LOW. SDA state changes during SCL HIGH are reserved for indicating start and stop conditions. Refer to Figures 1 and 2.

**Figure 1. Data Validity**

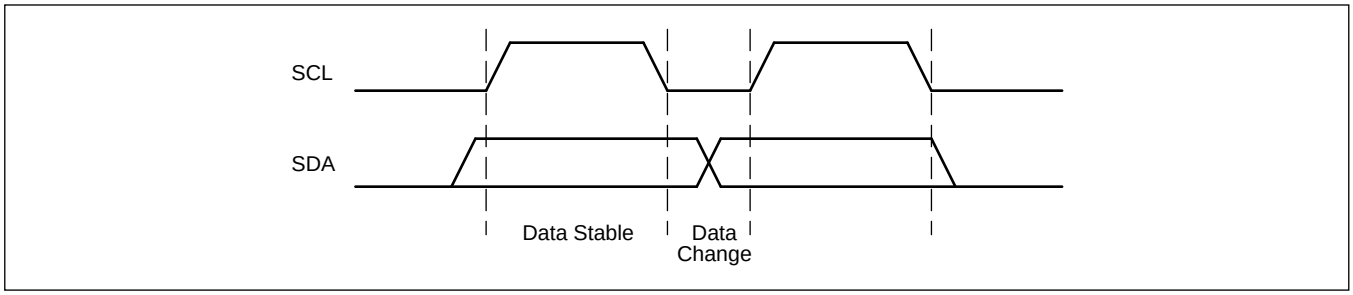
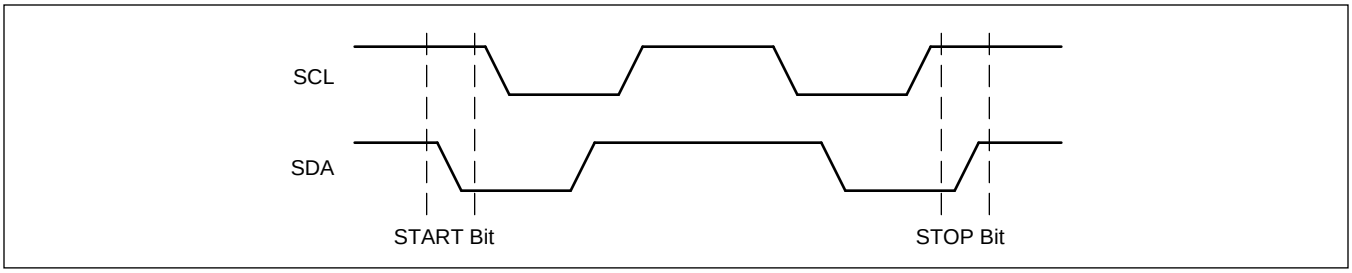


**Figure 2. Definition of Start and Stop**




### Start Condition

All commands are preceded by the start condition, which is a HIGH to LOW transition of SDA when SCL is HIGH. The device continuously monitors the SDA and SCL lines for the start condition and will not respond to any command until this condition has been met.

### Stop Condition

All communications must be terminated by a stop condition, which is a LOW to HIGH transition of SDA when SCL is HIGH. The stop condition is also used to place the device into the standby power mode after a read sequence. A stop condition can only be issued after the transmitting device has released the bus.

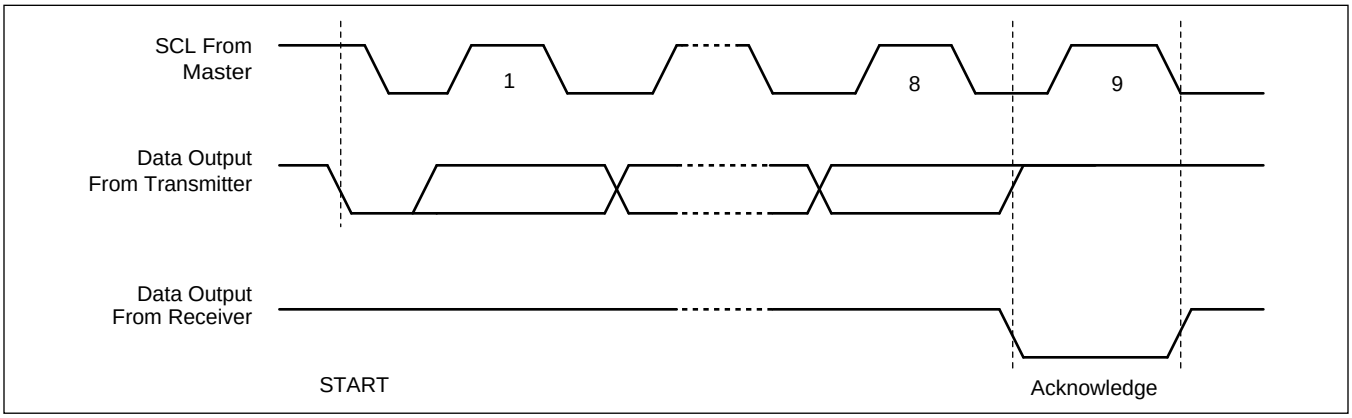
### Acknowledge

Acknowledge is a software convention used to indicate successful data transfer. The transmitting device, either master or slave, will release the bus after transmitting eight bits. During the ninth clock cycle the receiver will pull the SDA line LOW to acknowledge that it received the eight bits of data. Refer to Figure 3.

The device will respond with an acknowledge after recognition of a start condition and its slave address. If both the device and a Write Operation have been selected, the device will respond with an acknowledge after the receipt of each subsequent byte.

In the read mode the device will transmit eight bits of data, release the SDA line and monitor the line for an acknowledge. If an acknowledge is detected and no stop condition is generated by the master, the device will continue to transmit data. If an acknowledge is not detected, the device will terminate further data transmissions. The master must then issue a stop condition to return the device to the standby power mode and place the device into a known state.

**Figure 3. Acknowledge Response From Receiver**



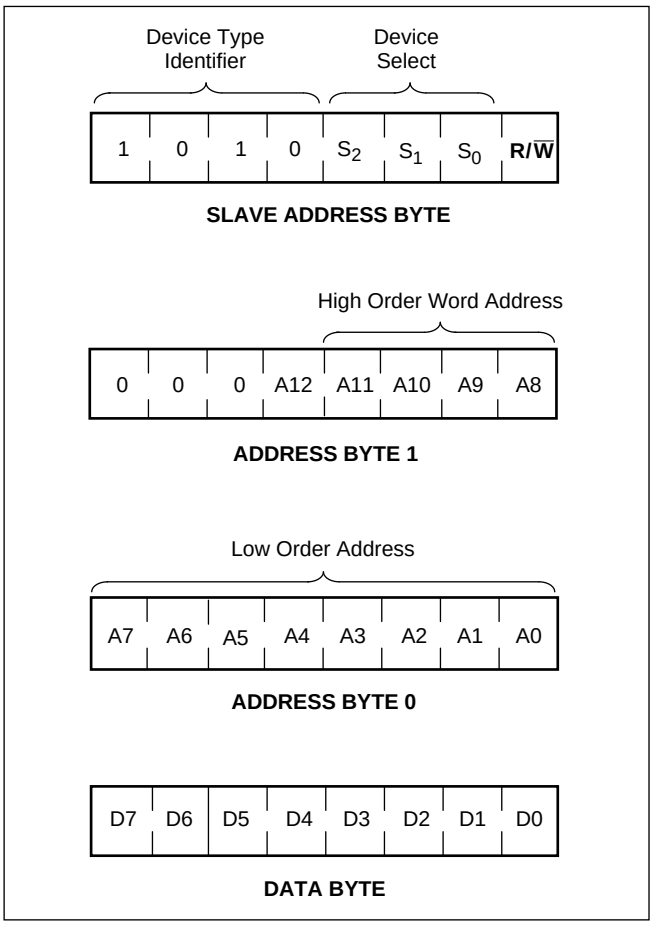
## DEVICE ADDRESSING

Following a start condition, the master must output the address of the slave it is accessing. The first four bits of the Slave Address Byte are the device type identifier bits. These must equal “1010”. The next 3 bits are the device select bits $S_0$, $S_1$, and $S_2$. This allows up to 8 devices to share a single bus. These bits are compared to the $S_0$, $S_1$, and $S_2$ device select input pins. The last bit of the Slave Address Byte defines the operation to be performed. When the R/$\overline{W}$ bit is a one, then a Read Operation is selected. When it is zero then a Write Operation is selected. Refer to Figure 4. After loading the Slave Address Byte from the SDA bus, the device compares the device type bits with the value “1010” and the device select bits with the status of the device select input pins. If the compare is not successful, no acknowledge is output during the ninth clock cycle and the device returns to the standby mode.

The byte address is either supplied by the master or obtained from an internal counter, depending on the operation. When required, the master must supply the two Address Bytes as shown in Figure 4.

The internal organization of the E$^2$PROM array is 256 pages by 32 bytes per page. The page address is partially contained in the Address Byte 1 and partially in bits 7 through 5 of the Address Byte 0. The specific byte address is contained in bits 4 through 0 of the Address Byte 0. Refer to Figure 4.

**Figure 4. Device Addressing**



## WRITE OPERATIONS

### Byte Write

For a Byte Write Operation, the device requires the Slave Address Byte, the Word Address Byte 1, and the Word Address Byte 0, which gives the master access to any one of the bytes in the array. Upon receipt of the Word Address Byte 0, the device responds with an acknowledge, and waits for the first eight bits of data. After receiving the 8 bits of the data byte, the device again responds with an acknowledge. The master then terminates the transfer by generating a stop condition, at which time the device begins the internal write cycle to the nonvolatile memory. While the internal write cycle is in progress the device inputs are disabled and the device will not respond to any requests from the master. The SDA pin is at high impedance. See Figure 4.

### Page Write Operation

The device executes a thirty-two byte Page Write Operation. For a Page Write Operation, the device requires the Slave Address Byte, Address Byte 1, and Address Byte 0. Address Byte 0 must contain the first byte of the page to be written. Upon receipt of Address Byte 0, the device responds with an acknowledge, and waits for the first eight bits of data. After receiving the 8 bits of the first data byte, the device again responds with an acknowledge. The device will respond with an acknowledge after the receipt of each of 31 more bytes. Each time the byte address is internally incremented by one, while page address remains constant. When the counter reaches the end of the page, the master terminates the data loading by issuing a stop condition, which causes the device to begin the nonvolatile write cycle. All inputs are disabled until completion of the nonvolatile write cycle. The SDA pin is at high impedance. Refer to Figure 5 for the address, acknowledge, and data transfer sequence.

**Figure 5. Byte Write Sequence**

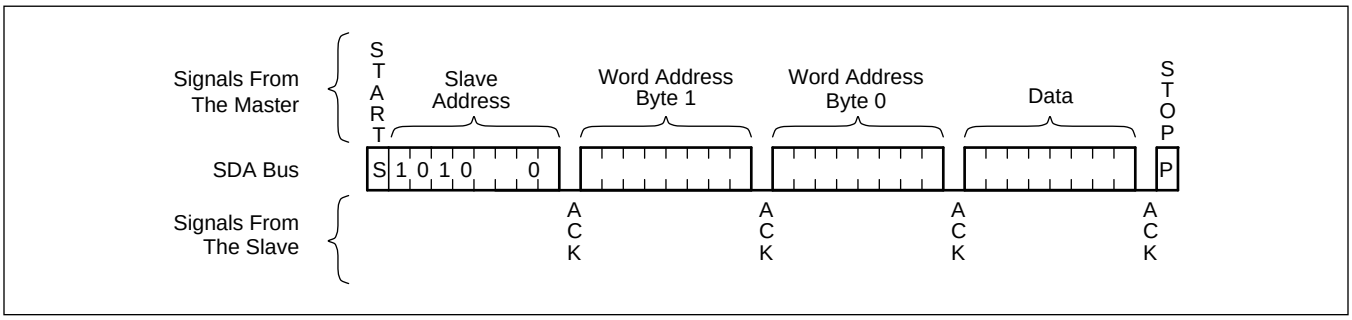
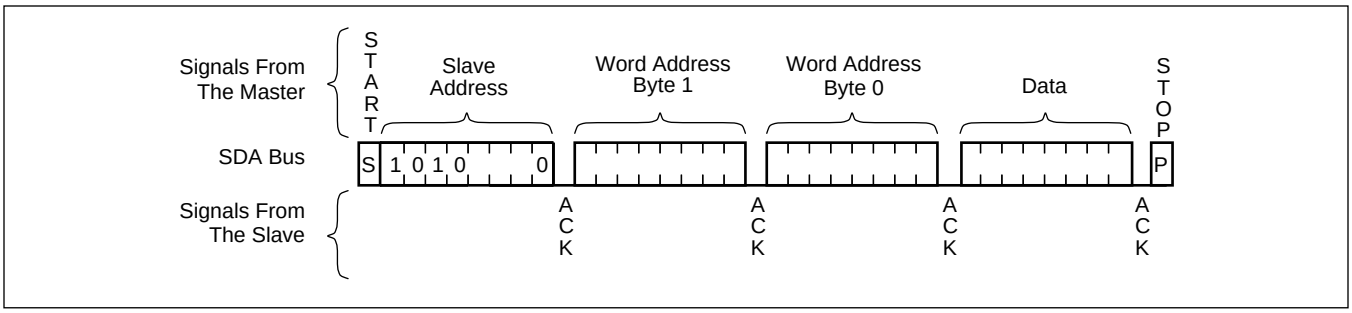


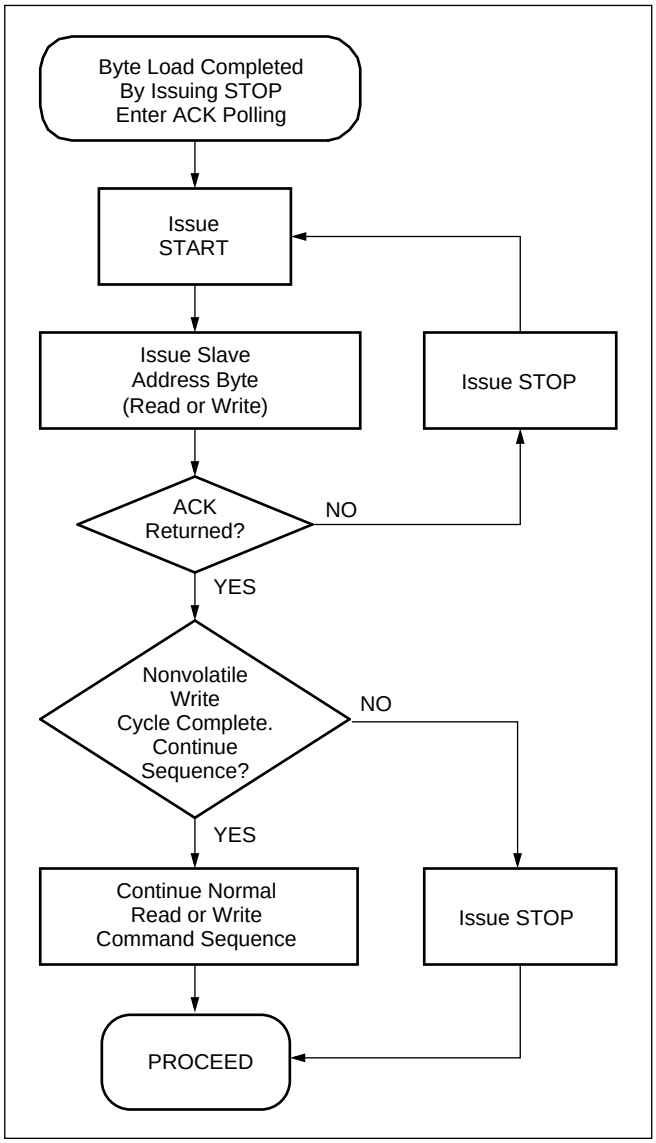

**Figure 6. Page Write Sequence**



### Acknowledge Polling

The maximum write cycle time can be significantly reduced using Acknowledge Polling. To initiate Acknowledge Polling, the master issues a start condition followed by the Slave Address Byte for a write or read operation. If the device is still busy with the nonvolatile write cycle, then no ACK will be returned. If the device has completed the nonvolatile write operation, an ACK will be returned and the host can then proceed with the read or write operation. Refer to Figure 7.

**Figure 7. Acknowledge Polling Sequence**




## READ OPERATIONS

Read operations are initiated in the same manner as write operations with the exception that the R/$\overline{W}$ bit of the Slave Address Byte is set to one. There are three basic read operations: Current Address Reads, Random Reads, and Sequential Reads.

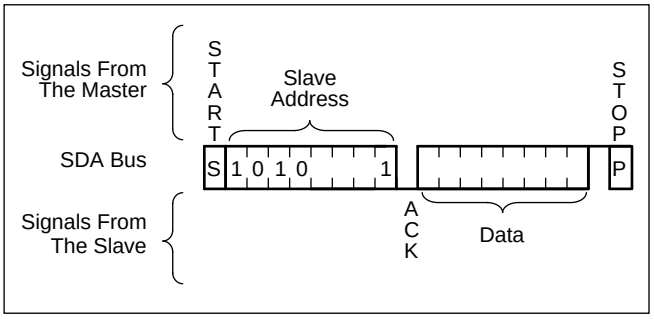
### Current Address Read

Internally, the device contains an address counter that maintains the address of the last byte read or written, incremented by one. After a read operation from the last address in the array, the counter will “roll over” to the first address in the array. After a write operation to the last address in a given page, the counter will “roll over” to the first address of the same page.

Upon receipt of the Slave Address Byte with the R/$\overline{W}$ bit set to one, the device issues an acknowledge and then transmits the byte at the current address. The master terminates the read operation when it does not respond with an acknowledge during the ninth clock and then issues a stop condition. Refer to Figure 8 for the address, acknowledge, and data transfer sequence.

It should be noted that the ninth clock cycle of the read operation is not a “don’t care.” To terminate a read operation, the master must either issue a stop condition during the ninth cycle or hold SDA HIGH during the ninth clock cycle and then issue a stop condition.

**Figure 8. Current Address Read Sequence**



### Random Read

Random read operation allows the master to access any memory location in the array. Prior to issuing the Slave Address Byte with the R/$\overline{W}$ bit set to one, the master must first perform a “Dummy” write operation. The master issues the start condition and the Slave Address Byte with the R/$\overline{W}$ bit low, receives an acknowledge, then issues Address Byte 1, receives another acknowledge, then issues Address Byte 0 containing the address of the byte to be read. After the device acknowledges receipt of Address Byte 0, the master issues another start condition and the Slave Address Byte with the R/$\overline{W}$ bit set to one. This is followed by an acknowledge and then eight bits of data from the device. The master terminates the read operation by not responding with an acknowledge and then issuing a stop condition. Refer to Figure 9 for the address, acknowledge, and data transfer sequence.

The device will perform a similar operation called “Set Current Address” if a stop is issued instead of the second start shown in Figure 9. The device will go into standby mode after the stop and all bus activity will be ignored until a start is detected. The effect of this operation is that the new address is loaded into the address counter, but no data is output by the device.

The next Current Address Read operation will read from the newly loaded address.

### Sequential Read

Sequential reads can be initiated as either a current address read or random read. The first byte is transmitted as with the other modes; however, the master now responds with an acknowledge, indicating it requires additional data. The device continues to output data for each acknowledge received. The master terminates the read operation by not responding with an acknowledge and then issuing a stop condition.

The data output is sequential, with the data from address n followed by the data from address n + 1. The address counter for read operations increments through all byte addresses, allowing the entire memory contents to be read during one operation. At the end of the address space the counter “rolls over” to address 0000h and the device continues to output data for each acknowledge received. Refer to Figure 9 for the acknowledge and data transfer sequence.

**Figure 9. Random Read Sequence**

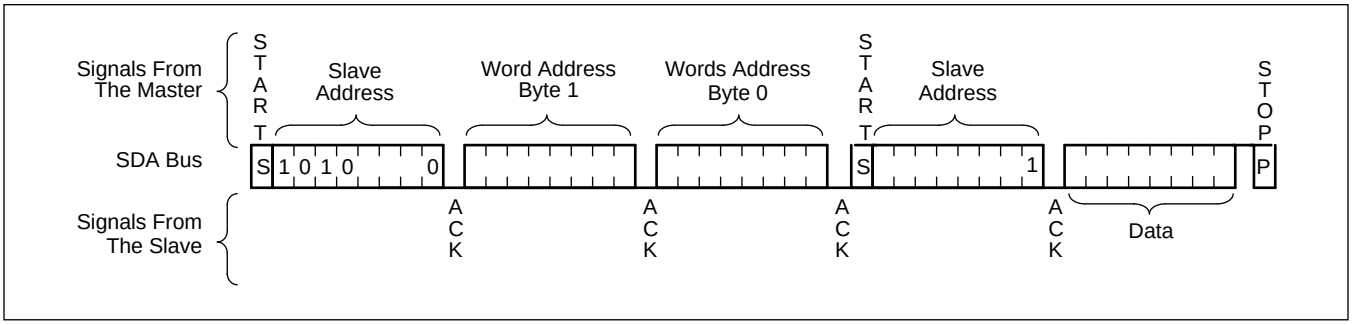
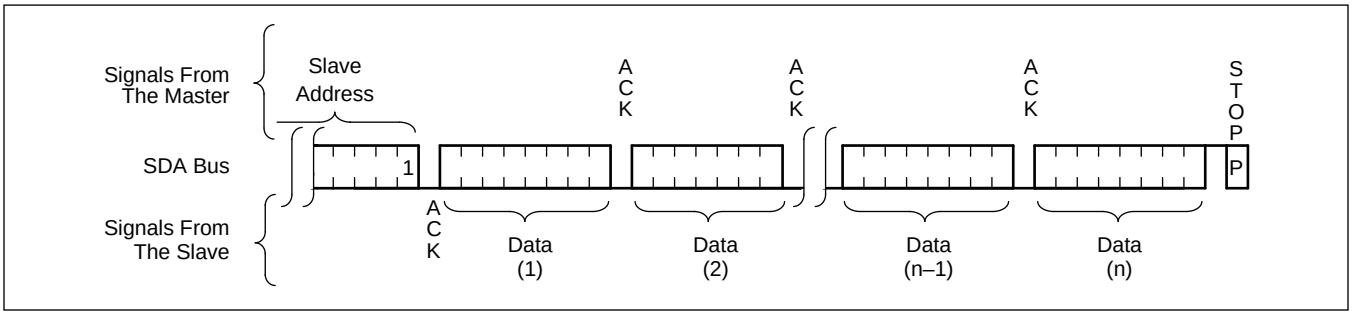



**Figure 10. Sequential Read Sequence**



### ABSOLUTE MAXIMUM RATINGS

Temperature under bias X24641 .....–65 to +135°C
Storage temperature .....–65 to +150°C
Voltage on any pin with respect to $V_{SS}$.....–1V to +7V
D.C. output current ..... 5mA
Lead temperature (soldering, 10 seconds).....300°C

### COMMENT

Stresses above those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. This is a stress rating only; at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

### RECOMMENDED OPERATING CONDITIONS

| Temperature | Min. | Max. |
|---|---|---|
| Commercial | 0°C | +70°C |
| Industrial | –40°C | +85°C |

| Supply Voltage | Limits |
|---|---|
| X24641 | 4.5V to 5.5V |
| X24641–2.5 | 2.5V to 5.5V |
| X24641–1.8 | 1.8V to 3.6V |

### D.C. OPERATING CHARACTERISTICS

| Symbol | Parameter | Limits | | Units | Test Conditions |
|---|---|---|---|---|---|
| | | Min. | Max. | | |
| $I_{CC1}$ | $V_{CC}$ Supply Current (Read) | | 1 | mA | SCL = $V_{CC}$ X 0.1/$V_{CC}$ X 0.9 Levels @ 400KHz, SDA = Open, All Other Inputs = $V_{SS}$ or $V_{CC}$ – 0.3V |
| $I_{CC2}$ | $V_{CC}$ Supply Current (Write) | | 3 | mA | |
| $I_{SB1}$(1) | $V_{CC}$ Standby Current | | 3 | µA | SCL = SDA = $V_{CC}$ – 0.3V, All Other Inputs = $V_{SS}$ or $V_{CC}$ – 0.3V, $V_{CC}$ = 5V ± 10% |
| $I_{SB2}$(1) | $V_{CC}$ Standby Current | | 1 | µA | SCL = SDA = $V_{CC}$ – 0.1V, All Other Inputs = $V_{SS}$ or $V_{CC}$ – 0.1V, $V_{CC}$ = 1.8V |
| $I_{LI}$ | Input Leakage Current | | 10 | µA | $V_{IN}$ = $V_{SS}$ to $V_{CC}$ |
| $I_{LO}$ | Output Leakage Current | | 10 | µA | $V_{OUT}$ = $V_{SS}$ to $V_{CC}$ |
| $V_{IL}$(2) | Input LOW Voltage | –0.5 | $V_{CC}$ x 0.3 | V | |
| $V_{IH}$(2) | Input HIGH Voltage | $V_{CC}$ x 0.7 | $V_{CC}$ + 0.5 | V | |
| $V_{OL}$ | Output LOW Voltage | | 0.4 | V | $I_{OL}$ = 3mA |
| $V_{hys}$(3) | Hysteresis of Schmitt Trigger Inputs | $V_{CC}$ x 0.05 | | V | |

**CAPACITANCE** $T_A$ = +25°C, f = 1MHz, $V_{CC}$ = 5V

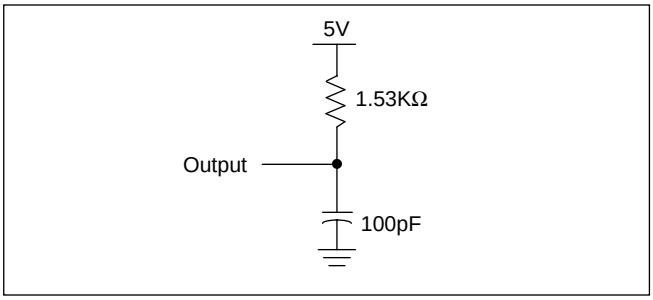
| Symbol | Parameter | Max. | Units | Test Conditions |
|---|---|---|---|---|
| $C_{I/O}$(3) | Input/Output Capacitance (SDA) | 8 | pF | $V_{I/O}$ = 0V |
| $C_{IN}$(3) | Input Capacitance ($S_0$, $S_1$, $S_2$, SCL,WP) | 6 | pF | $V_{IN}$ = 0V |

**Notes:** (1) Must perform a stop command prior to measurement.
(2) $V_{IL}$ min. and $V_{IH}$ max. are for reference only and are not 100% tested.
(3) This parameter is periodically sampled and not 100% tested.

### A.C. CONDITIONS OF TEST

| | |
|---|---|
| Input pulse levels | $V_{CC}$ x 0.1 to $V_{CC}$ x 0.9 |
| Input rise and fall times | 10ns |
| Input and output timing levels | $V_{CC}$ X 0.5 |

### EQUIVALENT A.C. LOAD CIRCUIT




**A.C. OPERATING CHARACTERISTICS** (Over the recommended operating conditions, unless otherwise specified.)

**Read & Program Cycle Limits**

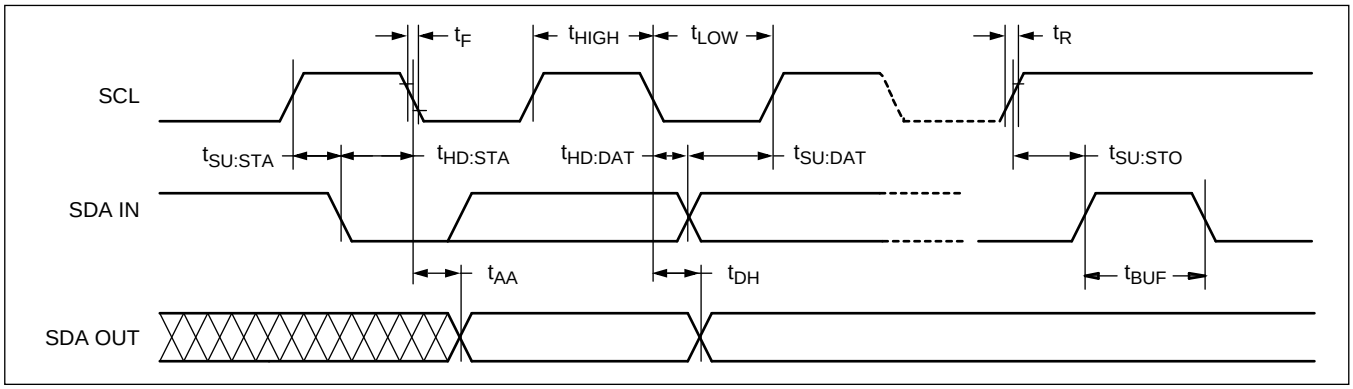
| Symbol | Parameter | Min. | Max. | Units |
|---|---|---|---|---|
| $f_{SCL}$ | SCL Clock Frequency | 0 | 400 | KHz |
| $T_I$ | Noise Suppression Time Constant at SCL, SDA Inputs | 50 | | ns |
| $t_{AA(6)}$ | SCL LOW to SDA Data Out Valid | 0.1 | 0.9 | µs |
| $t_{BUF}$ | Time the Bus Must Be Free Before a New Transmission Can Start | 1.2 | | µs |
| $t_{HD:STA}$ | Start Condition Hold Time | 0.6 | | µs |
| $t_{LOW}$ | Clock LOW Period | 1.2 | | µs |
| $t_{HIGH}$ | Clock HIGH Period | 0.6 | | µs |
| $t_{SU:STA}$ | Start Condition Setup Time (for a Repeated Start Condition) | 0.6 | | µs |
| $t_{HD:DAT}$ | Data In Hold Time | 0 | | µs |
| $t_{SU:DAT}$ | Data In Setup Time | 100 | | ns |
| $t_R$ | SDA and SCL Rise Time | $20+0.1XC_b$(5) | 300 | ns |
| $t_F$ | SDA and SCL Fall Time | $20+0.1XC_b$(5) | 300 | ns |
| $t_{SU:STO}$ | Stop Condition Setup Time | 0.6 | | µs |
| $t_{DH}$ | Data Out Hold Time | 50 | | ns |
| $t_{OF}$ | Output Fall Time | $20 + 0.1C_b$(5) | 250 | ns |

**POWER-UP TIMING(4)**

| Symbol | Parameter | Max. | Units |
|---|---|---|---|
| $t_{PUR}$ | Power-up to Read Operation | 1 | ms |
| $t_{PUW}$ | Power-up to Write Operation | 5 | ms |

**Notes:** (4) $t_{PUR}$ and $t_{PUW}$ are the delays required from the time $V_{CC}$ is stable until the specified operation can be initiated. These parameters are periodically sampled and not 100% tested.
(5) $C_b$ = total capacitance of one bus line in pF
(6) $t_{AA}$ = 1.1µs Max below $V_{CC}$ = 2.5V.

### Bus Timing



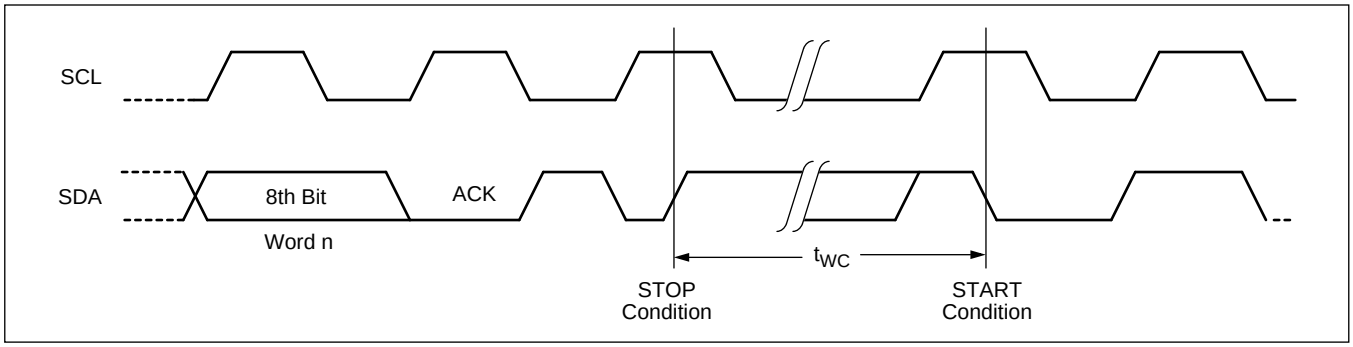

### Write Cycle Limits

| Symbol | Parameter | Min. | Typ.(6) | Max. | Units |
|---|---|---|---|---|---|
| $t_{WC}$(8) | Write Cycle Time | | 5 | 10 | ms |

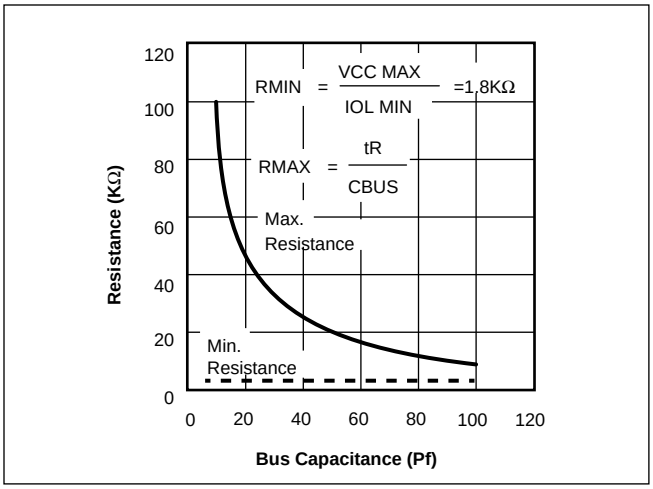
**Notes:** (7) Typical values are for $T_A$ = 25°C and nominal supply voltage (5V).
(8) $t_{WR}$ is the minimum cycle time to be allowed from the system perspective unless polling techniques are used. It is the maximum time the device requires to automatically complete the internal write operation.

The write cycle time is the time from a valid stop condition of a write sequence to the end of the internal erase/write cycle. During the write cycle, the X24641 bus interface circuits are disabled, SDA is allowed to remain HIGH, and the device does not respond to its slave address.

### Bus Timing



## Guidelines for Calculating Typical Values of Bus Pull-Up Resistors

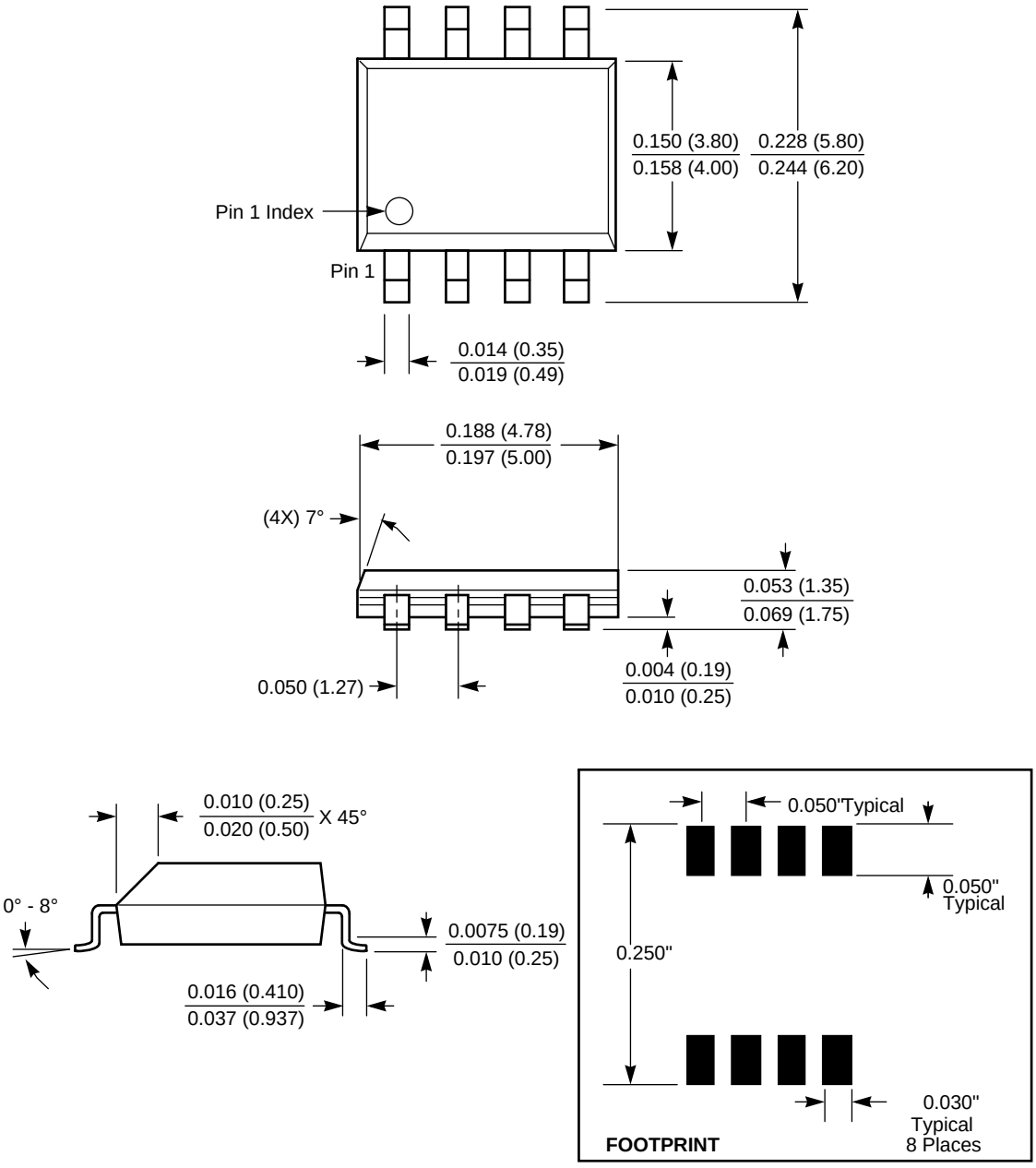



## Symbol Table

| WAVEFORM | INPUTS | OUTPUTS |
|---|---|---|
| | Must be steady | Will be steady |
| | May change from Low to High | Will change from Low to High |
| | May change from High to Low | Will change from High to Low |
| | Don't Care: Changes Allowed | Changing: State Not Known |
| | N/A | Center Line is High Impedance |

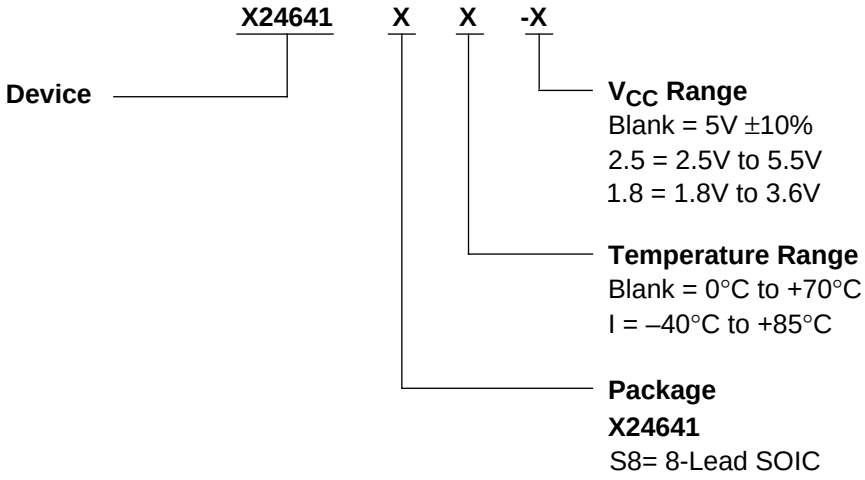
## PACKAGING INFORMATION

### 8-Lead Plastic Small Outline Gull Wing Package Type S




**NOTE: ALL DIMENSIONS IN INCHES (IN PARENTHESES IN MILLIMETERS)**

## Ordering Information



## Part Mark Convention

**X24641**

**X** — Blank = 8-Lead SOIC

**X**

- Blank = 4.5V to 5.5V, 0°C to +70°C
- I = 4.5V to 5.5V, –40°C to +85°C
- AE = 2.5V to 5.5V, 0°C to +70°C
- AF = 2.5V to 5.5V, –40°C to +85°C
- AG = 1.8V to 3.6V, 0°C to +70°C
- AH = 1.8V to 3.6V, –40°C to +85°C