DATA SHEET

SUNPLUS

SPLC782A

16COM/80SEG Controller/Driver

FEB. 15, 2005

Version 1.7

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16COM/80SEG CONTROLLER/DRIVER

1. GENERAL DESCRIPTION

The SPLC782A, a dot-matrix LCD controller and driver, is a low-power CMOS integrated circuit. The SPLC782A is capable of connecting with MPU for LCD application and easily to be used for designing the low-cost products.

2. FEATURES

- Character generator ROM: 10880 bits
  - Character font 5 x 8 dots: 192 characters
  - Character font 5 x 10 dots: 64 characters
- 4 type CGROM mode, Max. 256 characters can be used.
- Character generator RAM: 512 bits
  - Character font 5 x 8 dots: 8 characters
  - Character font 5 x 10 dots: 4 characters
- Provide connecting to 4-bit or 8-bit MPU
- Direct driver for LCD: 16 COMs x 80 SEGs
- 80-channel Bi-Direction segment driver
- 16-channel Bi-direction common driver
- Duty factor (selected by program):
  - 1/8 duty: 1 line of 5 x 8 dots
  - 1/11 duty: 1 line of 5 x 10 dots
  - 1/16 duty: 2 lines of 5 x 8 dots / line
- LCD type-A, type-B waveform can be selected.
- Built-in power on automatic reset circuit
- Built-in oscillator circuit (with internal resistor)
- Built-in Bias resistor
- Support external clock operation
- Package form: Au bump chip

3. BLOCK DIAGRAM

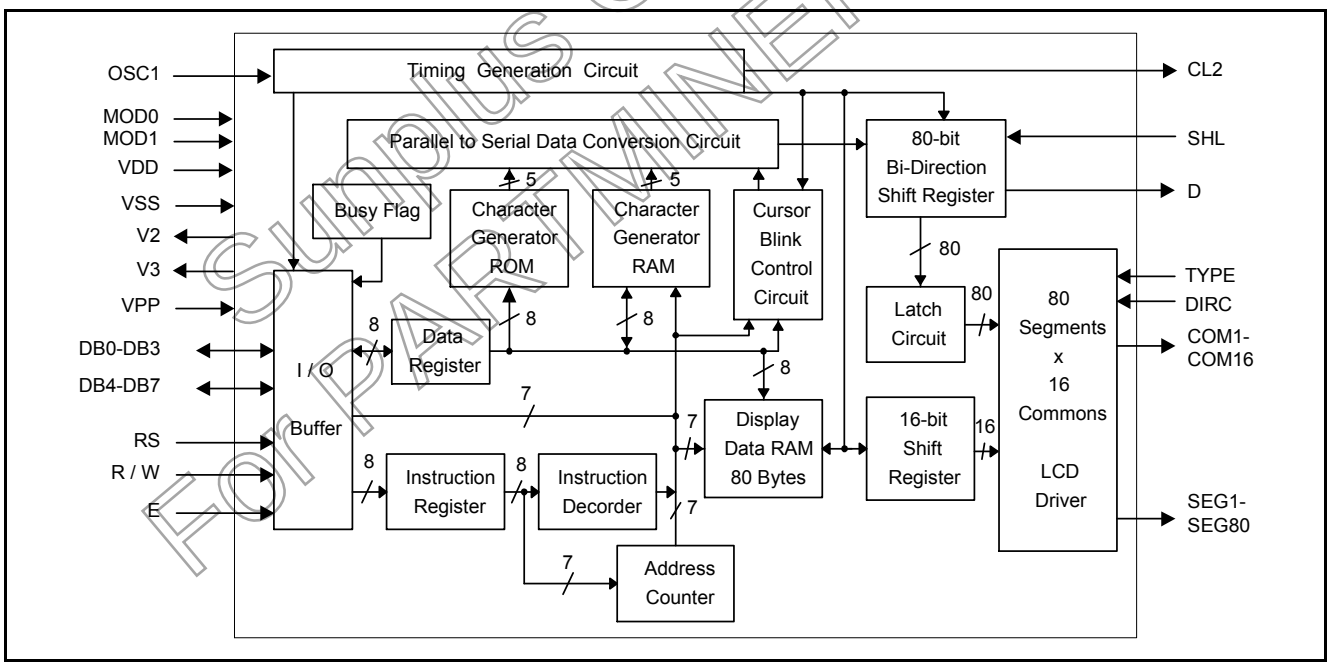


Figure 3-1: Block Diagram

4. SIGNAL DESCRIPTIONS

Mnemonic	PIN No.	Type	Description
VDD	19, 20, 28	I	Logic Power input
VSS	11, 12, 37	I	Ground
VPP	23, 24	I	LCD Voltage; V_{LCD} = VPP - VSS
V2 V3	22 21	I	LCD Bias Voltage Control. Open for 1/5 Bias, Short for 1/4 Bias
E	27	I	It is a start signal to read data or write data.
R / W	26	I	It is a signal to select read or write. 1: Read, 0: Write.
RS	25	I	It is a signal to select register. 1: Data register (for read and write) 0: Instruction register (for write), Busy flag -- address counter (for read).
DB3 - DB0	32 - 29	I/O	Low-order 4 data bits
DB7 - DB4	36 - 33	I/O	High-order 4 data bits
SEG80 - SEG1	46 - 125	O	Segment signals for LCD.
COM16 - COM9	45 - 38	O	Common signals for LCD.
COM8 - COM1	1 - 8	O	Common signals for LCD.
TYPE	14	I	LCD Alternate Signals. TYPE = 0: Type-A TYPE = 1: Type-B
DIRC	15	I	Common Scan Direction DIRC = 0: COM1 → COM2 → … → COM15 → COM16 DIRC = 1: COM16 → COM15 → … → COM2 → COM1
SHL	16	I	Segment Shift Direction SHL = 0: SEG1 → SEG2 → … → SEG79 → SEG80 SHL = 1: SEG80 → SEG79 → … → SEG2 → SEG1
MOD1 MOD0	18 17	I	CGROM / CGRAM Mode Select
OSC1	13		For internal clock operation, leave this pin open. For external clock operation, the clock is input to OSC1.
CL2	10	O	Test Mode Clock Output; Open for normally use.
D	9	O	Test Mode Data Output; Open for normally use.

MOD1	MOD0	Function
1	1	$00 - $0F as CGRAM
1	0	$00 - $07 as CGRAM, $08 - $0F as CGROM
0	1	$00 - $03 as CGRAM, $04 - $0F as CGROM
0	0	$00 - $0F as CGROM

5. FUNCTIONAL DESCRIPTIONS

5.1. Oscillator

The built-in RC oscillator generates suitable clock for SPLC782A operation.

5.2. Control and Display Instructions

Control and display instructions is shown as follows:

5.2.1. Clear display

	RS	R/W	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
Code	0	0	0	0	0	0	0	0	0	1

Figure 5-1: Clear Display Instruction Code

It clears the whole display and sets display data RAM′s address 0 in address counter.

5.2.2. Return home

	RS	R/W	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
Code	0	0	0	0	0	0	0	0	1	X

Figure 5-2: Return Home Instruction Code

X: Do not care (0 or 1)

It sets display data RAM′s address 0 in address counter and display returns to its original position. The cursor or blink goes to the left edge of the display (to the 1st line if 2 lines are displayed). The content of the Display Data RAM does not change.

5.2.3. Entry mode set

During writing and reading data, it sets cursor move direction and shifts the display.

	RS	R/W	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
Code	0	0	0	0	0	0	0	1	I/D	S

Figure 5-3: Entry Mode Instruction Code

I / D = 1: Increment, I / D = 0: Decrement.

S = 1: The display shift, S = 0: The display does not shift.

S = 1	I / D = 1	It shifts the display to the left
S = 1	I / D = 0	It shifts the display to the right

Figure 5-4: Shift Direction Patterns According to S and I/D Bits

5.2.4. Display ON/OFF control

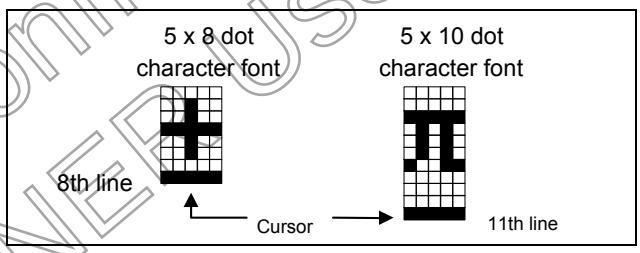
	RS	R/W	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
Code	0	0	0	0	0	0	1	D	C	B

Figure 5-5: Display ON/OFF Control Instruction Code

D = 1: Display on, D = 0: Display off

C = 1: Cursor on, C = 0: Cursor off

B = 1: Blinks on, B = 0: Blinks off



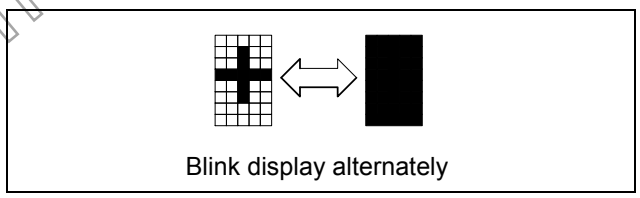


Figure 5-6: Cursor and Blinking

5.2.5. Cursor or display shift

Without changing DD RAM′s data, it can move cursor and shift display.

	RS	R/W	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
Code	0	0	0	0	0	1	S/C	R/L	X	X

Figure 5-7: Cursor or Display Shift Instruction Code

S/C	R/L	Description	Address Counter
0	0	Shift cursor to the left	AC = AC - 1
0	1	Shift cursor to the right	AC = AC + 1
1	0	Shift display to the left. Cursor follows the display shift	AC = AC
1	1	Shift display to the right. Cursor follows the display shift	AC = AC

Figure 5-8: Shift Patterns According to S/C and R/L Bits

5.2.6. Function set

	RS	R/W	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
Code	0	0	0	0	1	DL	N	F	X	X

Figure 5-9: Function Set Instruction Code

X: Do not care (0 or 1)

DL: It sets interface data length.

DL = 1: Datas are transferred with 8-bit lengths (DB0 - DB7).

DL = 0: Datas are transferred with 4-bit lengths (DB4 - DB7).

(It requires two times to transfer data)

N: It sets the number of the display line.

N = 0: One-line display.

N = 1: Two-line display.

F: It sets the character font.

F = 0: 5 x 8 dots character font.

F = 1: 5 x 10 dots character font.

N	F	No. of Display Lines	Character Font	Duty Factor
0	0	1	5 x 8 dots	1 / 8
0	1	1	5 x 10 dots	1 / 11
1	X	2	5 x 8 dots	1 / 16

Figure 5-10: Function Set Description

It cannot display two lines with 5 x 10 dot character font.

5.2.7. Set character generator RAM address

	RS	R/W	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
Code	0	0	0	1	a	a	a	a	a	a

Figure 5-11: Set CGRAM address Instruction Code

It sets character generator RAM address $(aaaaaa)_2$ to the address counter. Character generator RAM data can read or write after this setting.

5.2.8. Set display data RAM address

	RS	R/W	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
Code	0	0	1	a	a	a	a	a	a	a

Figure 5-12: Set DDRAM address Instruction Code

It sets display data RAM address $(aaaaaaa)_2$ to the address counter.

Display data RAM can read or write after this setting.

In one-line display (N = 0),

$(aaaaaaa)_{2:}$ $(00)_{16}$ - $(4F)_{16.}$

In two-line display (N = 1),

$(aaaaaaa)_{2:}$ $(00)_{16}$ - $(27)_{16}$ for the first line,

$(aaaaaaa)_{2:}$ $(40)_{16}$ - $(67)_{16}$ for the second line.

5.2.9. Read busy flag and address

	RS	R/W	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
Code	0	1	BF	AC6	AC5	AC4	AC3	AC2	AC1	AC0

Figure 5-13: Read busy flag and address Instruction Code

When (BF = 1) indicates that the system is busy now; it will not accept any instruction until no busy (BF = 0). At the same time, the address counter contents $(aaaaaaa)_2$ is read out.

5.2.10. Write data to character generator RAM or display data RAM

	RS	R/W	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
Code	1	0	d	d	d	d	d	d	d	d

Figure 5-14: Write Data to CGRAM/DDRAM Instruction Code

It writes data $(dddddddd)_2$ to character generator RAM or display data RAM.

5.2.11. Read data from character generator RAM or display data RAM

	RS	R/W	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
Code	1	1	d	d	d	d	d	d	d	d

Figure 5-15: Read Data from CGRAM/DDRAM Instruction Code

It reads data $(dddddddd)_2$ from character generator RAM or display data RAM.

To get the correct data readout is shown belows:

1). Set the address of the character generator RAM or display data RAM or shift the cursor instruction.

2). Send the “Read” instruction.

5.3. Instruction Table

Instruction	Instruction Code										Description	Max. Execution time (Temp = -20℃ ~ +75℃)
	RS	RW	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0		
Clear Display	0	0	0	0	0	0	0	0	0	1	Write "20H" to DDRAM and set DDRAM address to "00H" from AC	4.1ms
Return Home	0	0	0	0	0	0	0	0	1	-	Set DDRAM address to "00H" from AC and return cursor to its original position if shifted. The contents of DDRAM are not changed.	4.1ms
Entry Mode Set	0	0	0	0	0	0	0	1	I/D	S	Assign cursor moving direction and enable the shift of entire display	100μs
Display ON/ OFF Control	0	0	0	0	0	0	1	D	C	B	Set display (D), cursor(C), and blinking of cursor(B) on/off control bit.	100μs
Cursor or Display Shift	0	0	0	0	0	1	S/C	R/L	-	-	Set cursor moving and display shift control bit, and the direction, without changing of DDRAM data.	100μs
Function Set	0	0	0	0	1	DL	N	F	-	-	Set interface data length (DL: 8-bit/4-bit), numbers of display line (N: 2-line/1-line) and, display font type (F:5x10 dots/5x8 dots)	100μs
Set CGRAM Address	0	0	0	1	AC5	AC4	AC3	AC2	AC1	AC0	Set CGRAM address in address counter.	100μs
Set DDRAM Address	0	0	1	AC6	AC5	AC4	AC3	AC2	AC1	AC0	Set DDRAM address in address counter	100μs
Read Busy Flag and Address Counter	0	1	BF	AC6	AC5	AC4	AC3	AC2	AC1	AC0	Whether during internal operation or not can be known by reading BF. The contents of address counter can also be read.	0μs
Write Data to RAM	1	0	D7	D6	D5	D4	D3	D2	D1	D0	Write data into internal RAM (DDRAM/CGRAM).	100μs
Read Data from RAM	1	1	D7	D6	D5	D4	D3	D2	D1	D0	Read data from internal RAM (DDRAM/CGRAM).	100μs

Figure 5-16: Instruction Table

Note: "-" don't care

5.4. 8-Bit Operation and 16-Digit 1-Line Display (Using Internal Reset)

NO.	Instruction	Display	Operation
1	Power on. (SPLC782A starts initializing)		Power on reset. No display.
2	Function set RS R/W DB7 DB6 DB5 DB4 DB3 DB2 DB1 DB0 0 0 0 0 1 1 0 0 X X		Set to 8-bit operation and select 1-line display line and character font.
3	Display on / off control 0 0 0 0 0 0 1 1 1 0	_	Display on. Cursor appear.
4	Entry mode set 0 0 0 0 0 0 0 1 1 0	_	Increase address by one. It will shift the cursor to the right when writing to the DD RAM/CG RAM. Now the display has no shift.
5	Write data to CG RAM / DD RAM 1 0 0 1 0 1 0 1 1 1	W_	Write " W ". The cursor is incremented by one and shifted to the right.
6	Write data to CG RAM / DD RAM 1 0 0 1 0 0 0 1 0 1	WE_	Write " E ". The cursor is incremented by one and shifted to the right.
7	:	:	
8	Write data to CG RAM / DD RAM 1 0 0 1 0 0 0 1 0 1	WELCOME_	Write " E ". The cursor is incremented by one and shifted to the right.
9	Entry mode set 0 0 0 0 0 0 0 1 1 1	WELCOME_	Set mode for display shift when writing
10	Write data to CG RAM / DD RAM 1 0 0 0 1 0 0 0 0 0	ELCOME _	Write " "(space). The cursor is incremented by one and shifted to the right.
11	Write data to CG RAM / DD RAM 1 0 0 1 0 0 0 0 1 1	LCOME C_	Write " C ". The cursor is incremented by one and shifted to the right.
12	:	:	
13	Write data to CG RAM / DD RAM 1 0 0 1 0 1 1 0 0 1	COMPAMY _	Write " Y ". The cursor is incremented by one and shifted to the right.
14	Cursor or display shift 0 0 0 0 0 1 0 0 X X	COMPAMY _	Only shift the cursor's position to the left (Y).
15	Cursor or display shift 0 0 0 0 0 1 0 0 X X	COMPAMY	Only shift the cursor's position to the left (M).
16	Write data to CG RAM / DD RAM 1 0 0 1 0 0 1 1 1 0	COMPANY	Write " N ". The display moves to the left.
17	Cursor or display shift 0 0 0 0 0 1 1 1 X X	COMPANY	Shift the display and the cursor's position to the right.
18	Cursor or display shift 0 0 0 0 0 1 0 1 X X	COMPANY_	Shift the display and the cursor's position to the right.
19	Write data to CG RAM / DD RAM 1 0 0 1 0 0 0 0 0 0	COMPANY _	Write " " (space). The cursor is incremented by one and shifted to the right.
20	:	:	
21	Return home 0 0 0 0 0 0 0 0 1 0	WELCOME _	Both the display and the cursor return to the original position (address 0).

Figure 5-17: 8-Bit Operation and 16-Digit 1-Line Display

5.5. 4-Bit Operation and 16-Digit 1-Line Display (Using Internal Reset)

NO.	Instruction	Display	Operation
1	Power on. (SPLC782A starts initializing)		Power on reset. No display.
2	Function set RS R/W DB7 DB6 DB5 DB4 0 0 0 0 1 0		Set to 4-bit operation.
3	Function set 0 0 0 0 1 0 0 0 0 0 X X		Set to 4-bit operation and select 1-line display line and character font.
4	Display on / off control 0 0 0 0 0 0 0 0 1 1 1 0	_	Display on. Cursor appears.
5	Entry mode set 0 0 0 0 0 0 0 0 0 1 1 0	_	Increase address by one. It will shift the cursor to the right when writing to the DD RAM/CG RAM. Now the display has no shift.
6	Write data to CG RAM / DD RAM 1 0 0 1 0 1 1 0 0 1 1 1	W_	Write " W ". The cursor is incremented by one and shifted to the right.

Figure 5-18: 4-Bit Operation and 16-Digit 1-Line Display

5.6. 8-Bit Operation and 16-Digit 2-Line Display (Using Internal Reset)

NO.	Instruction	Display	Operation
1	Power on. (SPLC782A starts initializing)		Power on reset. No display.
2	Function set RS R/W DB7 DB6 DB5 DB4 DB3 DB2 DB1 DB0 0 0 0 0 1 1 1 0 X X		Set to 8-bit operation and select 2-line display line and 5 x 7 dot character font.
3	Display on / off control 0 0 0 0 0 0 1 1 1 0	_	Display on. Cursor appear.
4	Entry mode set 0 0 0 0 0 0 0 1 1 0	_	Increase address by one. It will shift the cursor to the right when writing to the DD RAM/CG RAM. Now the display has no shift.
5	Write data to CG RAM / DD RAM 1 0 0 1 0 1 0 1 1 1	W_	Write " W ". The cursor is incremented by one and shifted to the right.
6	:	:	
7	Write data to CG RAM / DD RAM 1 0 0 1 0 0 0 1 0 1	WELCOME_	Write " E ". The cursor is incremented by one and shifted to the right.
8	Set DD RAM address 0 0 1 1 0 0 0 0 0 0	WELCOME _	It sets DD RAM's address. The cursor is moved to the beginning position of the 2nd line.
9	Write data to CG RAM / DD RAM 1 0 0 1 0 1 0 1 0 0	WELCOME T_	Write " T ". The cursor is incremented by one and shifted to the right.
10	:	:	
11	Write data to CG RAM / DD RAM 1 0 0 1 0 1 0 1 0 0	WELCOME TO PART_	Write " T ". The cursor is incremented by one and shifted to the right.

NO.	Instruction	Display	Operation
12	Write data to CG RAM / DD RAM 1 0 0 1 0 1 0 1 0 0	WELCOME TO PART_	Write " T ". The cursor is incremented by one and shifted to the right.
13	Entry mode set 0 0 0 0 0 0 0 1 1 1	WELCOME TO PART_	When writing, it sets mode for the display shift.
14	Write data to CG RAM / DD RAM 1 0 0 1 0 1 1 0 0 1	ELCOME O PARTY_	Write " Y ". The cursor is incremented by one and shifted to the right.
15	:	:	
16	Return home 0 0 0 0 0 0 0 0 1 0	WELCOME TO PARTY	Both the display and the cursor return to the original position (address 0).

Figure 5-19: 8-Bit Operation and 16-Digit 2-Line Display

5.7. Reset Function

At power on, it starts the internal auto-reset circuit and executes the initial instructions. There are the initial procedures shown as belows:

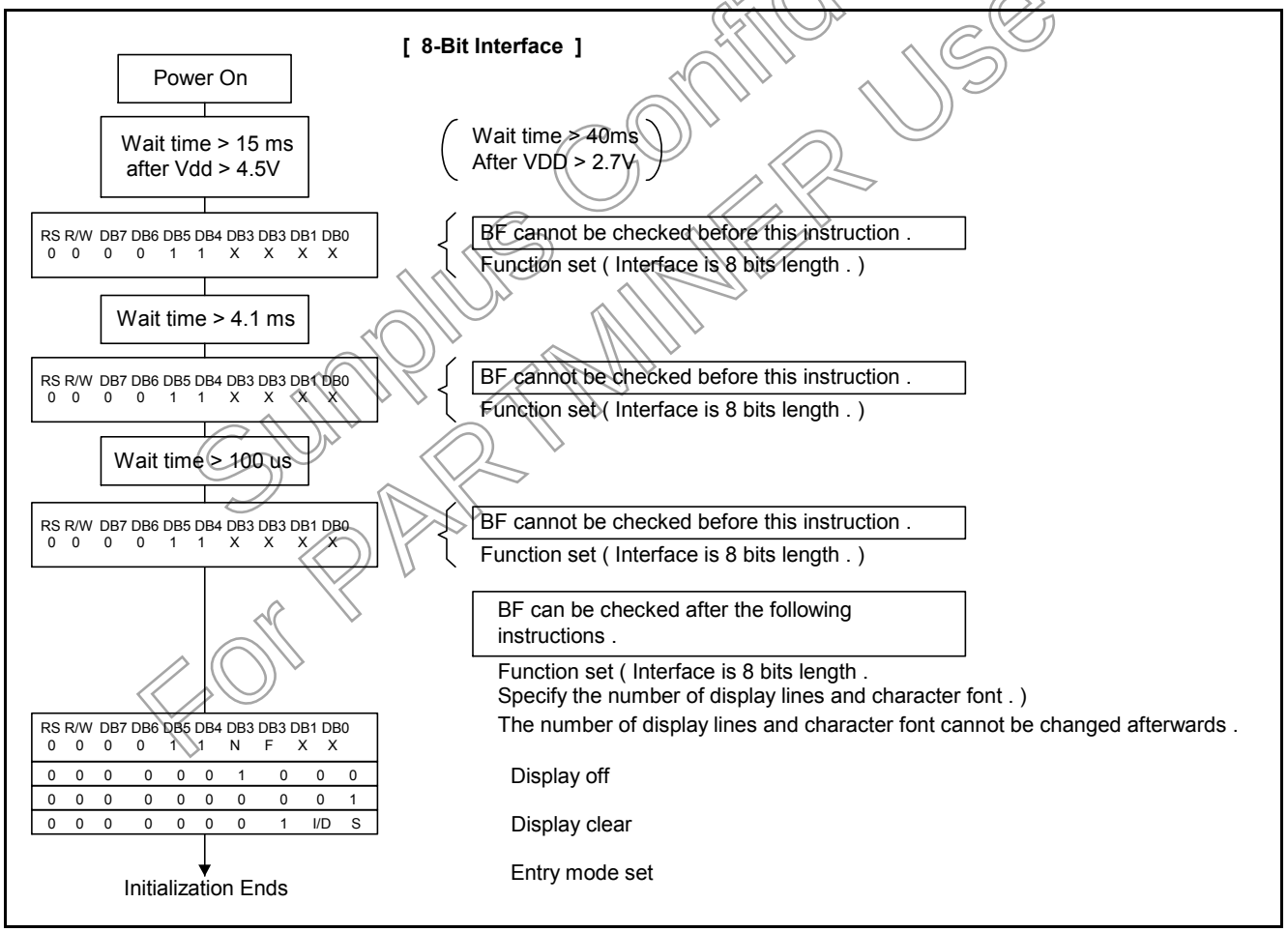


Figure 5-20: Reset Function (8-bit Interface)

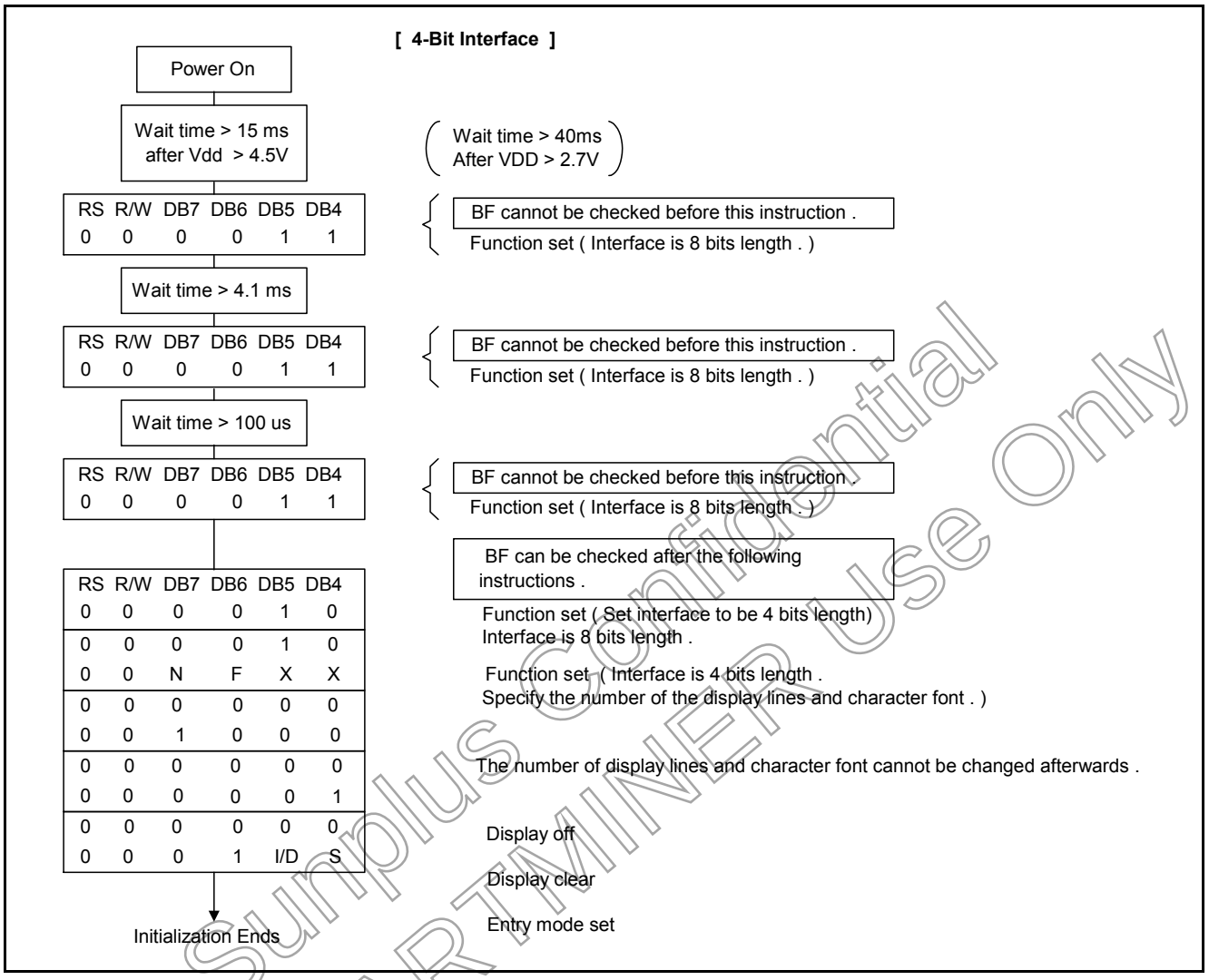


Figure 5-21: Reset Function (4-bit Interface)

5.8. Display Data RAM (DD RAM)

The DD RAM stores display data and its RAM size is 80 bytes. The area in DD RAM that is not used for display can be used as a general data RAM. Its address is set in the address counter.

There are the relations between the display data RAM′s address and the LCD′s position shown belows.

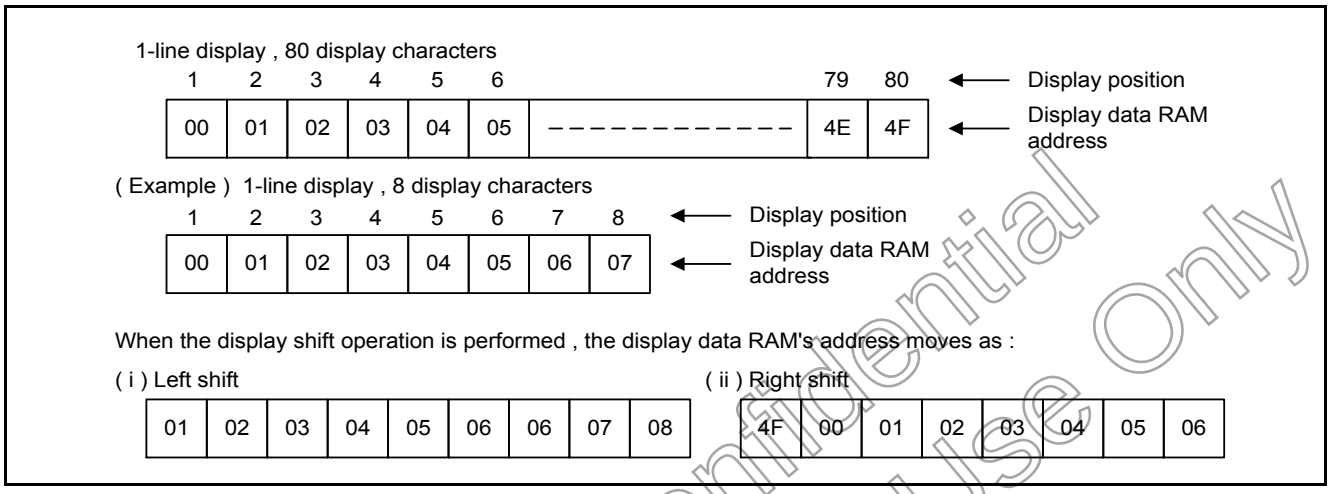


Figure 5-22: Relations Between Display Data Ram's Address and the LCD's Position

5.9. Timing Generation Circuit

The timing generation circuit can generate needed timing signals to the internal circuits. To prevent the internal timing interface, the MPU access timing and the RAM access timing are separately generated.

5.10. LCD Driver Circuit

There are 16 commons x 80 segments signal drivers in the LCD driver circuit. When a program specifies the character fonts and line numbers, the corresponding common signals will output drive waveforms and the others still output unselected waveforms.

5.11. Character Generator ROM (CG ROM)

Using 8-bit character code, the character generator ROM generates 5 x 8 dot or 5 x 10 dot character patterns. It also can generate 192 5 x 8 dot character patterns and 64 5 x 10 dot character patterns.

5.12. Character Generator RAM (CG RAM)

Using the programs, users can easily change the character patterns in the character generator RAM. It can be written with 5 x 8 dots, 8 character patterns or written with 5 x 10 dots, 4 character patterns.

Here are the SPLC782A's character patterns shown as belows:

Correspondence between Character Codes and Character Patterns.

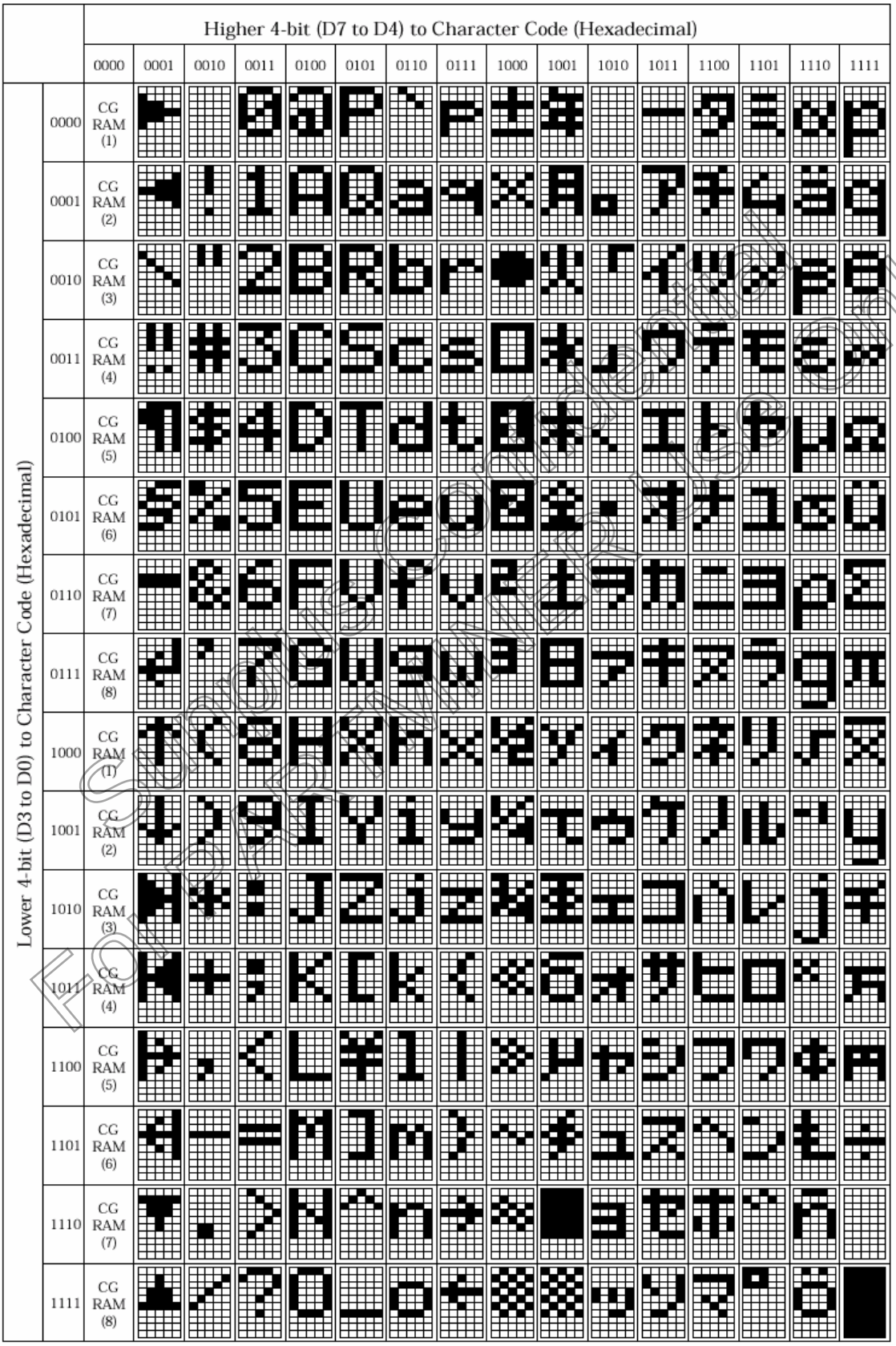


Figure 5-23: Character Code and Character Patterns

The relations between character generator RAM addresses, character generator RAM data (character patterns) and character codes are shown as belows:

5.12.1. 5 x 8 dot character patterns

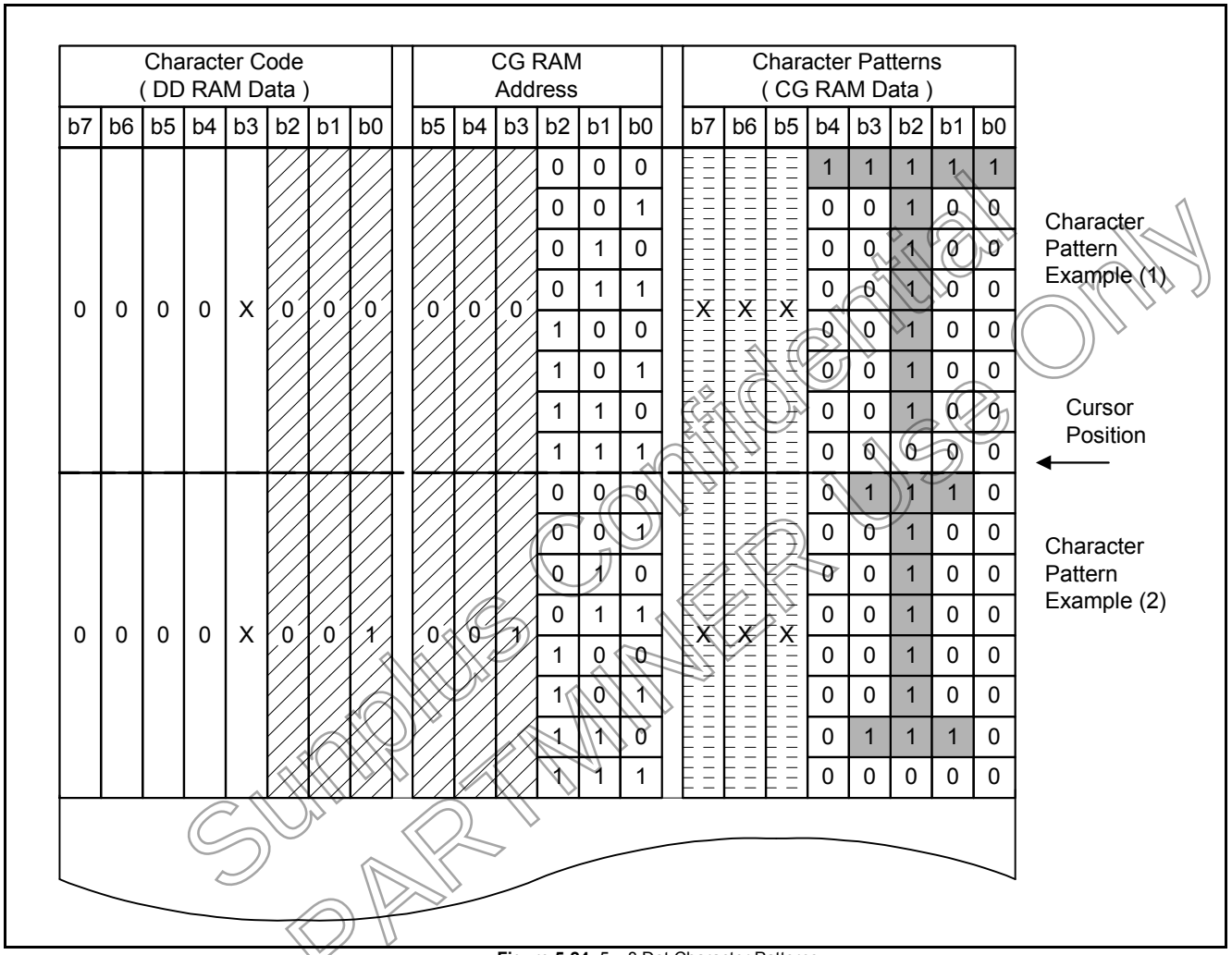


Figure 5-24: 5 x 8 Dot Character Patterns

Note1: It means that the bit0~2 of the character code correspond to the bit3~5 of the CG RAM address.

Note2: These areas are not used for display, but can be used for the general data RAM.

Note3: When all of the bit4-7 of the character code are 0, CG RAM character patterns are selected.

Note4: " 1 ": Selected, " 0 " : No selected , " X " : Do not care (0 or 1).

Note5: For example (1), set character code (b2 = b1 = b0 = 0, b3 = 0 or 1, b7-b4 = 0) to display " T ". That means character code (00) 16,and (08) 16 can display " T " character.

Note6: The bits 0-2 of the character code RAM is the character pattern line position. The 8th line is the cursor position and display is formed by logical OR with the cursor.

5.12.2. 5 X 10 dot character patterns

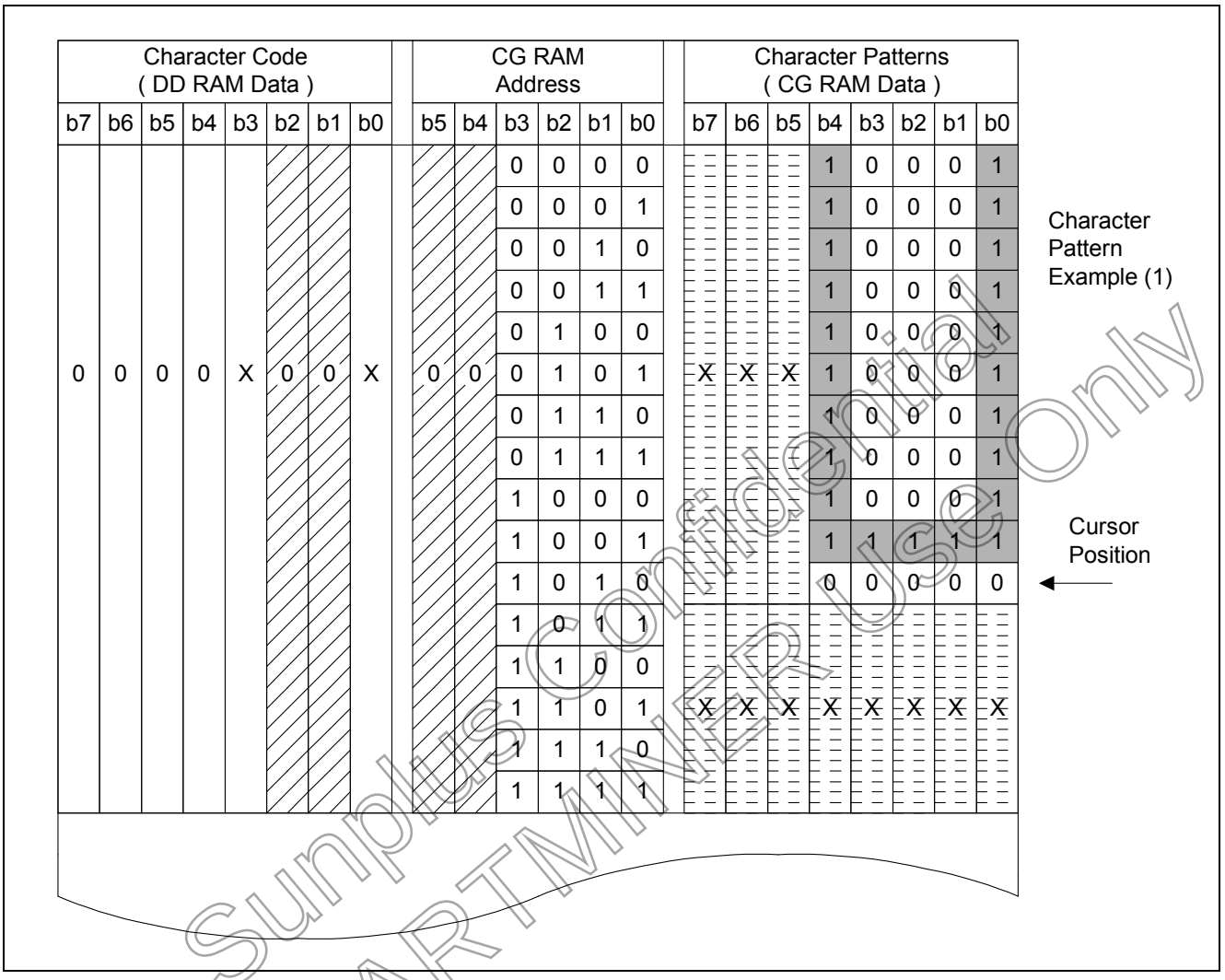


Figure 5-25: 5 x 10 Dot Character Patterns

Note1: ▨ It means that the bit1~2 of the character code correspond to the bit4~5 of the CG RAM address.

Note2: ▤ These areas are not used for display, but can be used for the general data RAM.

Note3: When all of the bit4-7 of the character code are 0, CG RAM character patterns are selected.

Note4: " 1 ": Selected, " 0 ": No selected, " X ": Do not care (0 or 1).

Note5: For example (1), set character code (b2 = b1 = 0, b3 = b0 = 0 or 1, b7-b4 = 0) to display " U ". That means all of the character codes (00) 16, (01) 16, (08) 16,and (09) 16 can display " U " character.

Note6: The bits 0-3 of the character code RAM is the character pattern line position. The 11th line is the cursor position and display is formed by logical OR with the cursor.

5.13. Cursor/Blink Control Circuit

It can generate the cursor or blink in the cursor / blink control circuit. The cursor or the blink appears in the digit at the display data RAM address set in the address counter.

When the address counter is $(07)_{16}$, the cursor's position is shown as follows:

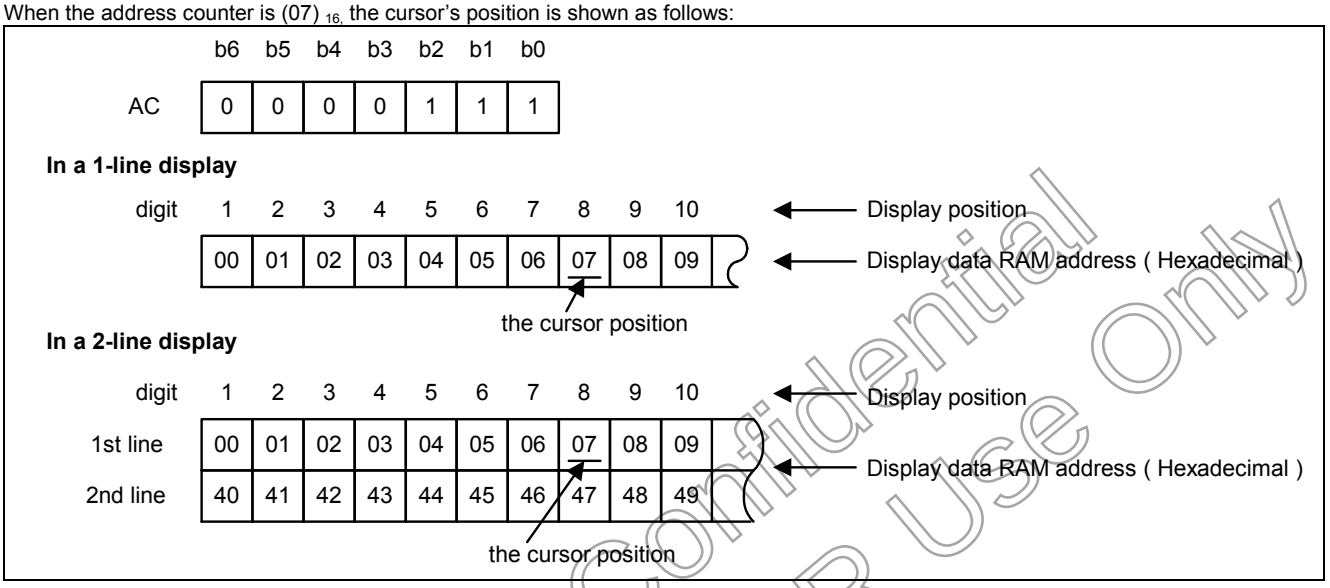


Figure 5-26: Cursor/Blink Control

5.14. Interfacing to MPU

There are two types of data operations: 4-bit operation and 8-bit operation. Using 4-bit MPU, the interfacing 4-bit data is transferred by 4 bus lines (for 8-bit operation, DB7 to DB4). The bus lines of DB0 - DB3 are not used. Using 4-bit MPU to interface 8-bit data needs two times. First, the higher 4-bit data is transferred by 4-busline (for 8-bit operation, DB7 to DB4). Secondly, the lower 4-bit data is transferred by 4 bus lines (for 8-bit operation, DB3 to DB0). Using 8-bit MPU, the interfacing 8-bit data is transferred by 8 bus lines (DB0 - DB7).

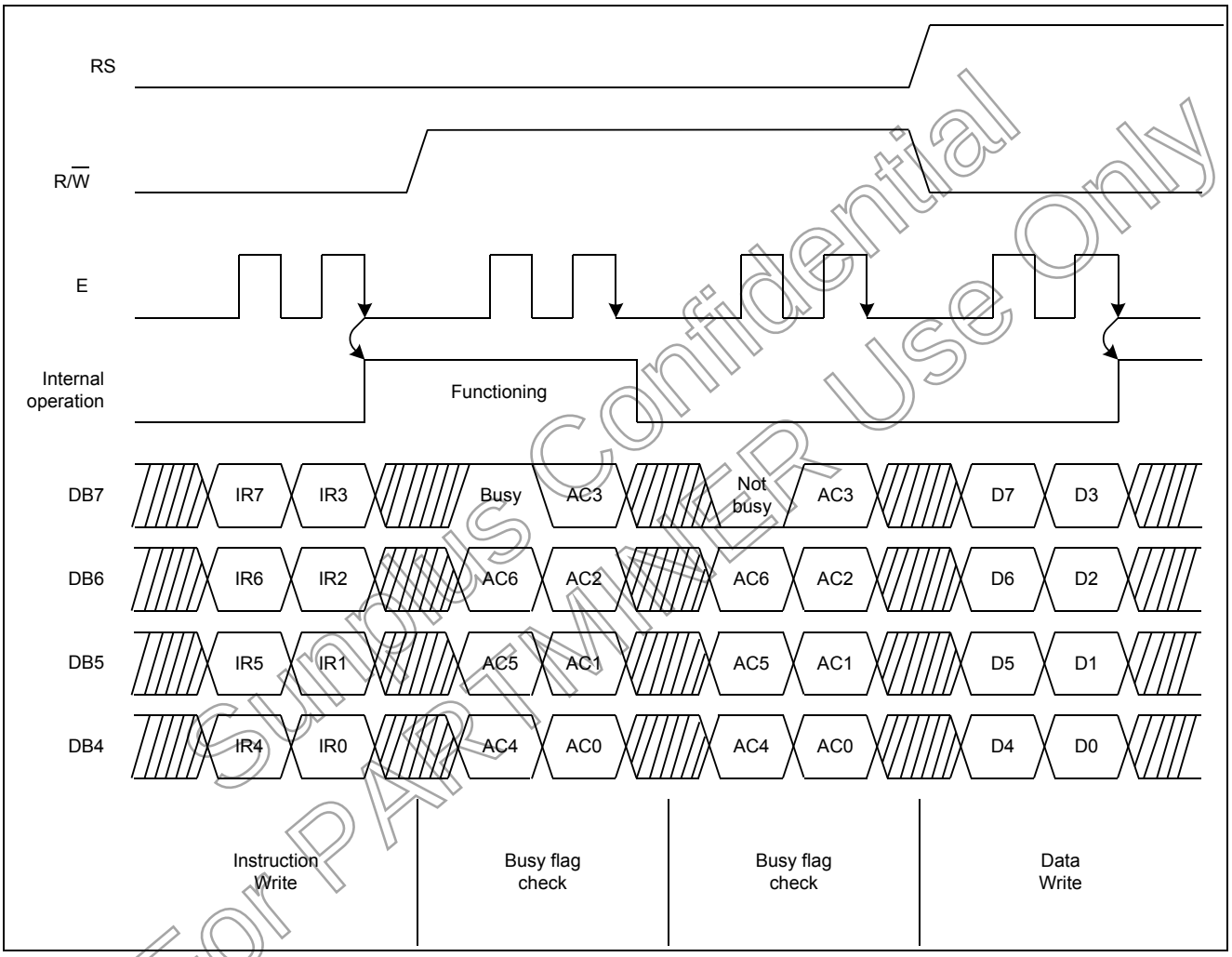


Figure 5-27: Example of 4-bit Data Transfer Timing Sequence

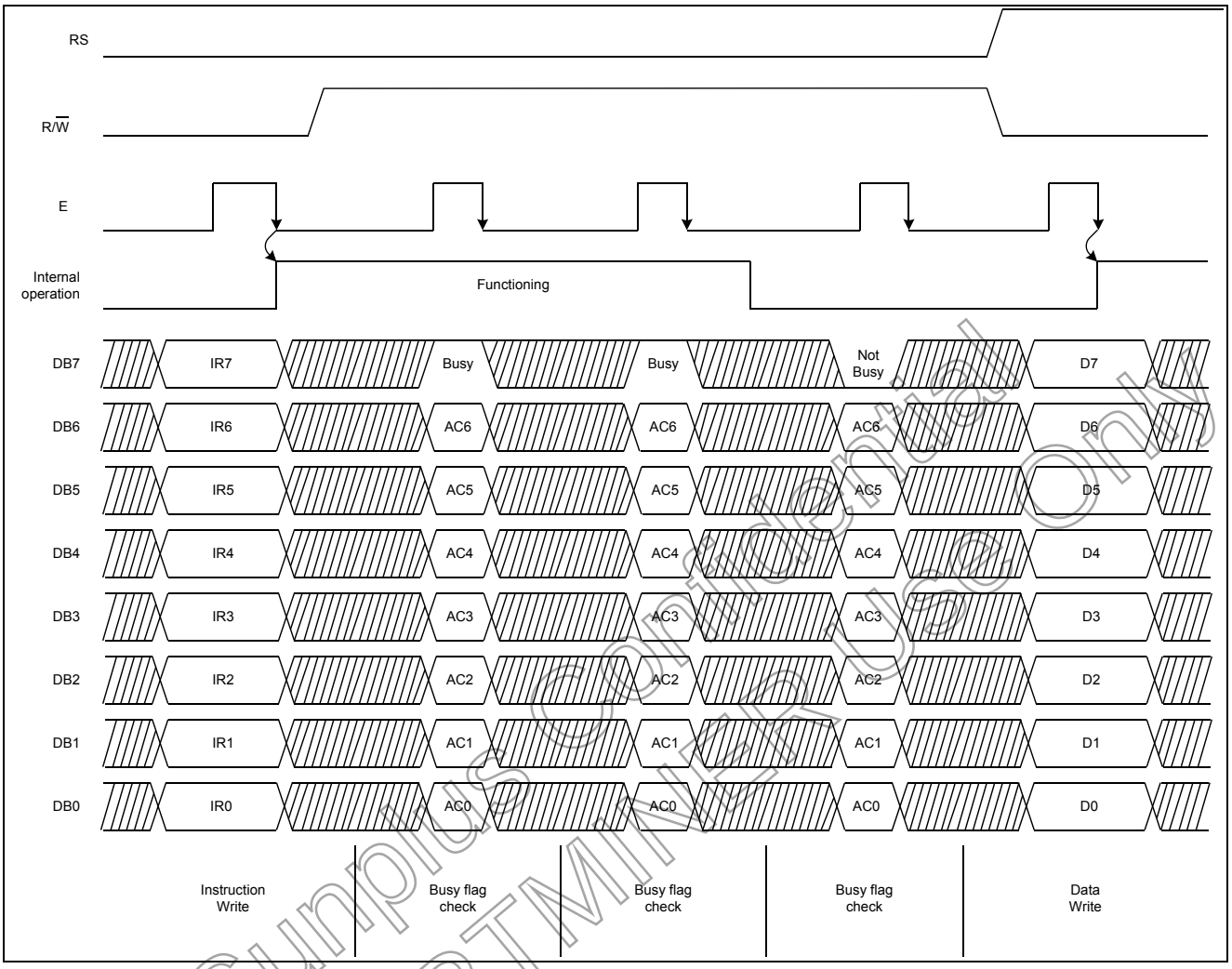


Figure 5-28: Example of 8-bit Data Transfer Timing Sequence

5.15. Supply Voltage for LCD Drive

LCD bias can be selected by open/short V2 and V3 pins.

Duty Factor / Supply Voltage	1/8, 1/11	1/16
	1/4	1/5
V2, V3	Short	Open

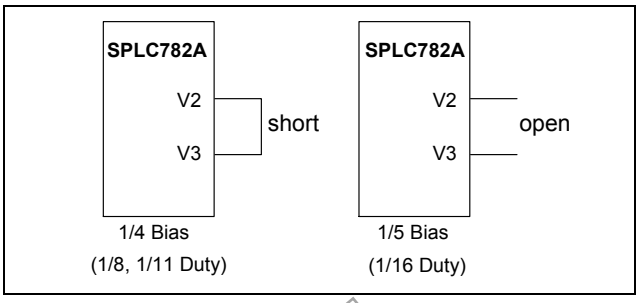


Figure 5-29: Supply Voltage for LCD Drive

5.15.1. The relations between LCD frame's frequency and oscillator's frequency

(Assume the oscillation frequency is 250KHz, 1 clock cycle time = 4.0μs)

5.15.2. 1/8 Duty, type-A waveform

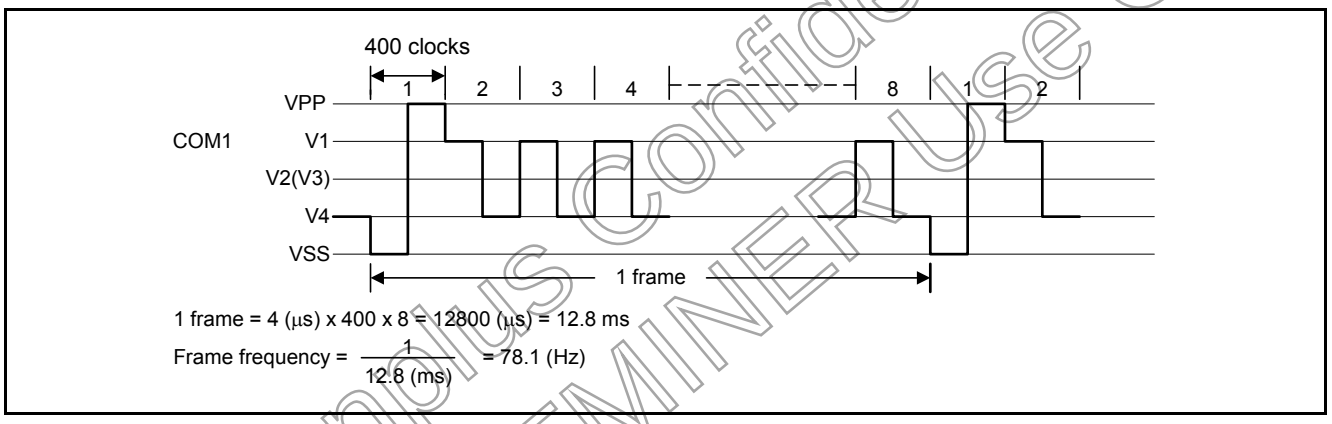


Figure 5-30: 1/8 Duty type-A waveform

5.15.3. 1/11 Duty, type-A waveform

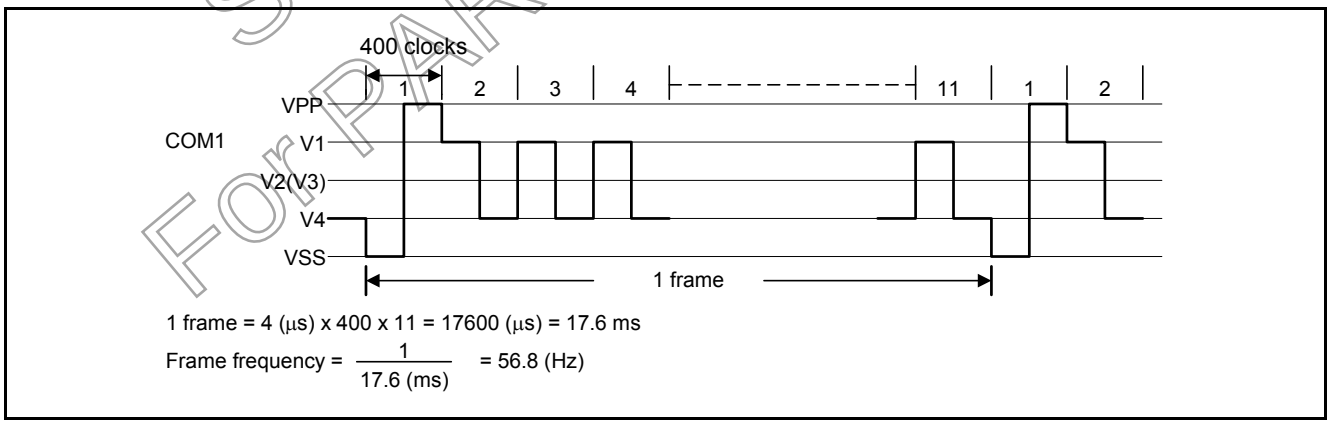
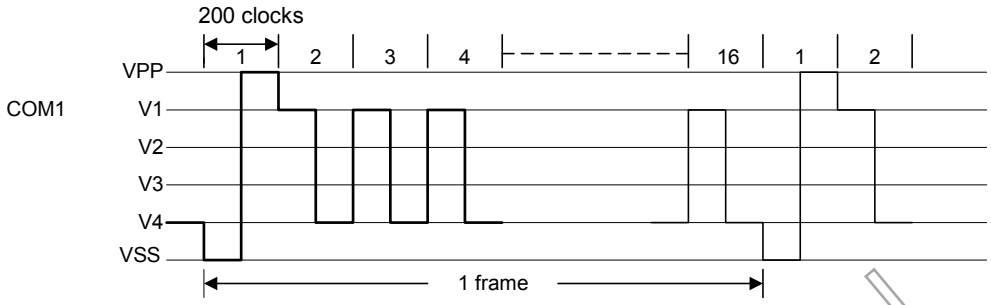


Figure 5-31: 1/11 Duty type-A waveform

5.15.4. 1/16 Duty, type-A waveform

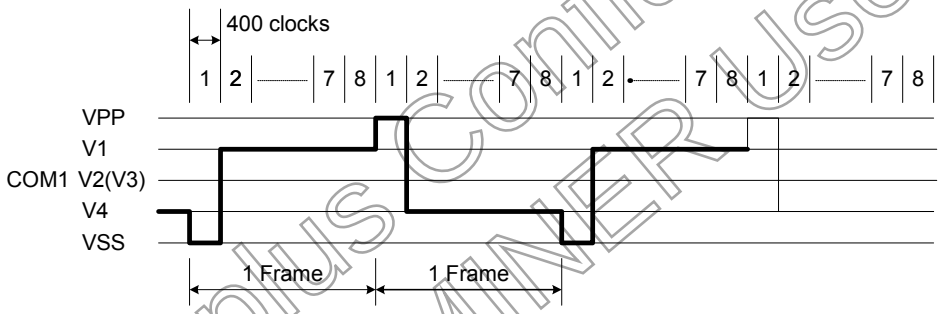


1 frame = 4 (μs) x 200 x 16 = 12800 (μs) = 12.8 ms

Frame frequency = $\frac{1}{12.8\ (ms)}$ = 78.1 (Hz)

Figure 5-32: 1/16 Duty type-A waveform

5.15.5. 1/8 Duty, type-B waveform

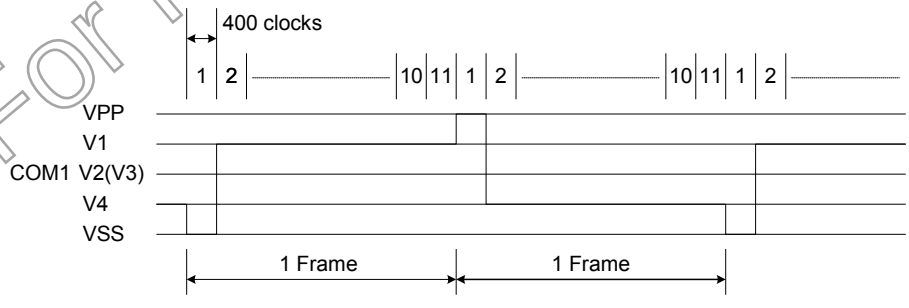


1 frame = 4(μs) x 400 x 8 = 12800(μs) = 12.8ms

Framefrequency = $\frac{1}{12.8(ms)}$ = 78.1(Hz)

Figure 5-33: 1/8 Duty type-B waveform

5.15.6. 1/11 Duty, type-B waveform



1 frame = 4(μs) x 400 x 11 = 17600(μs) = 17.6ms

Framefrequency = $\frac{1}{17.6(ms)}$ = 56.8(Hz)

Figure 5-34: 1/11 Duty type-B waveform

5.15.7. 1/16 Duty, type-B waveform

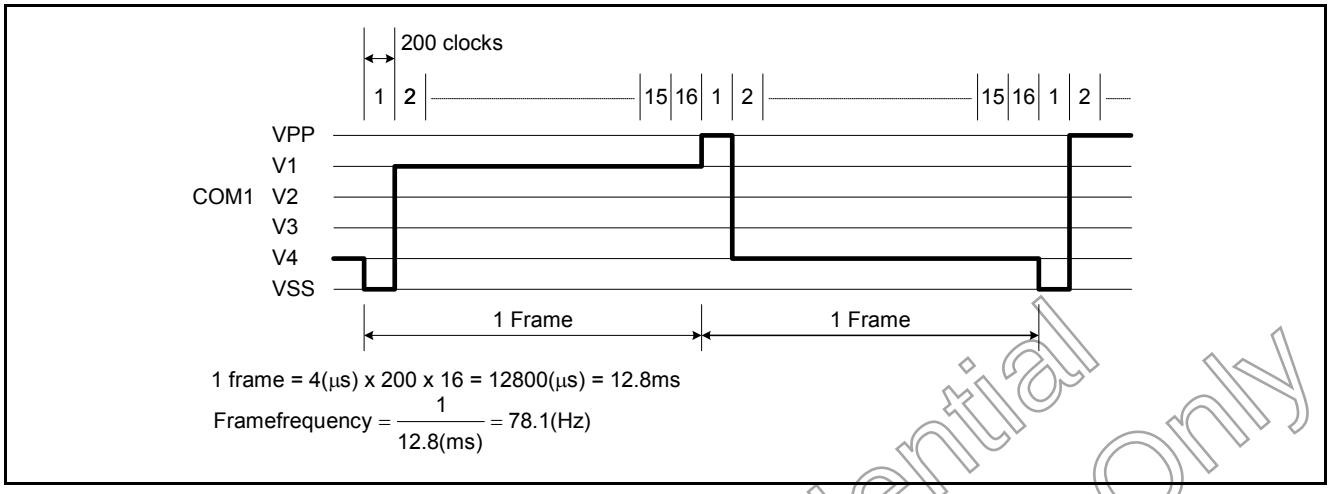


Figure 5-35: 1/16 Duty type-B waveform

5.16. Register --- IR (Instruction Register) and DR (Data Register)

SPLC782A has two 8-bit registers - IR (instruction register) and DR (data register). In the followings, we can use the combinations of the RS pin and the R/W pin to select the IR and DR.

RS	R/W	Operation
0	0	IR write (Display clear, etc.)
0	1	Read busy flag (DB7) and address counter (DB0 - DB6)
1	0	DR write (DR to Display data RAM or Character generator RAM)
1	1	DR read (Display data RAM or Character generator RAM to DR)

5.17. Busy Flag (BF)

When RS = 0 and R/W = 1, the busy flag is output to DB7. As the busy flag = 1, SPLC782A is in busy state and does not accept any instructions until the busy flag = 0.

5.18. Address Counter (AC)

The address counter assigns addresses to display data RAM and character generator RAM. When an instruction for address is written in IR, the address information is sent from IR to AC. After writing into (or reading from)display data RAM or character generator RAM, AC is automatically incremented by +1 (or decremented by -1). AC contents are output to DB0 - DB6 when RS = 0 and R/W = 1.

5.19. Segment Data Direction

SHL is the segment data shift direction control pin.

LCD data is shifted from SEG1 to SEG80 by connecting SHL to VSS, and is reversed by connecting SHL to VDD.

5.20. Common Data Direction

DIRC is the common data shift direction control pin.

LCD common scan sequence from COM1 to COM16 by connecting DIRC to VSS, and is reversed by connecting DIRC to VDD.

5.21. I/O Port Configuration

5.21.1. Input port: E

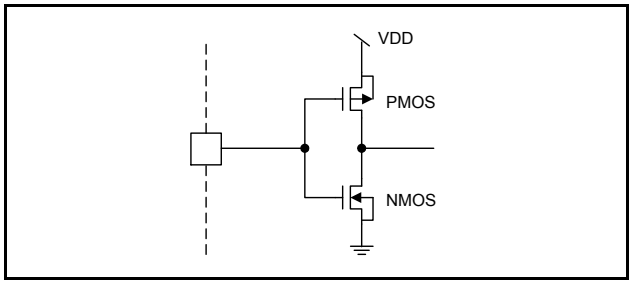


Figure 5-36: Input port: E Configuration

5.21.2. Input port: R/W, RS

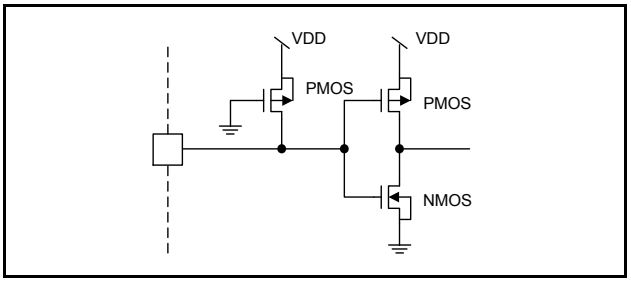


Figure 5-37: Input port: RW, RS Configuration

5.21.3. Output port: CL2, D

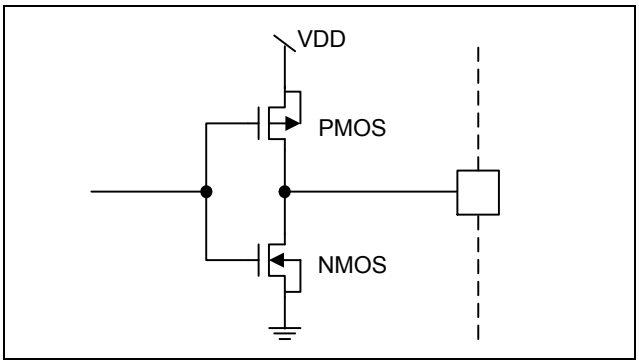


Figure 5-38: Output port: CL2, D Configuration

5.21.4. Input / Output port: DB0 - DB7

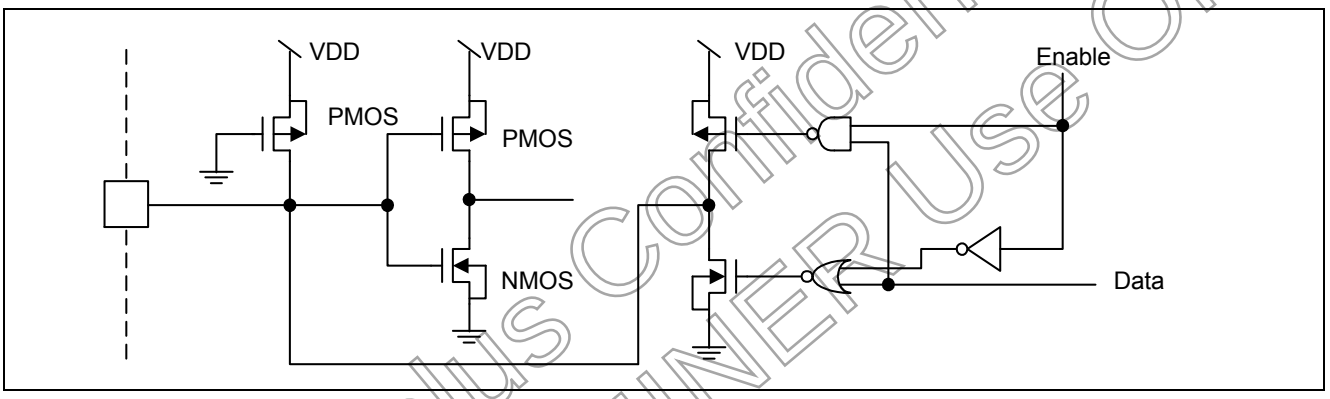


Figure 5-39: Input/Output port: DB0-DB7 Configuration

6. ELECTRICAL SPECIFICATIONS

6.1. Absolute Maximum Ratings

Characteristics	Symbol	Ratings
Operating Voltage	VDD	-0.3V to +7.0V
Driver Supply Voltage	V_{PP}	-0.3V to +7.0V
Input Voltage Range	V_{IN}	-0.3V to VDD +0.3V
Operating Temperature	T_A	-20℃ to +75℃
Storage Temperature	T_{STO}	-55℃ to +125℃

Note: Stresses beyond those given in the Absolute Maximum Rating table may cause operational errors or damage to the device. For normal operational conditions see AC/DC Electrical Characteristics.

6.2. DC Characteristics (VDD = 2.4V to 4.5V, T_A = -20℃ to +75℃)

Characteristics	Symbol	Limit			Unit	Test Condition
		Min.	Typ.	Max.		
Operating Voltage	VDD	2.4	-	4.5	V	
Operating Current	I_{DD1}	-	0.15	0.25	mA	No access from MPU **(Note1)**
	I_{DD2}	-	0.18	0.48	mA	Access operation from MPU (F_{CYC} = 500KHz)**(Note1)**
Input High Voltage	V_{IH1}	0.7VDD	-	VDD	V	Pins:(E, RS, R/W, DB0 - DB7)
Input Low Voltage	V_{IL1}	-0.3	-	0.55	V	
Input High Current	I_{IH}	-	-	2.0	μA	Pins: (RS, R/W, DB0 - DB7)
Input Low Current	I_{IL}	-5.0	-30	-100	μA	
Output High Voltage	V_{OH1}	0.75VDD	-	VDD	V	I_{OH} = - 0.1mA, Pins: DB0 - DB7
Output Low Voltage	V_{OL1}	-	-	0.2VDD	V	I_{OL} = 0.1mA, Pins: DB0 - DB7
Voltage Drop	V_{DCOM}	-	-	1.0	V	I_O = 0.1mA, Pins: COM1 - COM16
	V_{DSEG}	-	-	1.0	V	I_O = 0.1mA, Pins: SEG1 - SEG80
Operating Current	I_{PP}	-	0.35	0.45	mA	V_{PP} = 6.0V **(Note2)**
LCD Voltage	V_{PP}	4.0	-	6.0	V	1/4 bias or 1/5 bias

Note1: Typ. condition VDD = 3.0V @ 25℃, Max. condition VDD = 4.5V @ -20℃

Note2: Typ. condition VPP = 6.0V @ 25℃, Max. condition VPP = 6.0V @ -20℃

6.3. DC Characteristics (VDD = 4.5V to 5.5V, T_A = -20℃ to +75℃)

Characteristics	Symbol	Limit			Unit	Test Condition
		Min.	Typ.	Max.		
Operating Voltage	VDD	4.5	-	5.5	V	
Operating Current	I_{DD1}	-	0.25	0.35	mA	No access from MPU **(Note1)**
	I_{DD2}	-	0.45	0.7	mA	Access operation from MPU (F_{CYC} = 500KHz)**(Note1)**
Input High Voltage	V_{IH1}	0.7VDD	-	VDD	V	Pins:(E, RS, R/W, DB0 - DB7)
Input Low Voltage	V_{IL1}	-0.3	-	0.6	V	
Input High Current	I_{IH}	-	-	2.0	μA	Pins: (RS, R/W, DB0 - DB7)
Input Low Current	I_{IL}	-30	-80	-150	μA	
Output High Voltage (TTL)	V_{OH1}	2.4	-	VDD	V	I_{OH} = - 0.1mA, Pins: DB0 - DB7
Output Low Voltage (TTL)	V_{OL1}	-	-	0.4	V	I_{OL} = 0.1mA, Pins: DB0 - DB7
Voltage Drop	V_{DCOM}	-	-	1.0	V	I_O = 0.1mA, Pins: COM1 - COM16
	V_{DSEG}	-	-	1.0	V	I_O = 0.1mA, Pins: SEG1 - SEG80
Operating Current	I_{PP}	-	0.35	0.45	mA	V_{PP} = 6.0V **(Note2)**
LCD Voltage	V_{PP}	4.0	-	6.0	V	1/4 bias or 1/5 bias

Note1: Typ. condition VDD = 5.0V @ 25℃, Max. condition VDD = 5.5V @ -20℃

Note2: Typ. condition VPP = 6.0V @ 25℃, Max. condition VPP = 6.0V @ -20℃

6.4. AC Characteristics (VDD = 4.5V to 5.5V, T_A = -20℃ to +75℃)

6.4.1. Internal clock operation (T_A = 25℃, the oscillator frequency chart can be reference on Figure 6-3)

Characteristics	Symbol	Limit			Unit
		Min.	Typ.	Max.	
OSC Frequency	F_{OSC1}	190	270	350	KHz

6.4.2. LCD bias resistor (T_A = 25℃)

Characteristics	Symbol	Limit			Unit
		Min.	Typ.	Max.	
Bias Resistor	R1 - R5	3.0	5.0	7.0	K-ohm

6.4.3. Write mode (Writing data from MPU to SPLC782A)

Characteristics	Symbol	Limit			Unit	Test Condition
		Min.	Typ.	Max.		
E Cycle Time	t_C	500	-	-	ns	Pin E
E Pulse Width	t_{PW}	230	-	-	ns	Pin E
E Rise/Fall Time	t_R, t_F	-	-	20	ns	Pin E
Address Setup Time	t_{SP1}	40	-	-	ns	Pins: RS, R/W, E
Address Hold Time	t_{HD1}	10	-	-	ns	Pins: RS, R/W, E
Data Setup Time	t_{SP2}	80	-	-	ns	Pins: DB0 - DB7
Data Hold Time	t_{HD2}	10	-	-	ns	Pins: DB0 - DB7

6.4.4. Read mode (Reading Data from SPLC782A to MPU)

Characteristics	Symbol	Limit			Unit	Test Condition
		Min.	Typ.	Max.		
E Cycle Time	t_C	500	-	-	ns	Pin E
E Pulse Width	t_W	230	-	-	ns	Pin E
E Rise/Fall Time	t_R, t_F	-	-	20	ns	Pin E
Address Setup Time	t_{SP1}	40	-	-	ns	Pins: RS, R/W, E
Address Hold Time	t_{HD1}	10	-	-	ns	Pins: RS, R/W, E
Data Output Delay Time	t_D	-	-	160	ns	Pins: DB0 - DB7
Data hold time	t_{HD2}	5.0	-	-	ns	Pins: DB0 - DB7

6.5. AC Characteristics (VDD = 2.4V to 4.5V, T_A = -20℃ to +75℃)

6.5.1. Internal clock operation (T_A = 25℃, the oscillator frequency chart can be reference on Figure 6-3)

Characteristics	Symbol	Limit			Unit
		Min.	Typ.	Max.	
OSC Frequency	F_{OSC1}	190	270	350	KHz

6.5.2. LCD bias resistor (T_A = 25℃)

Characteristics	Symbol	Limit			Unit
		Min.	Typ.	Max.	
Bias Resistor	R1 - R5	3.0	5.0	7.0	K-ohm

6.5.3. Write mode (Writing data from MPU to SPLC782A)

Characteristics	Symbol	Limit			Unit	Test Condition
		Min.	Typ.	Max.		
E Cycle Time	t_C	1250	-	-	ns	Pin E
E Pulse Width	t_{PW}	600	-	-	ns	Pin E
E Rise/Fall Time	t_R, t_F	-	-	25	ns	Pin E
Address Setup Time	t_{SP1}	60	-	-	ns	Pins: RS, R/W, E
Address Hold Time	t_{HD1}	20	-	-	ns	Pins: RS, R/W, E
Data Setup Time	t_{SP2}	195	-	-	ns	Pins: DB0 - DB7
Data Hold Time	t_{HD2}	10	-	-	ns	Pins: DB0 - DB7

6.5.4. Read mode (Reading data from SPLC782A to MPU)

Characteristics	Symbol	Limit			Unit	Test Condition
		Min.	Typ.	Max.		
E Cycle Time	t_C	1250	-	-	ns	Pin E
E Pulse Width	t_W	600	-	-	ns	Pin E
E Rise/Fall Time	t_R, t_F	-	-	25	ns	Pin E
Address Setup Time	t_{SP1}	60	-	-	ns	Pins: RS, R/W, E
Address Hold Time	t_{HD1}	20	-	-	ns	Pins: RS, R/W, E
Data Output Delay Time	t_D	-	-	360	ns	Pins: DB0 - DB7
Data hold time	t_{HD2}	5.0	-	-	ns	Pin DB0 - DB7

6.6. Write Mode Timing Diagram (Writing Data from MPU to SPLC782A)

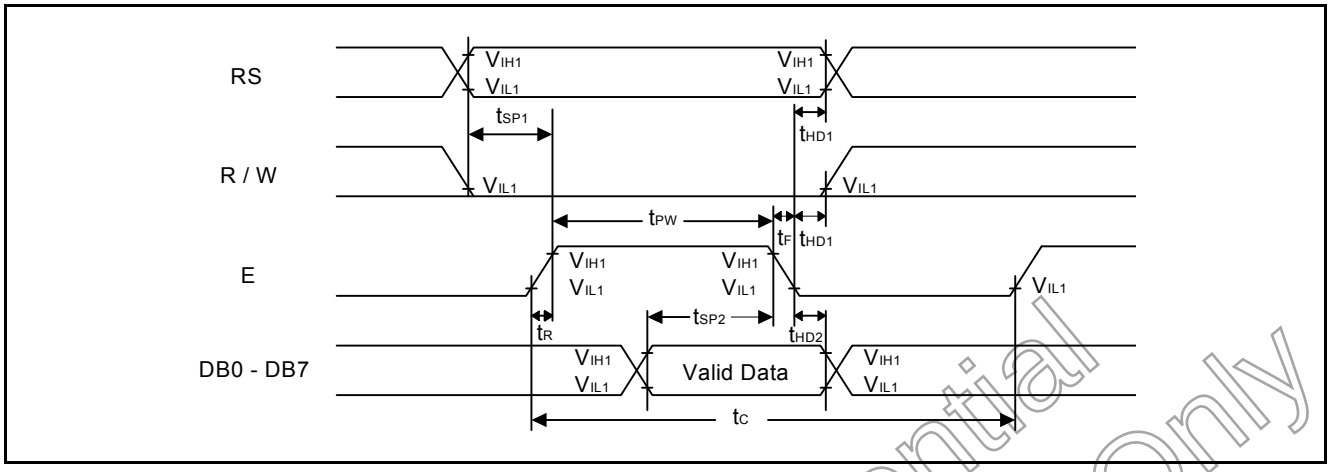


Figure 6-1: Write Mode Timing Diagram

6.7. Read Mode Timing Diagram (Reading Data from SPLC782A to MPU)

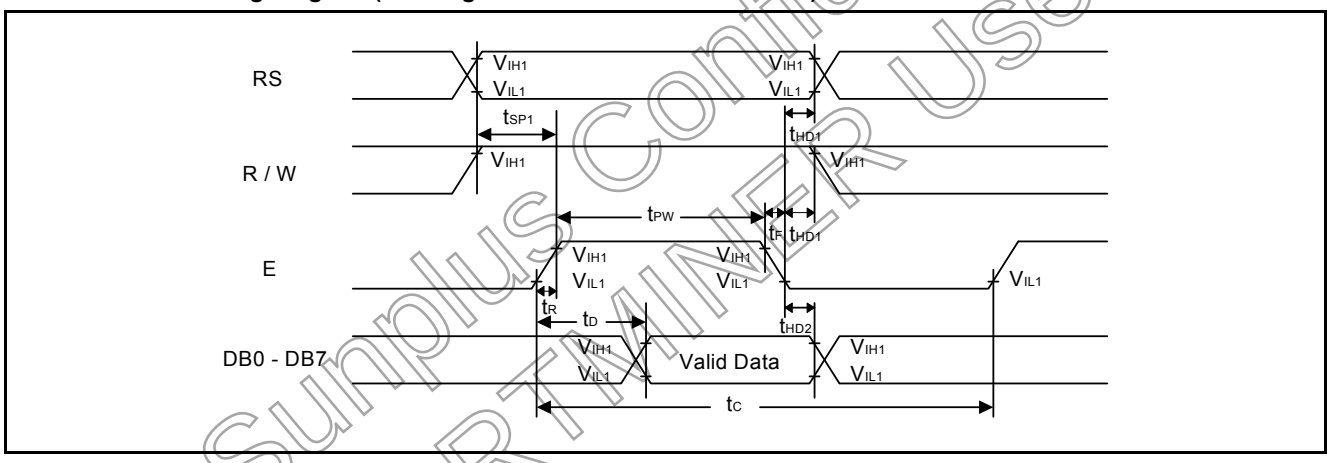
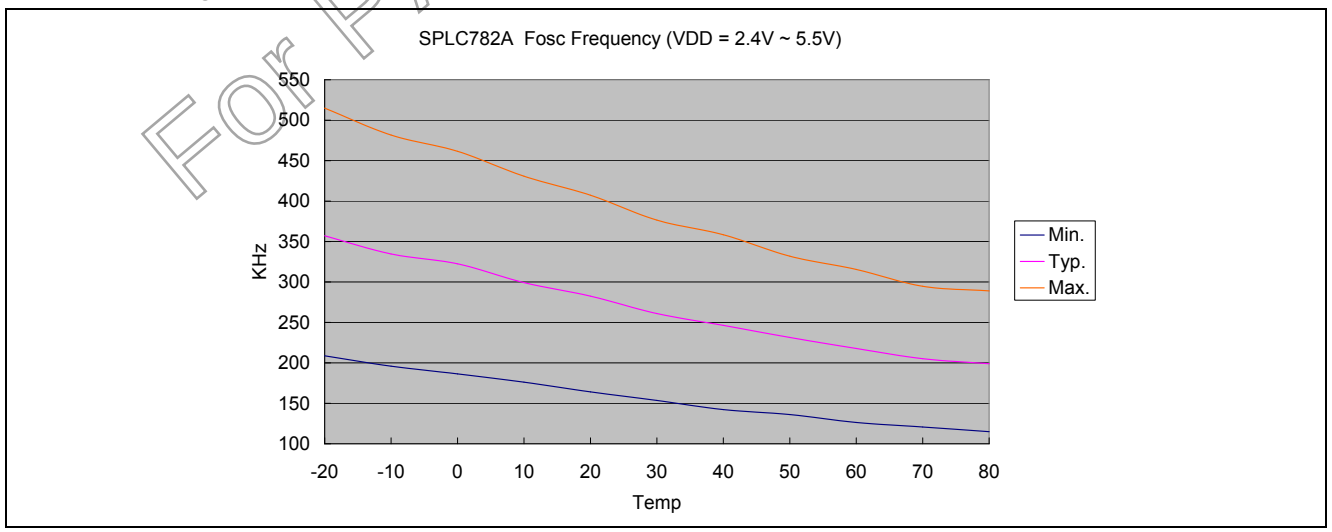


Figure 6-2: Read Mode Timing Diagram

6.8. The Following Graps Show the Relationship Between F_{osc} and Temperature



F_{osc} (Max.) = 515KHz @ VDD = 5.5V, Temp = -20℃
F_{osc} (Min.) = 114KHz @ VDD = 2.4V, Temp = 80℃

Figure 6-3: The Relationship Between Fosc and Temperature

7. APPLICATION CIRCUITS

7.1. Interface to MPU

7.1.1. Interface to 8-bit MPU (6805)

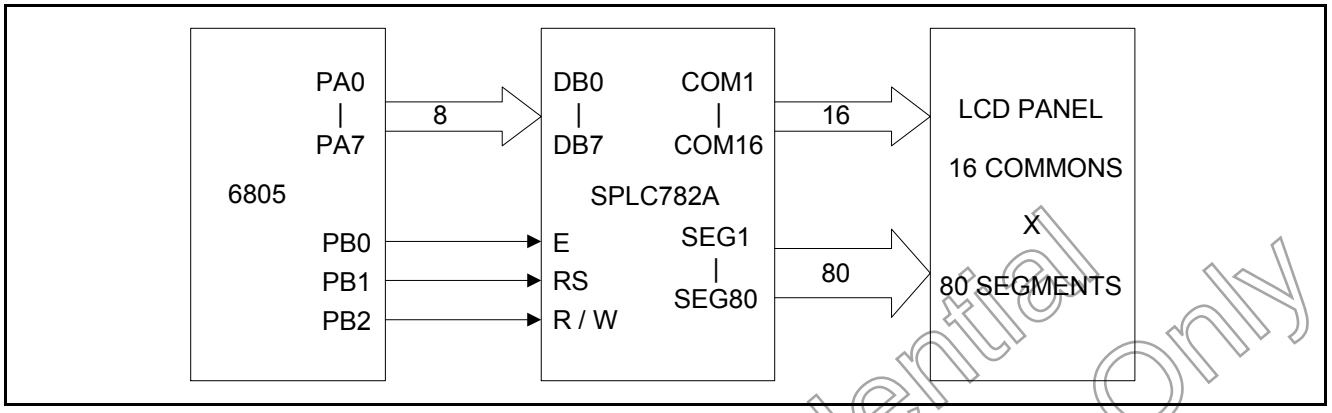


Figure 7-1: Interface to 8-bit MPU (6805)

7.1.2. Interface to 8-bit MPU (Z80)

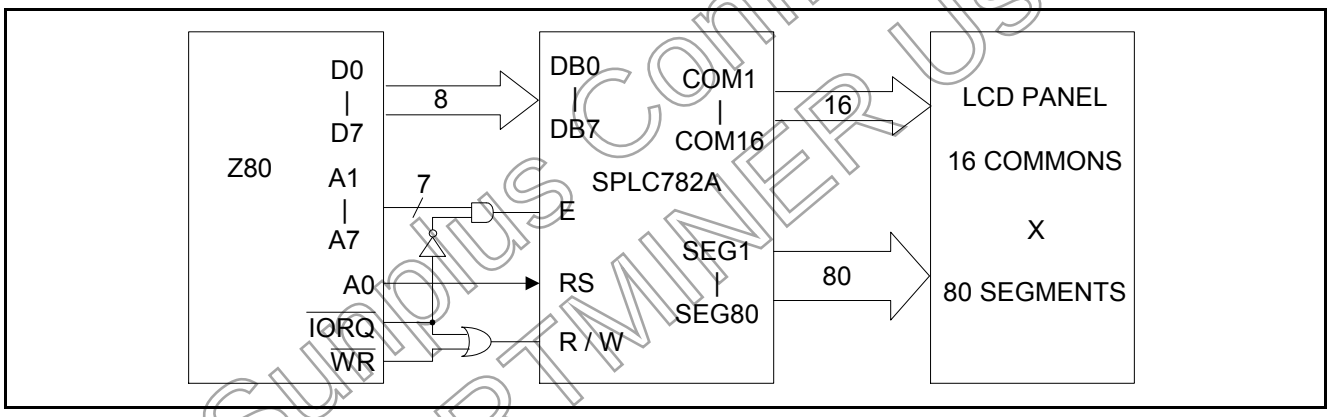


Figure 7-2: Interface to 8-bit MPU (Z80)

7.2. Applications for LCD

7.2.1. Chip bottom & lower view (DIRC = "0", SHL = "0")

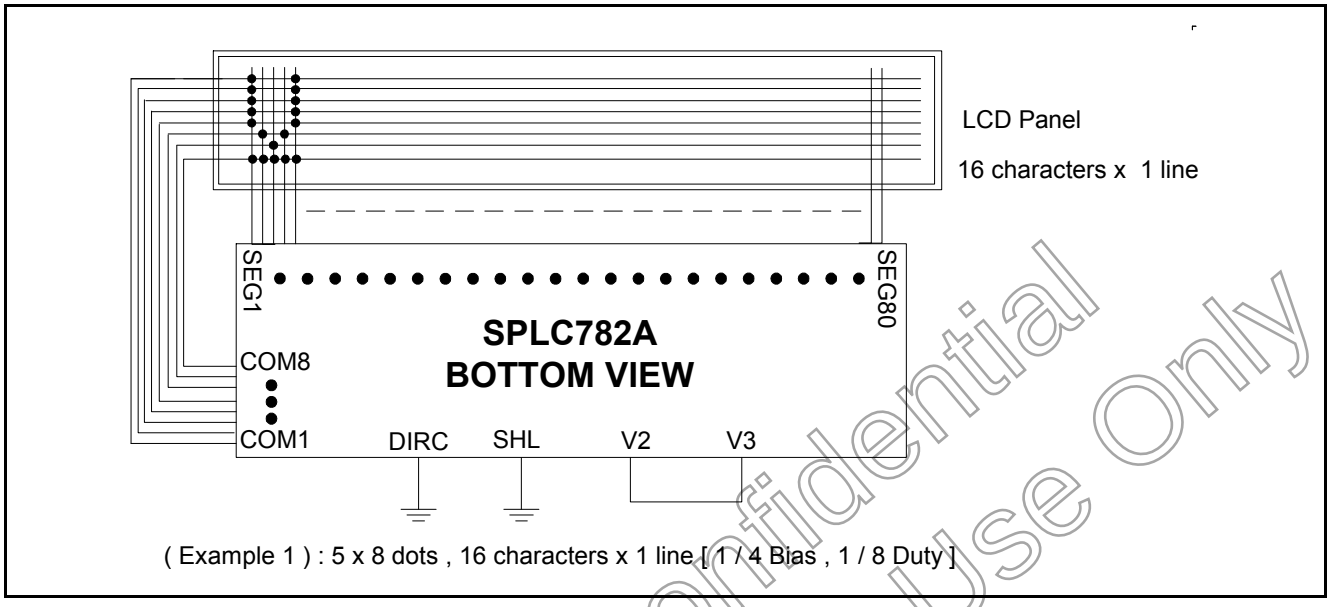


Figure 7-3: Chip Bottom & Lower View (Example 1)

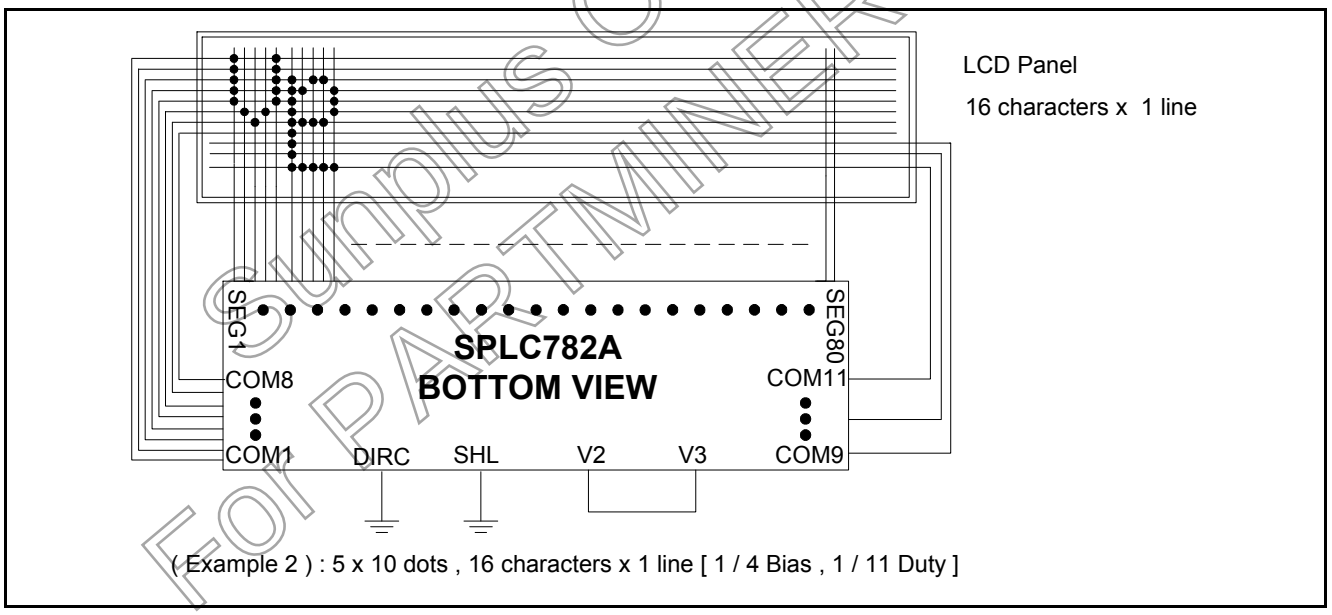


Figure 7-4: Chip Bottom & Lower View (Example 2)]

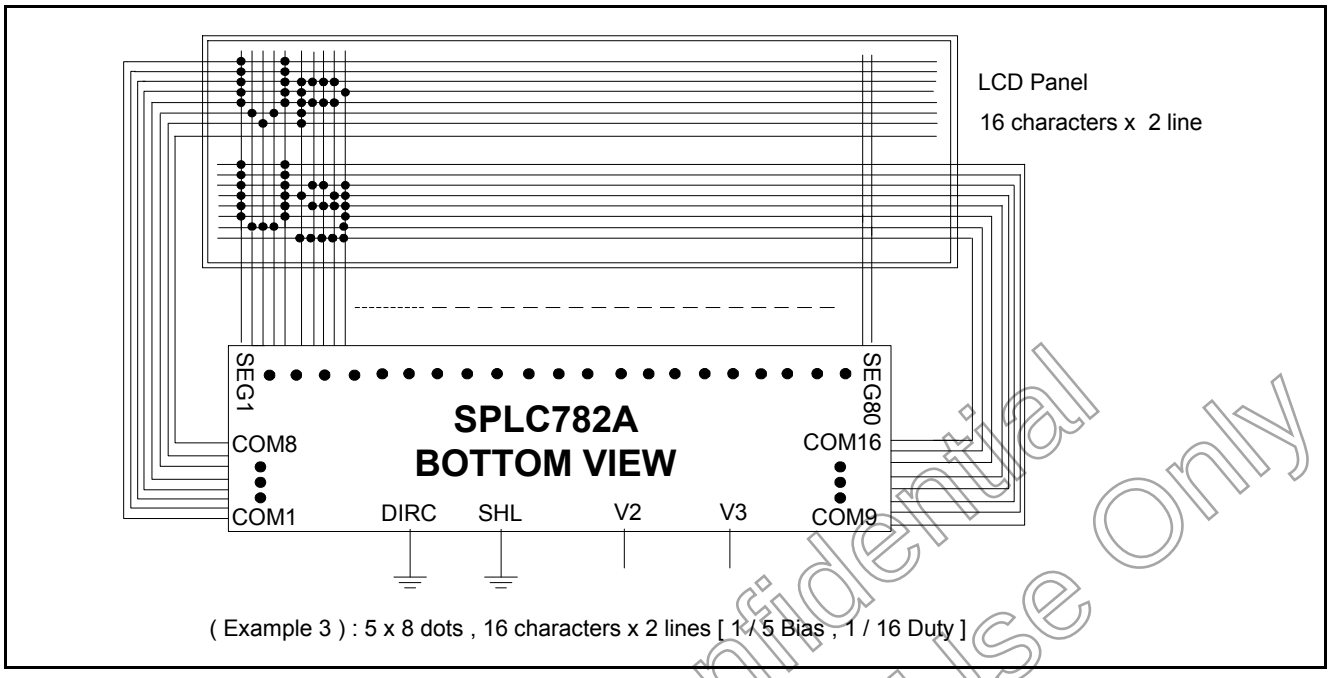


Figure 7-5: Chip Bottom & Lower View (Example 3)

7.2.2. Chip bottom & upper view (DIRC = "1", SHL = "1")

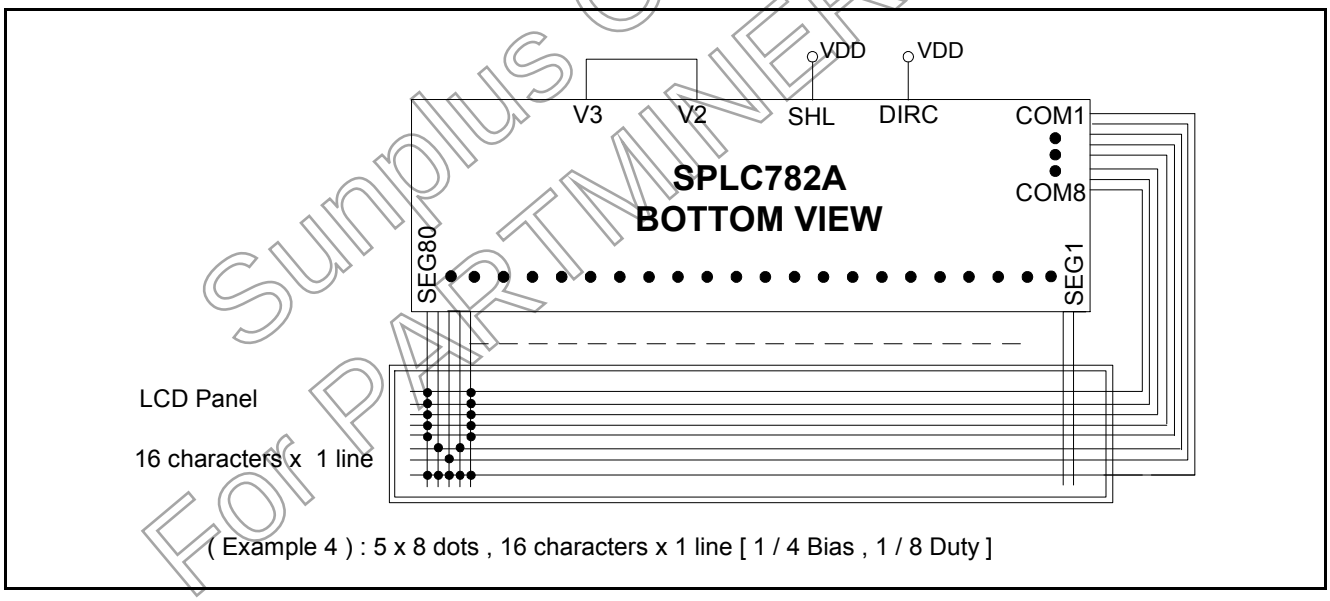


Figure 7-6: Chip Bottom & Upper View (Example 4)

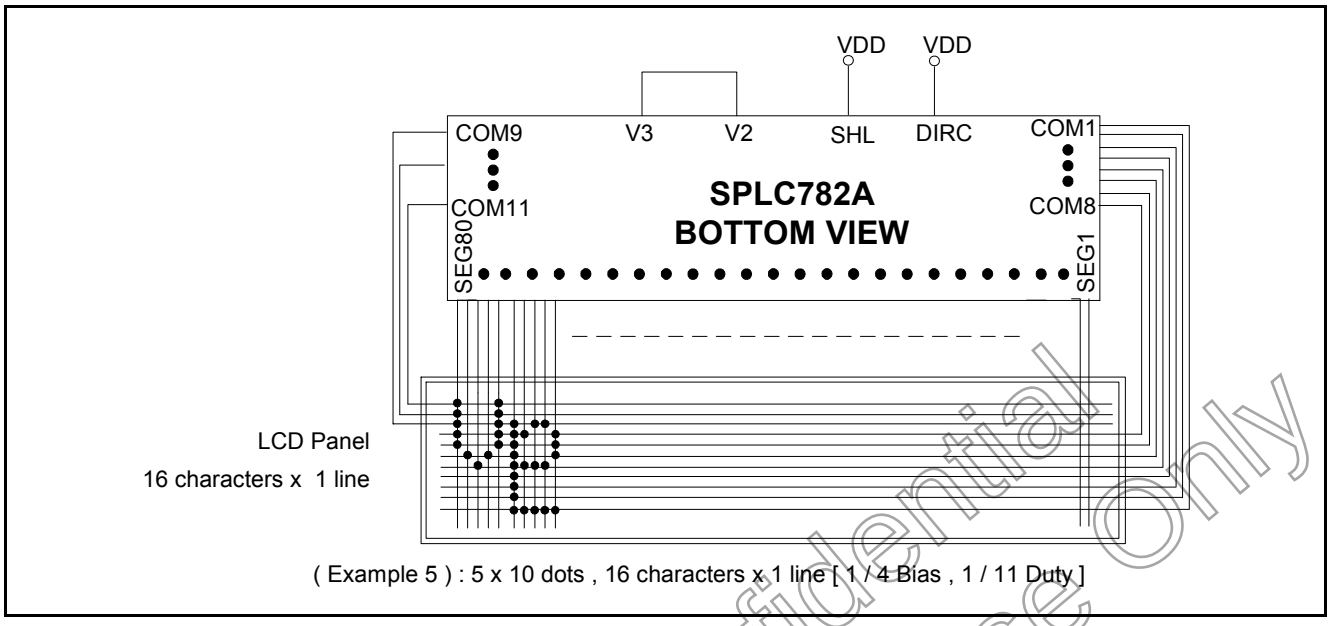


Figure 7-7: Chip Bottom & Upper View (Example 5)

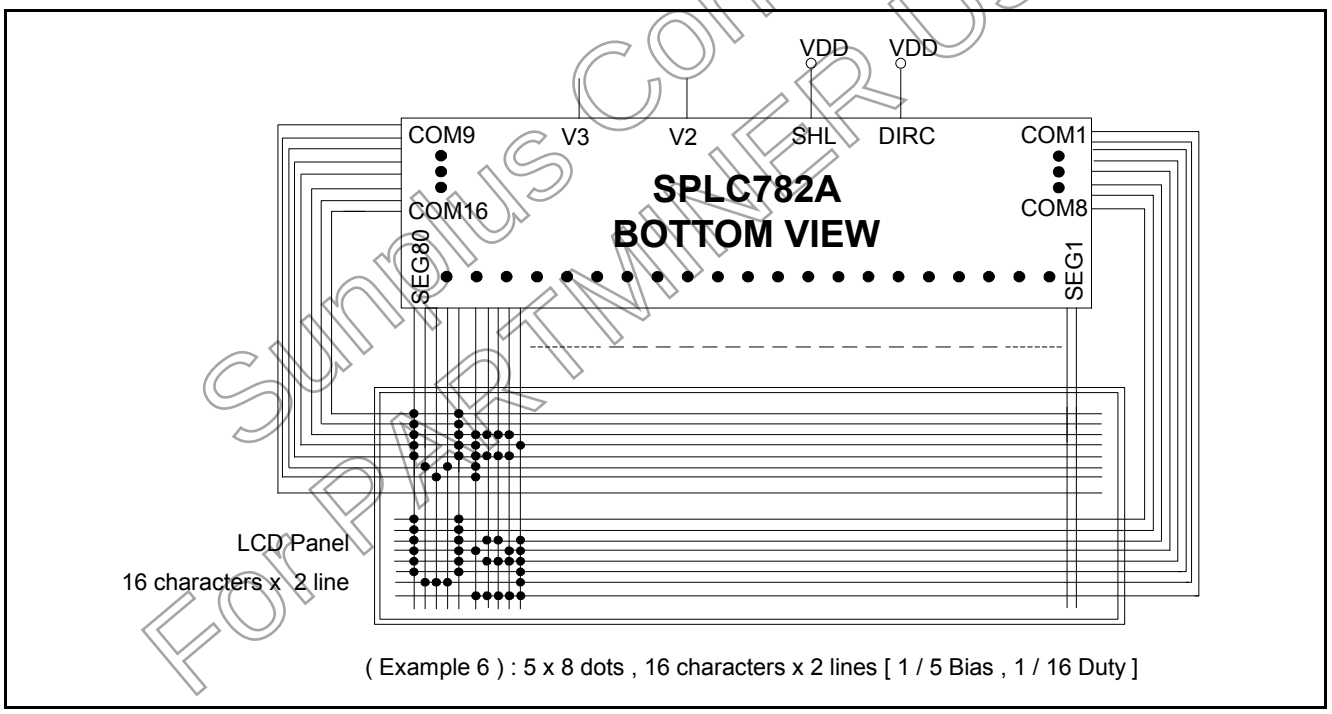


Figure 7-8: Chip Bottom & Upper View (Example 6)

7.2.3. Chip top & lower view (DIRC = "0", SHL = "1")

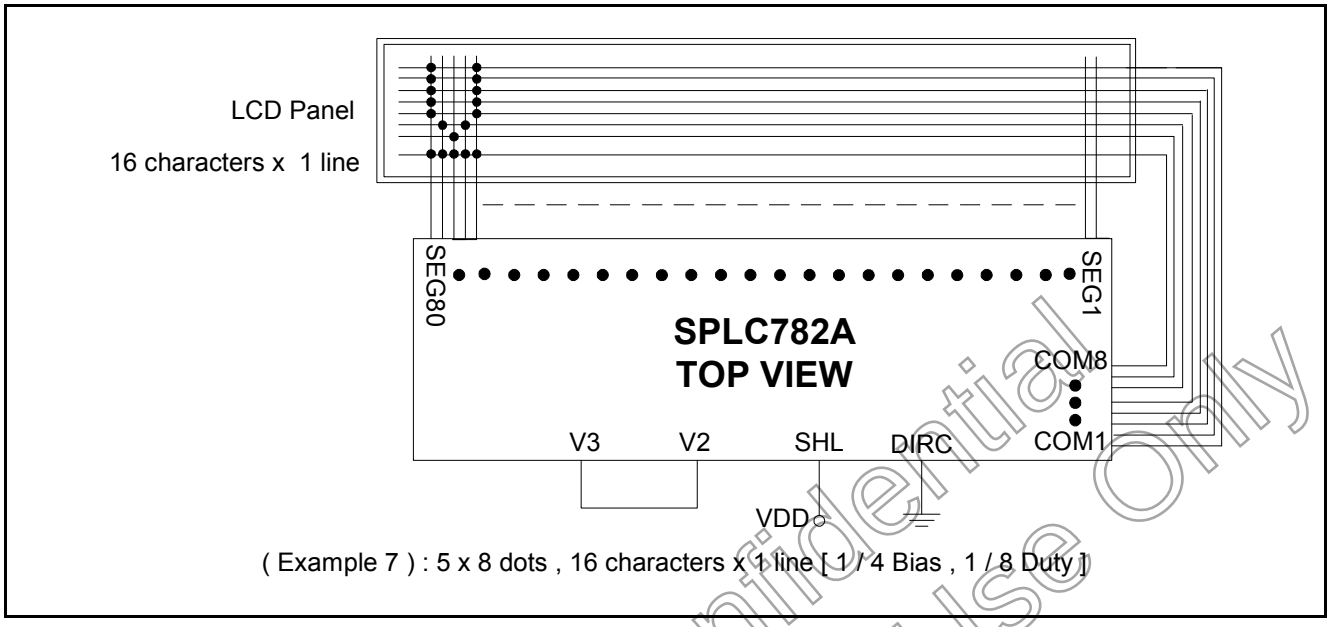


Figure 7-9: Chip Top & Lower View (Example 7)

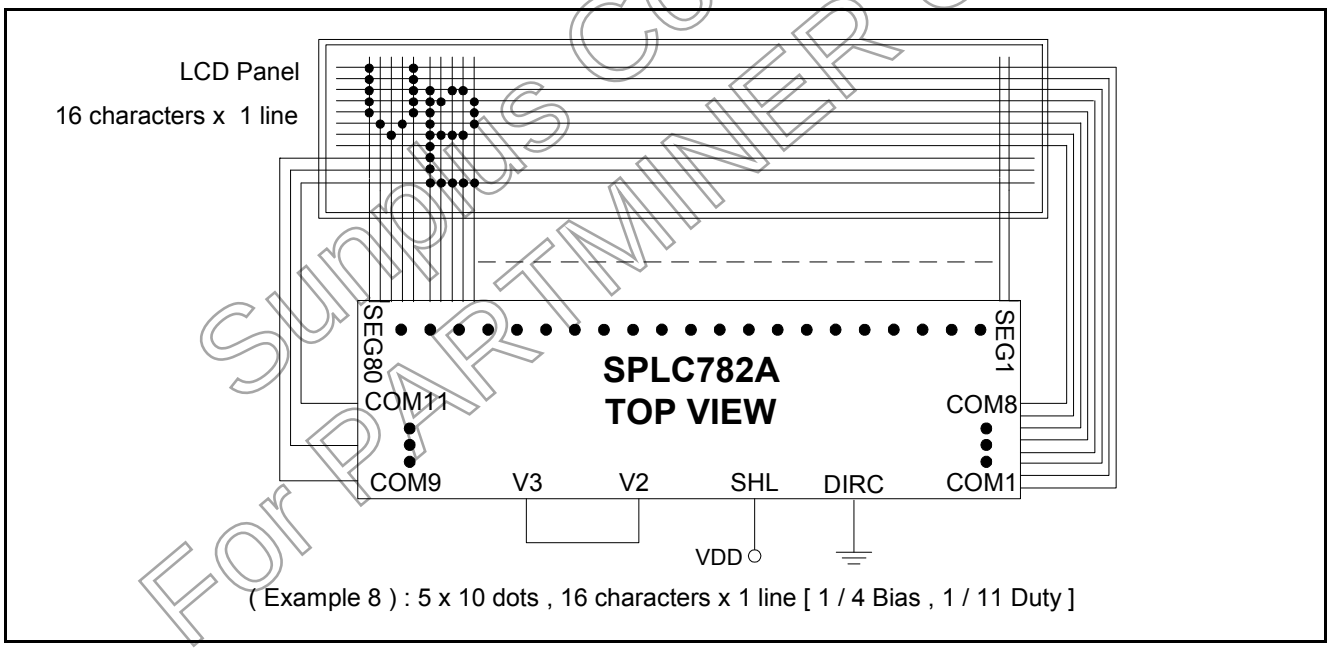


Figure 7-10: Chip Top & Lower View (Example 8)

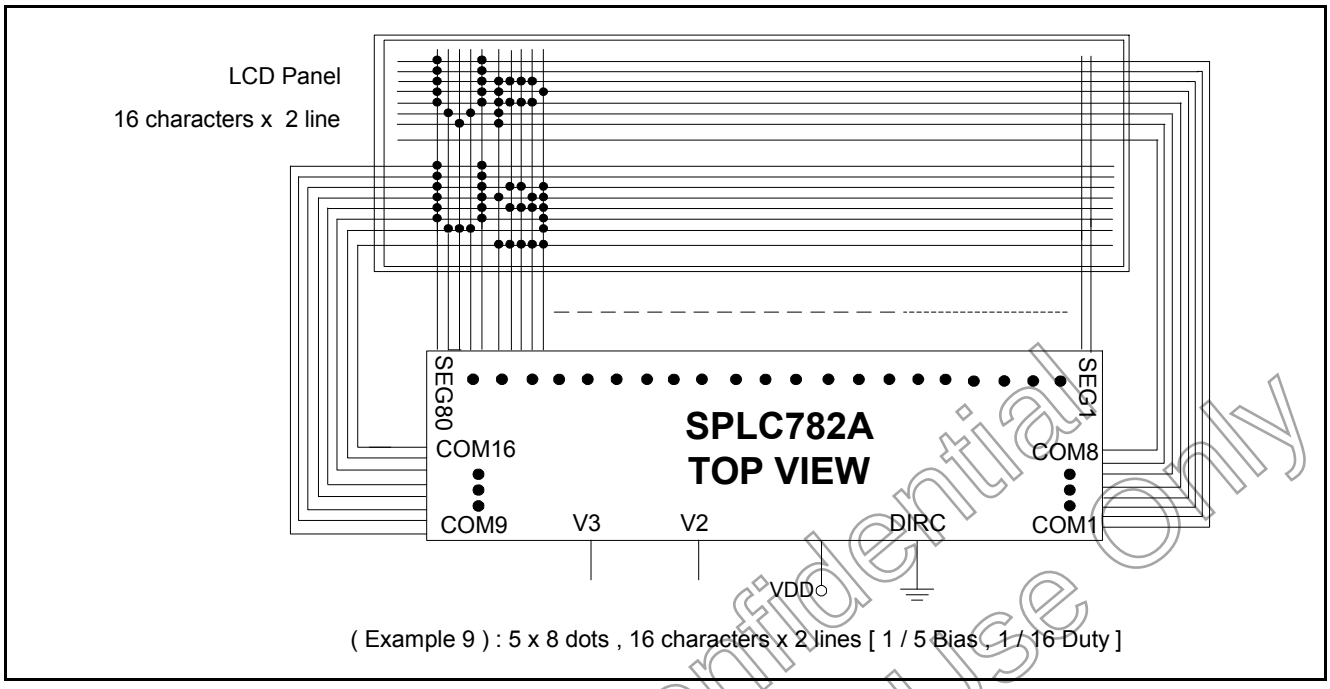


Figure 7-11: Chip Top & Lower View (Example 9)

7.2.4. Chip top & upper view (DIRC = "1", SHL = "0")

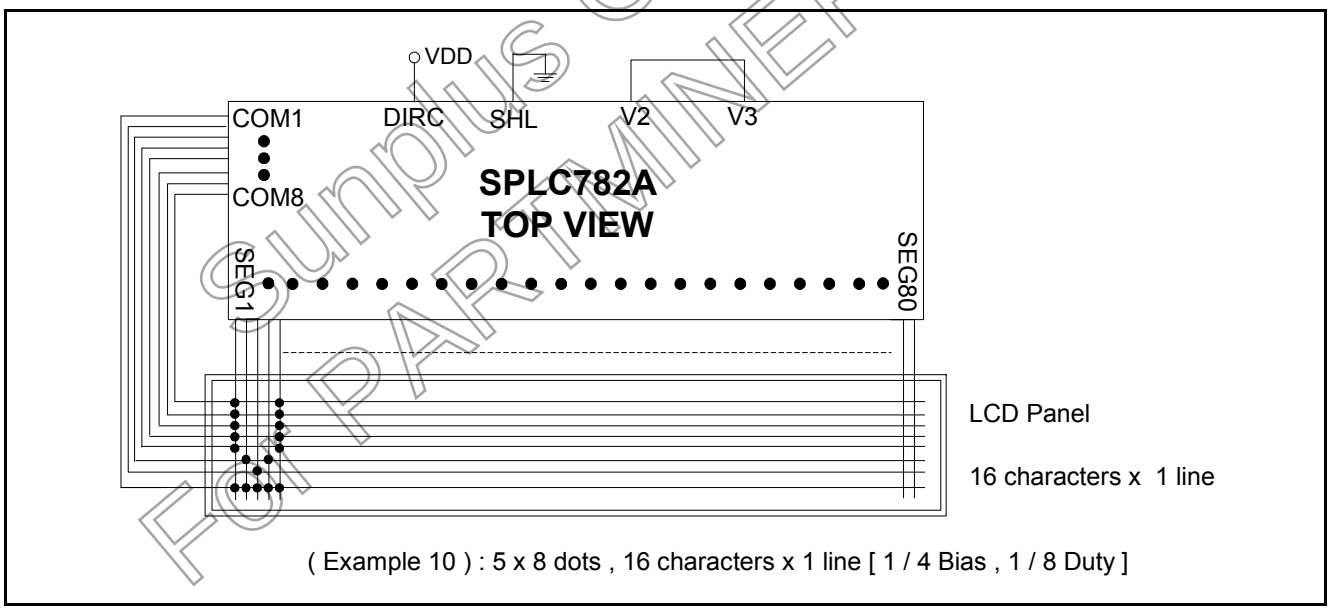


Figure 7-12: Chip Top & Upper View (Example 10)

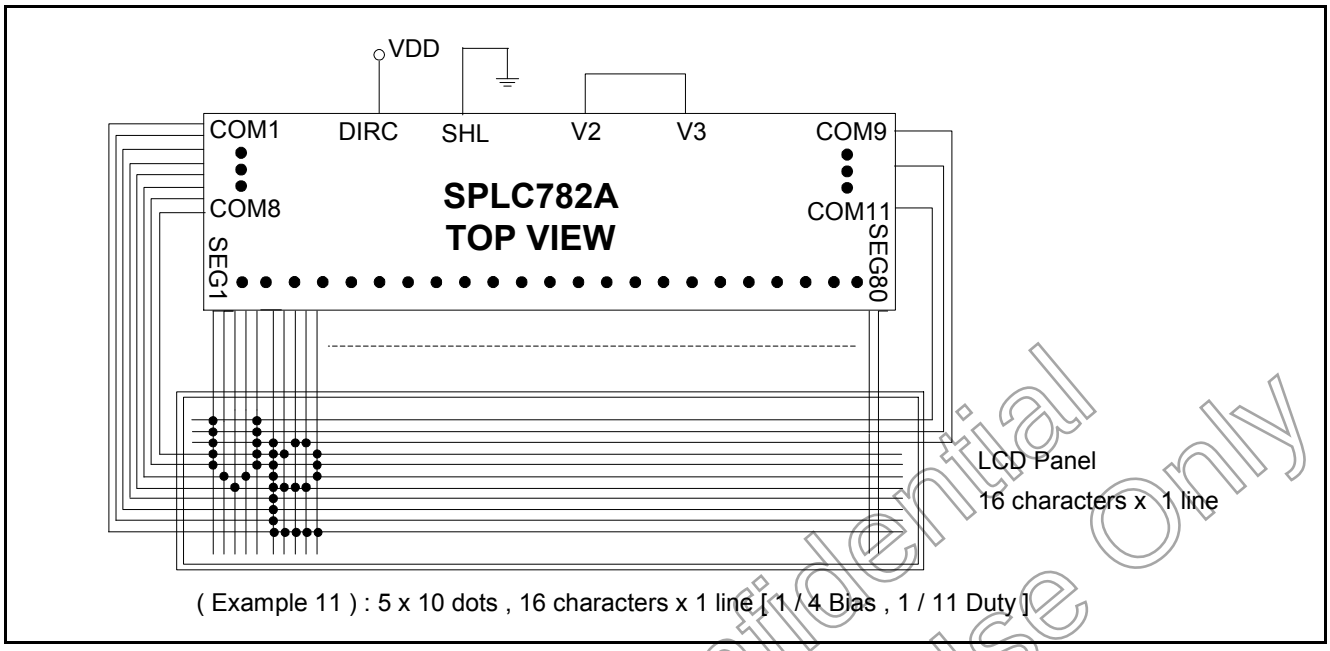


Figure 7-13: Chip Top & Upper View (Example 11)

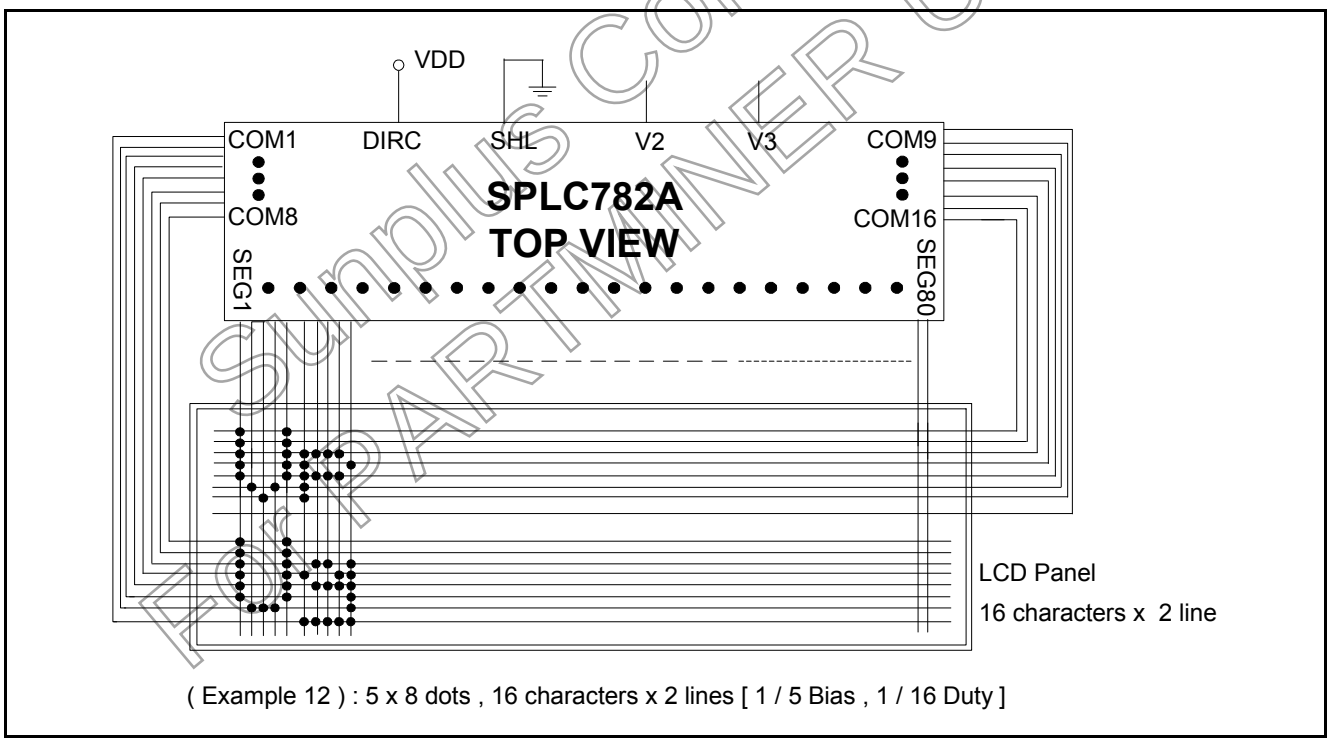


Figure 7-14: Chip Top & Upper View (Example 12)

8. CHARACTER GENERATOR ROM

8.1. SPLC782A - 016

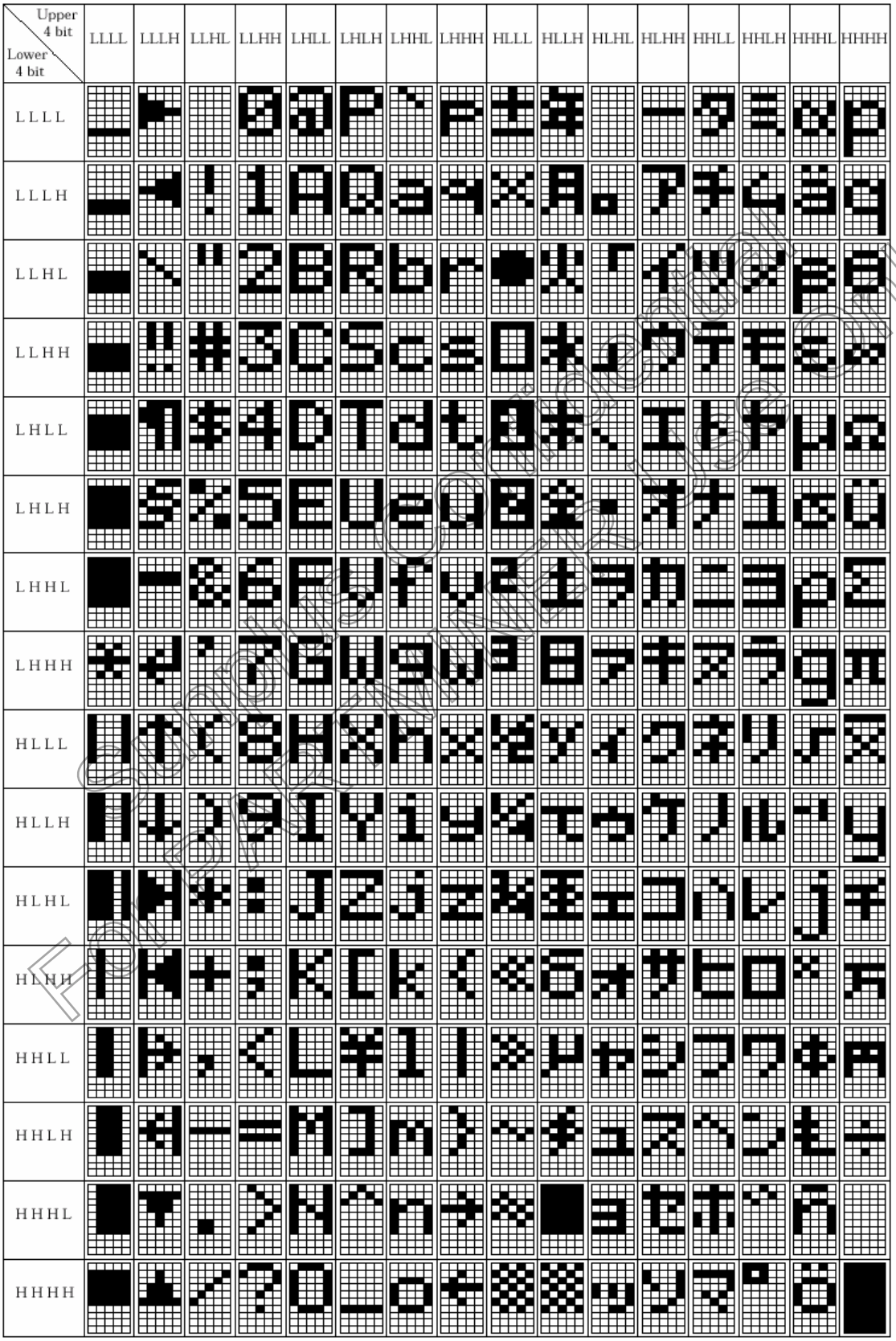


Figure 8-1: CGROM (SPLC782A-016)

8.2. SPLC782A - 022

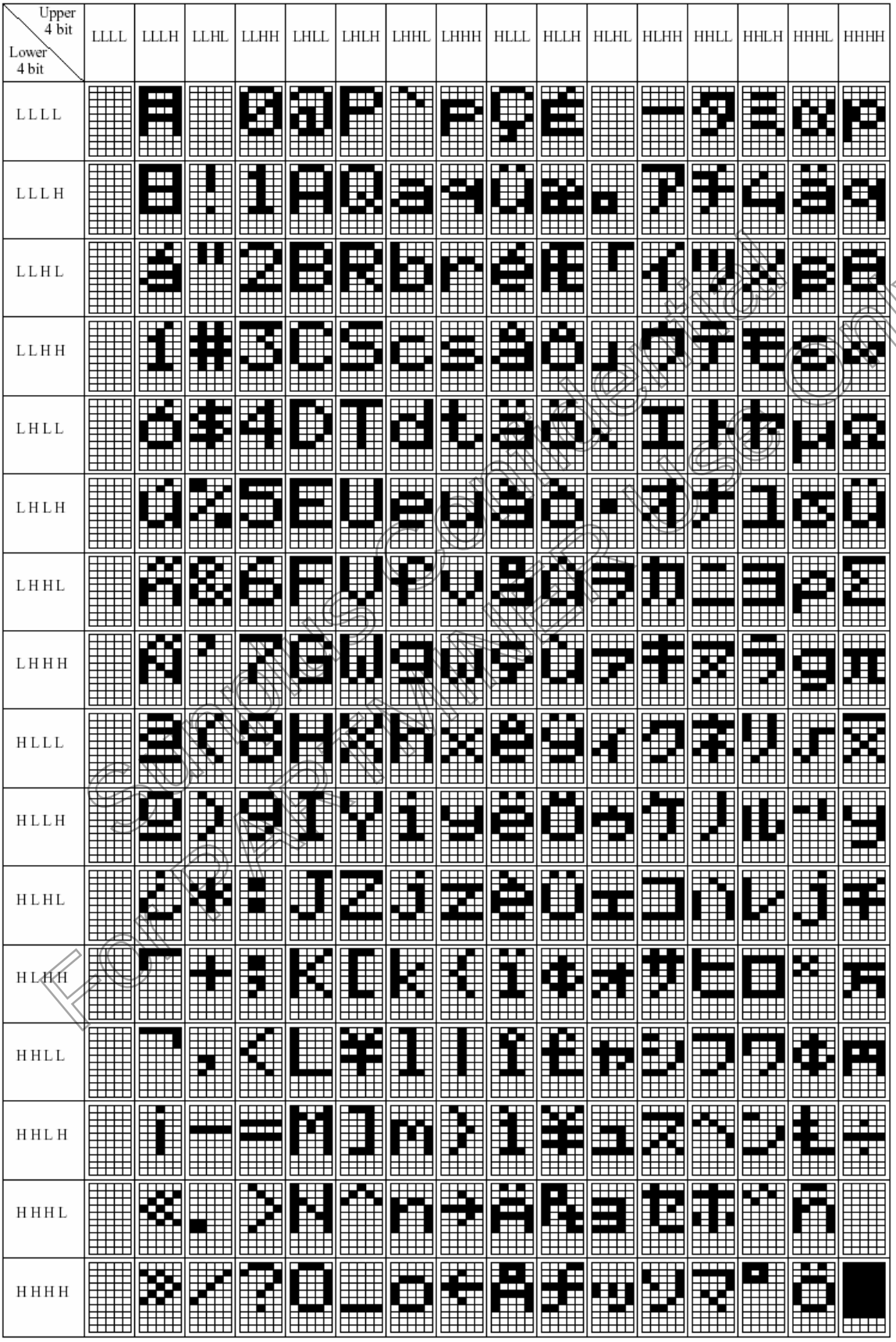


Figure 8-2: CGROM (SPLC782A-022)

9. PACKAGE/PAD LOCATIONS

9.1. PAD Assignment and Locations

Please contact Sunplus sales representatives for more information.

9.2. Ordering Information

Product Number	Package Type
SPLC782A-NnnnV-C	Chip form with gold bump

Note1: Code number is assigned for customer.

Note2: Code number (N = A - Z or 0 - 9, nnn = 000 - 999); version (V = A - Z).

10. DISCLAIMER

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11. REVISION HISTORY

Date	Revision #	Description	Page
FEB. 15, 2005	1.7	1. Modify from TYPE to DIRC in section 5.20 Common data Direction	22
		2. Add description(T_A=25℃) in section 6.5.1 and 6.5.2	26
		3. Correct the description of Figure 5-4	6
		4. Correct the code of 5.2.9 Read busy flag and address	7
		5. Modify the execution time of 5.3 Instruction table	8
		6. Remove the note of Figure 5-16	8
		7. Correct the display of 14~21 of Figure 5-17	9
		8. Insert the display of 10 of Figure 5-19	10
		9. Modify the Driver Supply voltage of 6.1 absolute maximum ratings	24
		10. Modify the operation current of IDD1 and IDD2 of 6.2 DC Characteristics and 6.3 DC Characteristics	24-25
		11. Add the operation current of Ipp of of 6.2 DC Characteristics and 6.3 DC Characteristics	24-25
		12. Add the description of max. and min. of Fosc of Figure 6-3	27
DEC. 24, 2004	1.6	1. Add figure number for all figure	
		2. Modify 6.2 IIL max. Value to -100uA	24
		3. Modify 6.3 IIL max. Value to -150uA	24
		4. Modify 6.3 VIH1 min. Value to 0.7VDD	24
		5. Modify TA of all DC/AC Characteristics to TA=-20℃ to +75℃	24 - 26
		6. Modify 6.5.3 and 6.5.4 E Cycle time to 1250ns	26
		7. Modify 6.5.3 and 6.5.4 E Pulse Width to 600ns	26
APR. 23, 2004	1.5	1. Modify description: “Execution time” to “Execution time (Temp = 25℃)”	8
		2. Modify Note2: from 2.3ms to 4.1ms	8
APR. 01, 2004	1.4	1. Add min. and max. value in Instruction Table	8
		2. Add 8-bit/4-bit data transfer timing sequence example	18 - 19
		3. Add “6.8 The Following Graps Show the Relationship Between FOSC and Temperature”	27
		4. Add Note2 in Instruction Table	8
JUN. 20, 2003	1.3	1. Add “*8.3 SPLC782A - 22*”	33
		2. Remove “*9. PACKAGE/PAD LOCATIONS*”	34
MAY. 09, 2002	1.2	1. Correct PIN No. error V2 pin: 21 to 22 V3 pin: 22 to 21 R/W pin: 25 to 26 RS pin: 26 to 25 MOD1 pin: 17 to 18 MOD0 pin: 18 to 17	5
		2. Correct ROM size: 160 5*8 dot -> 192 5*8 dot character patterns 32 5*10 dot -> 64 5*10 dot character patterns	13
NOV. 26, 2001	1.1	1. Modify “MODE1“ to “MOD1“, “MODE2“ to “MOD0“ in the “*4. SIGNAL DESCRIPTIONS*”	5
		2. Modify pins “CL2” and “D“ description: “normal mode” to “normally use” in the “*4. SIGNAL DESCRIPTIONS*”	5
		3. Modify pin OSC1 description in the “*4. SIGNAL DESCRIPTIONS*”	5
		4. Modify DC Characteristics in the “*6. ELECTRICAL SPECIFICATIONS*”	21

Date	Revision #	Description	Page
JUL. 27, 2001	1.0	1. Delete "*PRELIMINARY*" 2. Add "with gold bump" in the "*9.3 Ordering Information*" 3. Renew to a new document format	33
MAY. 04, 2001	0.1	Original	