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PUMA 68S2000X - 012/015/017/020

Issue 5.1 August 1999

64K x 32 Static RAM

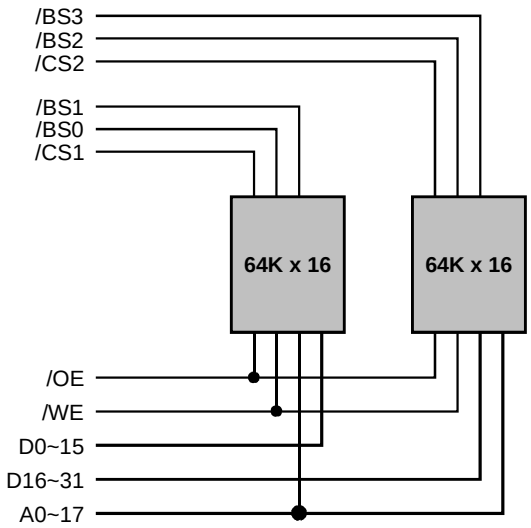
Description

The PUMA68 range of devices provide a high density surface mount industry standard memory solution which may accommodate various memory technologies including SRAM, EEPROM and Flash. The devices are designed to offer a defined upgrade path and may be user configured as 16 or 32 bits wide.

The PUMA68S2000X is a 64Kx32 SRAM module housed in a 68 Jleaded package which complies with the JEDEC 68 PLCC standard. Access times of 12, 15, 17 and 20ns are available. The 5V device is available to commercial and industrial temperature grade.

128Kx32 and 256Kx32 and 512Kx32 SRAM PUMA68 devices are available in the same footprint to offer a defined upgrade path.

Block Diagram



Features

- Access times of 12, 15, 17 or 20ns.
- 5V ± 10%.
- Commercial and Industrial temperature grades
- 68 J Lead Suface Mount Package.
- JEDEC standard footprint.
- User Configurable as 8 / 16 / 32 bits wide
- Operating Power (32 Bit) 2.31W (max)
- Low power standby. (TTL) 330mW (max)
  (CMOS) 83mW (max)

Pin Definition

See page 2.

Pin Functions

Description	Signal
Address Input	A0~A15
Data Input/Output	D0~D31
Chip Select	/CS1~2
Byte Select	/BS0~3
Write Enable	/WE
Output Enable	/OE
No Connect	NC
Power	V_{CC}
Ground	V_{SS}

Package Details

PUMA 68 - Plastic 68 'J' Leaded Package
Max. Dimensions - 0.988" x 0.988" x 0.200"

11403 West Bernardo Court, Suite 100, San Diego, CA92127.
TEL (858) 674 2233, Fax No. (858) 674 2230 E-mail: sales@mosaicsemi.com

Pin Definition - PUMA68S2000X

Pin	Signal	Pin	Signal
1	V_{CC}	35	V_{CC}
2	/CS2	36	A13
3	/BS0	37	A12
4	/BS1	38	A11
5	/BS2	39	A10
6	/BS3	40	A9
7	NC	41	A8
8	NC	42	A7
9	D16	43	D0
10	D17	44	D1
11	D18	45	D2
12	D19	46	D3
13	V_{SS}	47	V_{SS}
14	D20	48	D4
15	D21	49	D5
16	D22	50	D6
17	D23	51	D7
18	V_{CC}	52	V_{CC}
19	D24	53	D8
20	D25	54	D9
21	D26	55	D10
22	D27	56	D11
23	V_{SS}	57	V_{SS}
24	D28	58	D12
25	D29	59	D13
26	D30	60	D14
27	D31	61	D15
28	A6	62	A14
29	A5	63	A15
30	A4	64	NC
31	A3	65	/WE
32	A2	66	/OE
33	A1	67	/CS1
34	A0	68	NC

Absolute Maximum Ratings(1)

Parameter	Symbol	Min		Max	Unit
Voltage on any pin relative to V_{SS}	V_T(2)	-0.3	to	+7.0	V
Power Dissipation	P_T		2.0		W
Storage Temperature	T_{STG}	-55	to	+125	^OC

Notes : (1) Stresses above those listed may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability
(2) V_T can be -2.0V pulse of less than 10ns

Recommended Operating Conditions

Parameter	Symbol	Min	Typ	Max	Unit
Supply Voltage	V_{CC}	4.5	5.0	5.5	V
Input High Voltage	V_{IH}	2.2	-	V_{CC}+0.3	V
Input Low Voltage	V_{IL}	-0.3	-	0.8	V
Operating Temperature (Commercial)	T_A	0	-	70	^OC
(Industrial)	T_{AI}	-40	-	85	^OC

DC Electrical Characteristics

(V_{CC}=5V±10%, T_A=0^{O}C to +70^{O}C)

Parameter		Symbol	Test Condition	Min	Typ	Max	Unit
Input Leakage Current	Address, /OE,/WE	I_{LI}	$0V \le V_{IN} \le V_{CC}$	-4	-	4	µA
Output Leakage Current		I_{LO}	/CS1~2=V_{IH}, $V_{I/O}$=GND to V_{CC}	-4	-	4	µA
Operating Supply Current(2)	32 Bit	I_{CC1}	Min. Cycle, /CS1~2=V_{IL},$V_{IL} \le V_{IN} \le V_{CC}$-2.1V,/BS0~3=$V_{IL}$	-	-	420	mA
	16 Bit	I_{CC2}	Min. Cycle, ,/BS0~3=V_{IL},$V_{IL} \le V_{IN} \le V_{CC}$-2.1V,/CS1=$V_{IL}$ or ,/CS2=V_{IL}	-	-	260	mA
Standby Supply Current	TTL	I_{SB1}	/CS1~2=V_{IH}	-	-	60	mA
	CMOS	I_{SB2}	/CS1~2≥V_{CC}-0.2V, 0.2V ≤V_{IN}≤V_{CC}-0.2V	-	-	15	mA
Output Voltage Low		V_{OL}	I_{OL}=8.0mA	-	-	0.4	V
Output Voltage High		V_{OH}	I_{OH}=-4.0mA	2.4	-	-	V

Notes : Typical Values are at V_{CC}=5.0V, T_A=25^{O}C and specified loading.

Capacitance

(V_{CC} = 5.0V±10%, T_A = 25°C)

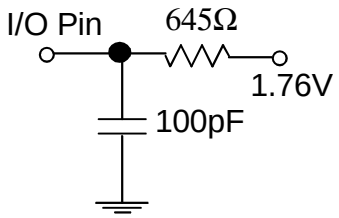
Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Input Capacitance, (Address, /OE, /WE)	C_{IN1}	V_{IN}=0V	-	-	20	pF
I/P Capacitance, (other)	C_{IN2}	V_{IN}=0V			10	
I/O Capacitance, (16 bit mode - worst case)	$C_{I/O}$	$V_{I/O}$=0V	-	-	24	pF

Note : These Parameters are calculated not measured.

Test Conditions

- Input pulse levels : 0V to 3.0V
- Input rise and fall times : 3ns
- Input and Output timing reference levels : 1.5V
- Output Load : See Load Diagram.
- V_{CC} = 5V±10%

Output Load



Operation Truth Table

/CS1	/CS2	/BS0	/BS1	/BS2	/BS3	/OE	/WE	Supply Current	Mode
L	L	L	H	H	H	X	L	I_{CC1}	Write D0~D7
L	L	H	L	H	H	X	L	I_{CC1}	Write D8~D15
L	L	H	H	L	H	X	L	I_{CC1}	Write D16~D23
L	L	H	H	H	L	X	L	I_{CC1}	Write D24~D31
L	L	L	L	H	H	X	L	I_{CC1}	Write D0~D15
L	L	H	H	L	L	X	L	I_{CC1}	Write D16~D31
L	L	L	L	L	L	X	L	I_{CC1}	Write D0~D31
L	L	H	H	H	H	X	L	I_{CC1}	D0~D31, High Z
L	L	L	H	H	H	L	H	I_{CC1}	Read D0~D7
L	L	H	L	H	H	L	H	I_{CC1}	Read D8~D15
L	L	H	H	L	H	L	H	I_{CC1}	Read D16~D23
L	L	H	H	H	L	L	H	I_{CC1}	Read D24~D31
L	L	L	L	H	H	L	H	I_{CC1}	Read D0~D15
L	L	H	H	L	L	L	H	I_{CC1}	Read D16~D31
L	L	L	L	L	L	L	H	I_{CC1}	Read D0~D31
L	L	X	X	X	X	H	H	I_{CC1}	D0~D31 High-Z
L	H	L	L	X	X	X	L	I_{CC2}	Write D0~D15, D16~31 Standby
L	H	L	H	X	X	X	L	I_{CC2}	Write D0~D7, D16~31 Standby
L	H	H	L	X	X	X	L	I_{CC2}	Write D8~D15, D16~31 Standby
L	H	H	H	X	X	X	L	I_{CC2}	D0~D15 High-Z, D16~31 Standby
L	H	X	X	X	X	H	H	I_{CC2}	D0~D15 High-Z, D16~31 Standby
H	L	X	X	L	L	X	L	I_{CC2}	D0~15 Standby, Write D16~31
H	L	X	X	L	H	X	L	I_{CC2}	D0~15 Standby, Write D16~23
H	L	X	X	H	L	X	L	I_{CC2}	D0~15 Standby, Write D24~31
H	L	X	X	H	H	X	L	I_{CC2}	D0~15 Standby, D16~31 High
H	L	X	X	X	X	H	H	I_{CC2}	D0~15 Standby, D16~31 High Z
H	H	X	X	X	X	X	X	I_{SB1}, I_{SB2}	D0~D31 Standby

Notes : H=V_{IH} : L=VI_{L} : X=V_{IH} or V_{IL}

Read Cycle

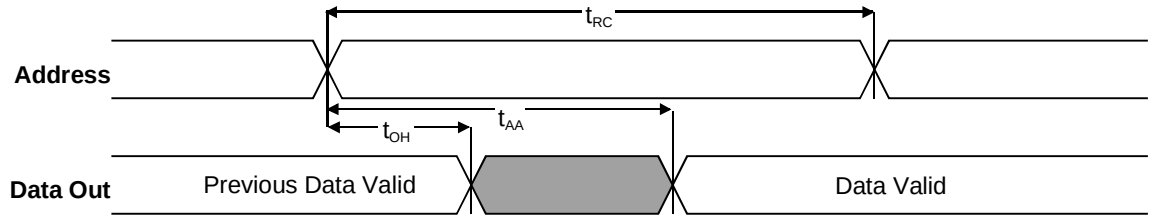
		12		15		17		20		
Parameter	Symbol	Min	Max	Min	Max	Min	Max	Min	Max	Units
Read Cycle Time	t_{RC}	12	-	15	-	17	-	20	-	ns
Address Access Time	t_{AA}	-	12	-	15	-	17	-	20	ns
Chip Select Access Time	t_{ACS}	-	12	-	15	-	17	-	20	ns
Byte Select Access Time	t_{BA}	-	6		7	-	8	-	9	ns
Output Enable to Output Valid	t_{OE}	-	6	-	7	-	8	-	9	ns
Output Hold From Address Change	t_{OH}	3	-	3	-	3	-	3	-	ns
Chip Selection to Output in Low Z	t_{CLZ}	3	-	3	-	3	-	3	-	ns
Byte Selection to Output in Low Z	t_{BLZ}	0	-	0	-	0	-	0	-	ns
Output Enable to Output in Low Z	t_{OLZ}	0	-	0	-	0	-	0	-	ns
Chip Deselection to Output in High Z	t_{CHZ}	0	6	0	7	0	8	0	9	ns
Output Disable to Output in High Z	t_{OHZ}	0	6	0	7	0	8	0	9	ns
Byte Deselction to Output in High Z	t_{BHZ}	0	6	0	7	0	8	0	9	ns

Write Cycle

		12		15		17		20		
Parameter	Symbol	Min	Max	Min	Max	Min	Max	Min	Max	Units
Write Cycle Time	t_{WC}	12	-	15	-	17	-	20	-	ns
Chip Selection to End of Write	t_{CW}	8	-	10	-	11	-	12	-	ns
Byte Selection to End of Write	t_{BW}	8	-	10	-	11	-	12	-	ns
Address Valid to End of Write	t_{AW}	8	-	10	-	11	-	12	-	ns
Address Setup Time	t_{AS}	0	-	0	-	0	-	0	-	ns
Write Pulse Width	t_{WP}	8	-	10	-	11	-	12	-	ns
Write Recovery Time	t_{WR}	0	-	0	-	0	-	0	-	ns
Write to Output in High Z	t_{WHZ}	0	6	0	7	0	8	0	9	ns
Data to Write Time Overlap	t_{DW}	6	-	7	-	8	-	9	-	ns
Data Hold time from Write Time	t_{DH}	0	-	0	-	0	-	0	-	ns
Output Active from End of Write	t_{OW}	3	-	3	-	3	-	3	-	ns

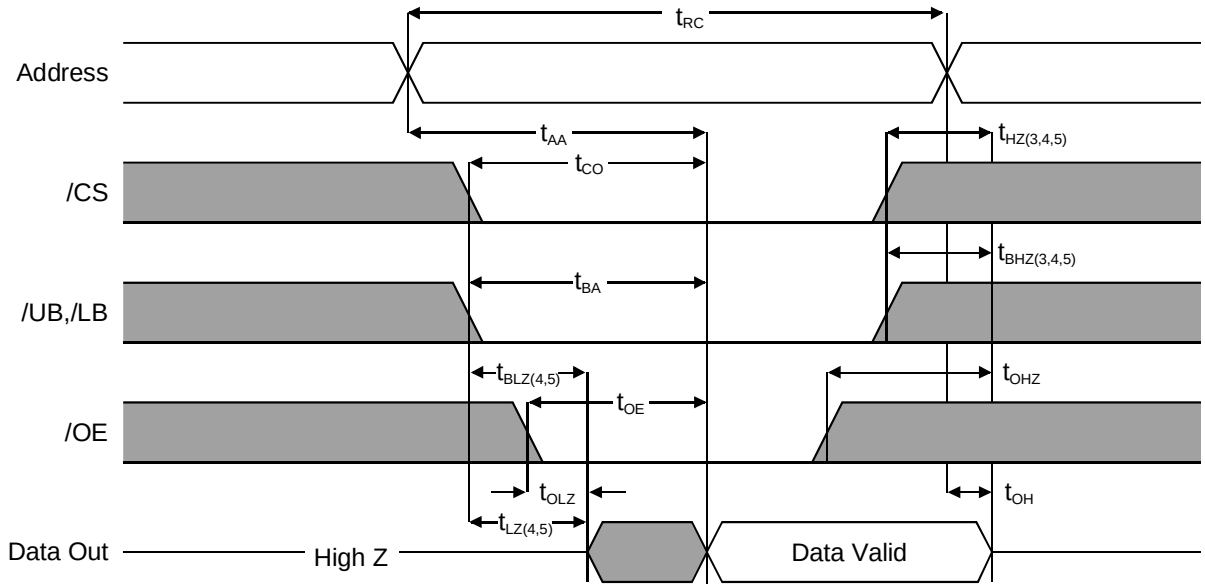
Read Cycle 1

(Address Controlled, /CS=/OE=V_{IL}, /WE=V_{IH})



Read Cycle 2

(/WE = V_{IH})

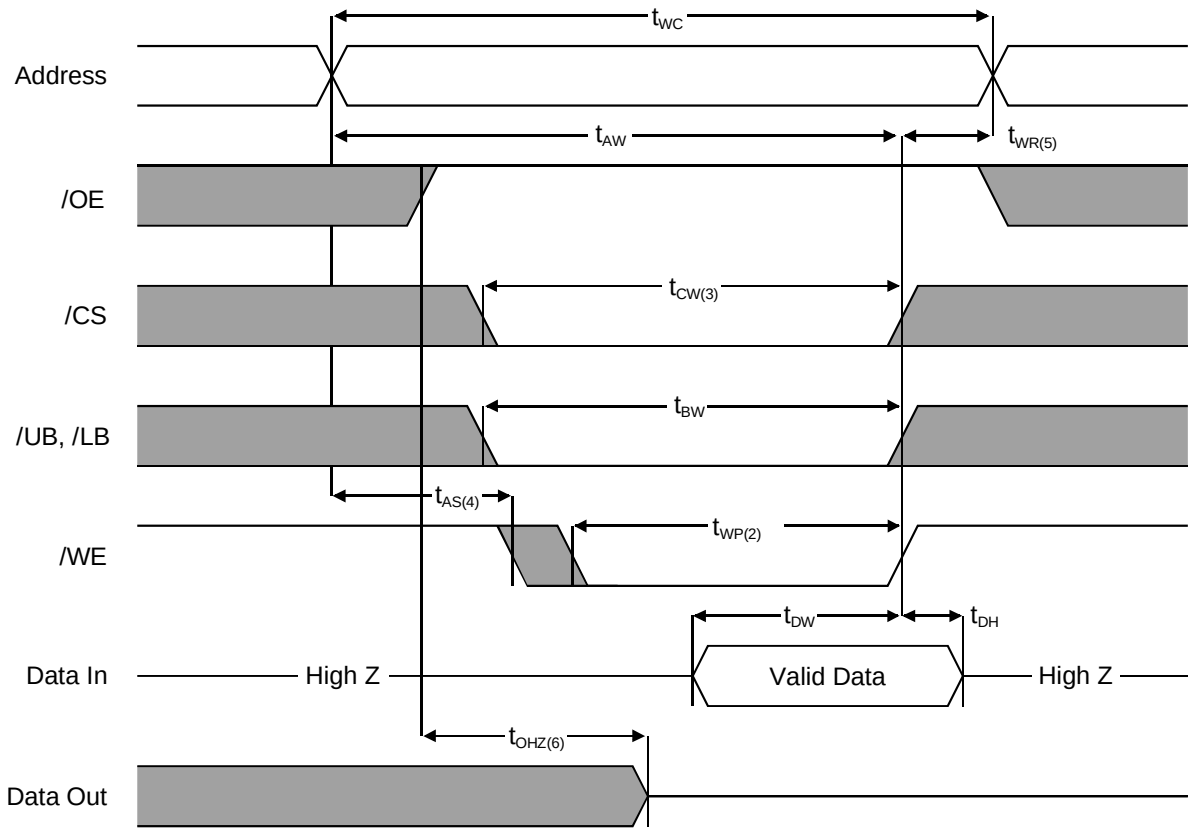


NOTES(READCYCLE)

1. /WE is high for read cycle.
2. All read cycle timing is referenced from the last valid address to the first transition address.
3. t_{HZ} and t_{OHZ} are defined as the time at which the outputs achieve the open circuit condition and are not referenced to V_{OH} or V_{OL} levels.
4. At any given temperature and voltage condition, t_{HZ}(Max.) is less than t_{LZ}(Min.) both for a given device and from device to device.
5. Transition is measured ±200mV from steady state voltage with Load(B). This parameter is sampled and not 100% tested.
6. Device is continuously selected with /CS=V_{IL}.
7. Address valid prior to coincident with /CS transition low.
8. For common I/O applications, minimization or elimination of bus contention conditions is necessary during read and write cycle.

Write Cycle 1

(/OE = Clock)

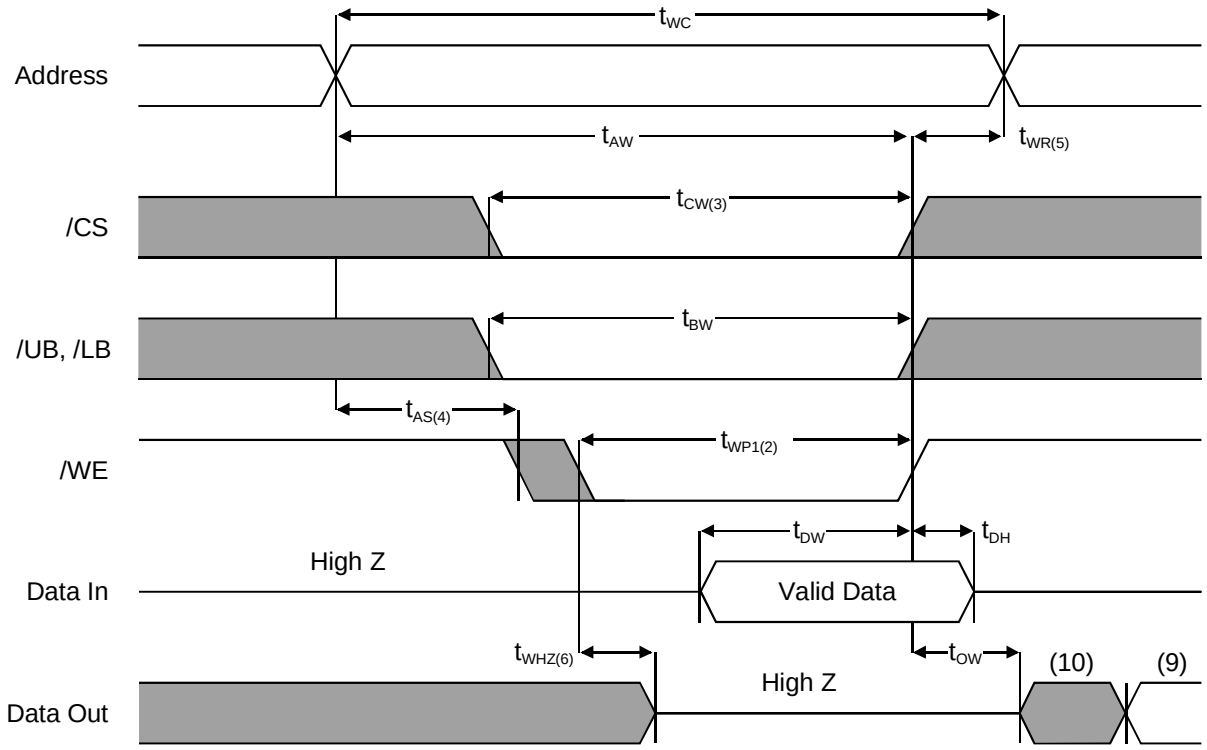


NOTES(WRITE CYCLE)

1. All write cycle timing is referenced from the last valid address to the first transition address.
2. A write occurs during the overlap of a low /CS and /WE. A write begins at the latest transition /CS going low and /WE going low ; A write ends at the earliest transition /CS going high or /WE going high. t_{WP} is measured from the beginning of write to the end of write.
3. t_{CW} is measured from the later of /CS going low to end of write.
4. t_{AS} is measured from the address valid to the beginning of write.
5. t_{WR} is measured from the end of write to the address change. t_{WR} applied in case a write ends as /CS or /WE going high.
6. If /OE, /CS and /WE are in the Read Mode during this period, the I/O pins are in the output low-Z state. Inputs of opposite phase of the output must not be applied because bus contention can occur.
7. For common I/O applications, minimization or elimination of bus contention conditions is necessary during read and write cycle.
8. If /CS goes low simultaneously with /WE going or after /WE going low, the outputs remain high impedance state.
9. Dout is the read data of the new address.
10. When /CS is low I/O pins are in the output state. The input signals in the opposite phase leading to the output should not be applied.

Write Cycle 2

(/OE = Low Fixed)

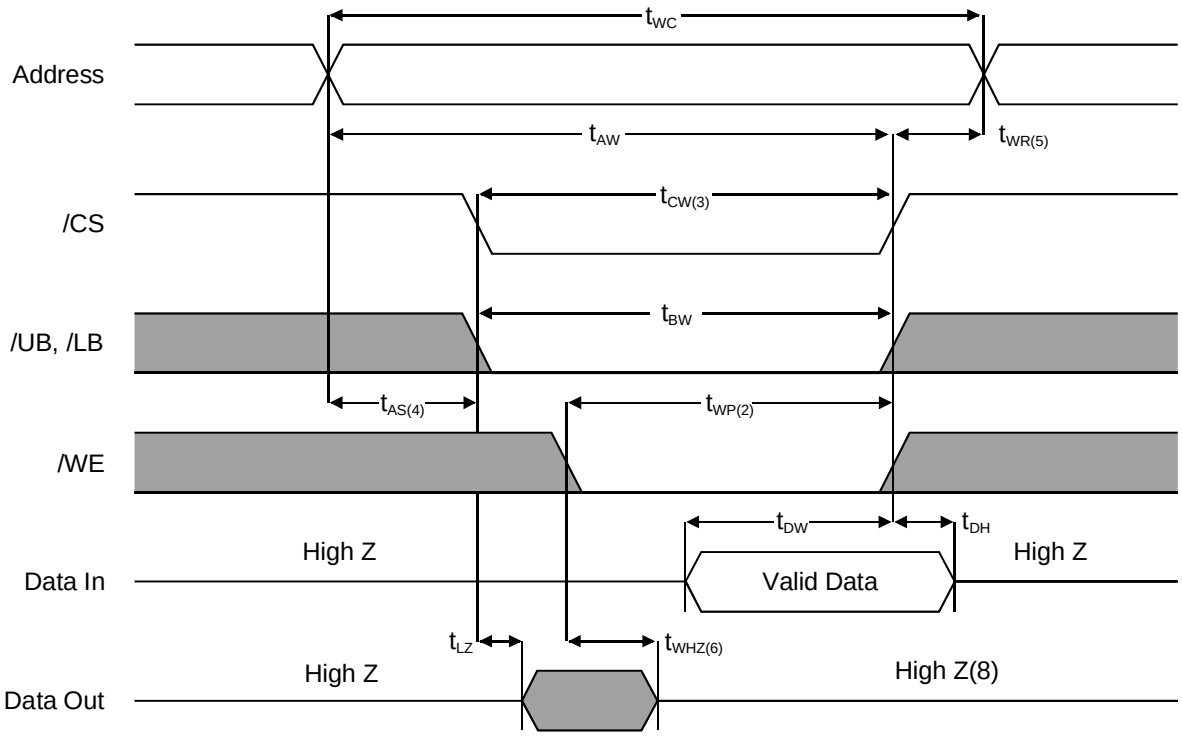


NOTES(WRITE CYCLE)

1. All write cycle timing is referenced from the last valid address to the first transition address.
2. A write occurs during the overlap of a low /CS and /WE. A write begins at the latest transition /CS going low and /WE going low ; A write ends at the earliest transition /CS going high or /WE going high. t_{WP} is measured from the beginning of write to the end of write.
3. t_{CW} is measured from the later of /CS going low to end of write.
4. t_{AS} is measured from the address valid to the beginning of write.
5. t_{WR} is measured from the end of write to the address change. t_{WR} applied in case a write ends as /CS or /WE going high.
6. If /OE, /CS and /WE are in the Read Mode during this period, the I/O pins are in the output low-Z state. Inputs of opposite phase of the output must not be applied because bus contention can occur.
7. For common I/O applications, minimization or elimination of bus contention conditions is necessary during read and write cycle.
8. If /CS goes low simultaneously with /WE going or after /WE going low, the outputs remain high impedance state.
9. Dout is the read data of the new address.
10. When /CS is low I/O pins are in the output state. The input signals in the opposite phase leading to the output should not be applied.

Write Cycle 3

(/CS = Controlled)

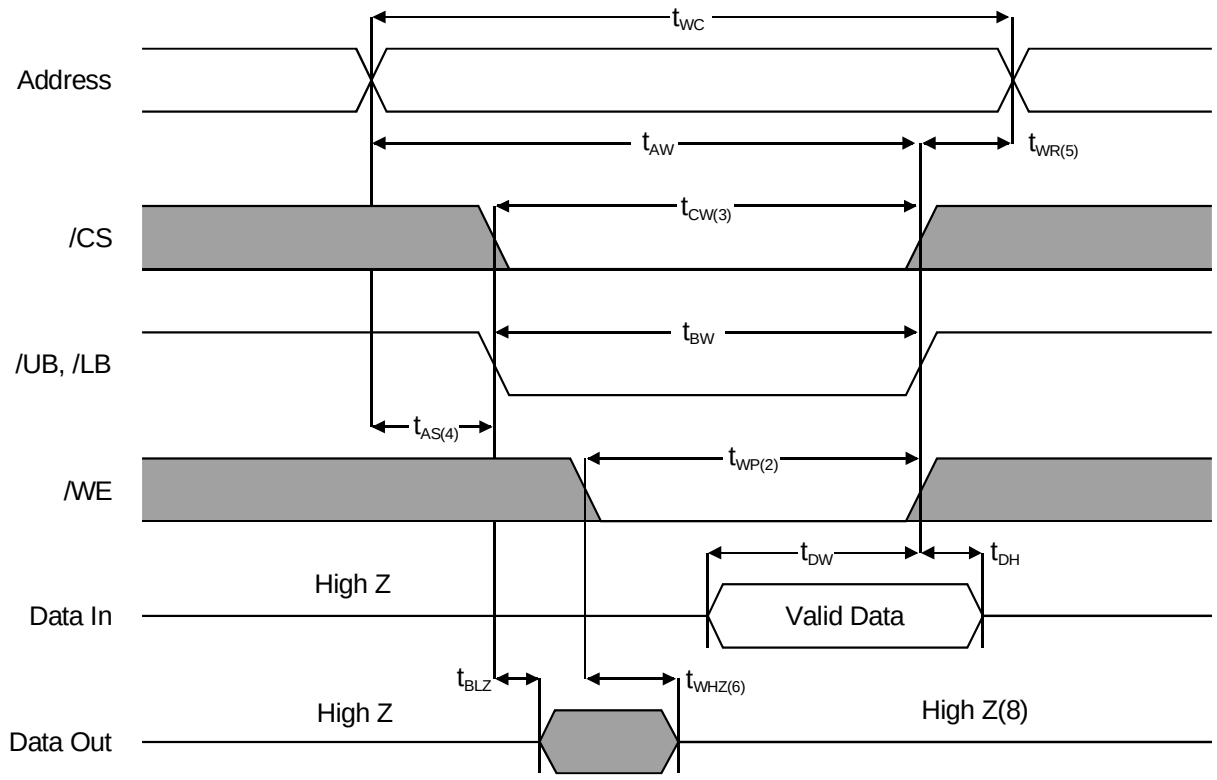


NOTES(WRITE CYCLE)

1. All write cycle timing is referenced from the last valid address to the first transition address.
2. A write occurs during the overlap of a low /CS and /WE. A write begins at the latest transition /CS going low and /WE going low ; A write ends at the earliest transition /CS going high or /WE going high. t_{WP} is measured from the beginning of write to the end of write.
3. t_{CW} is measured from the later of /CS going low to end of write.
4. t_{AS} is measured from the address valid to the beginning of write.
5. t_{WR} is measured from the end of write to the address change. t_{WR} applied in case a write ends as /CS or /WE going high.
6. If /OE, /CS and /WE are in the Read Mode during this period, the I/O pins are in the output low-Z state. Inputs of opposite phase of the output must not be applied because bus contention can occur.
7. For common I/O applications, minimization or elimination of bus contention conditions is necessary during read and write cycle.
8. If /CS goes low simultaneously with /WE going or after /WE going low, the outputs remain high impedance state.
9. Dout is the read data of the new address.
10. When /CS is low : I/O pins are in the output state. The input signals in the opposite phase leading to the output should not be applied.

Write Cycle 4

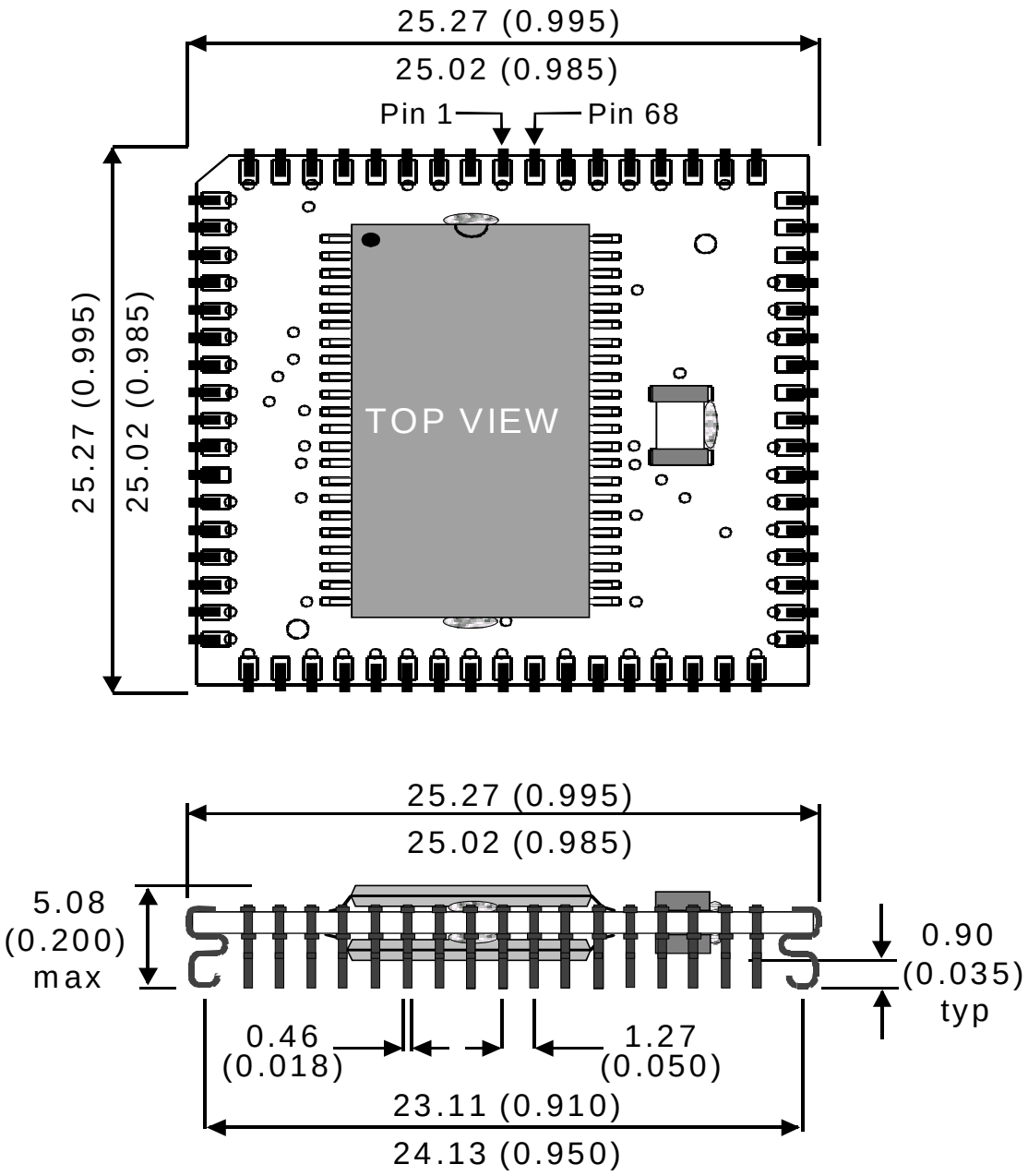
(/UB, /LB Controlled)



NOTES(WRITE CYCLE)

1. All write cycle timing is referenced from the last valid address to the first transition address.
2. A write occurs during the overlap of a low /CS and /WE. A write begins at the latest transition /CS going low and /WE going low ; A write ends at the earliest transition /CS going high or /WE going high. t_{WP} is measured from the beginning of write to the end of write.
3. t_{CW} is measured from the later of /CS going low to end of write.
4. t_{AS} is measured from the address valid to the beginning of write.
5. t_{WR} is measured from the end of write to the address change. t_{WR} applied in case a write ends as /CS or /WE going high.
6. If /OE, /CS and /WE are in the Read Mode during this period, the I/O pins are in the output low-Z state. Inputs of opposite phase of the output must not be applied because bus contention can occur.
7. For common I/O applications, minimization or elimination of bus contention conditions is necessary during read and write cycle.
8. If /CS goes low simultaneously with /WE going or after /WE going low, the outputs remain high impedance state.
9. Dout is the read data of the new address.
10. When /CS is low : I/O pins are in the output state. The input signals in the opposite phase leading to the output should not be applied.

PUMA 68 Pin JEDEC Surface Mount PLCC



Ordering Information

PUMA 68S2000X I - 015

Speed	012 =	12ns
	015 =	15ns
	017 =	17ns
	020 =	20ns
Temp. Range/Screening	Blank =	Commercial
	I =	Industrial
Power Consumption	Blank =	Standard
Pinout Configuration	X =	Industry Standard Pinout
Memory Organisation	2000 =	configurable as 64K x 32 or 128K x 16
Technology	S =	SRAM
Package	PUMA 68 =	68 pin 'J' Leaded PLCC

Co Planarity

Specified as +/- 2 thou max.

Visual Inspection Standard

All devices inspected to ANSI/J-STD-001B Class 2 standard

Moisture Sensitivity

Devices are **moisture sensitive.**

Shelf Life in Sealed Bag 12 months at <40^{O}C and <90% relative humidity (RH).

After this bag has been opened, devices that will be subjected to infrared reflow, vapour phase reflow, or equivalent processing (peak package body temp 220^{O}C) **must be** :

A : Mounted within 72 Hours at factory conditions of <30^{O}C/60% RH

OR

B : Stored at <20% RH

If these conditions are not met or indicator card is >20% when read at 23^{O}C +/-5% devices **require baking** as specified below.

If baking is required, devices may be baked for :-

A : 24 hours at 125^{O}C +/-5% for high temperature device containers

OR

B : 192 hours at 40^{O}C +5^{O}C/-0^{O}C and <5% RH for low temperature device containers**.**

Packaging Standard

Devices packaged in dry nitrogen, JED-STD-020.

Packaged in trays as standard.

Tape and reel available for shipment quantities exceeding 200pcs upon request.

Soldering Recomendations

IR/Convection -	Ramp Rate	6^{O}C/sec max.
	Temp. exceeding 183^{O}C	150 secs. max.
	Peak Temperature	225^{O}C
	Time within 5^{O}C of peak	20 secs max.
	Ramp down	6^{O}C/sec max.
Vapour Phase -	Ramp up rate	6^{O}C/sec max.
	Peak Temperature	215 - 219^{O}C
	Time within 5^{O}C of peak	60 secs max.
	Ramp down	6^{O}C/sec max.

The above conditions must not be exceeded

Note : The above recomendations are based on standard industry practice. Failure to comply with the above recommendations invalidates product warranty.