LATCHED SRAM

16K x 18 SRAM

WITH ADDRESS/ DATA INPUT LATCHES

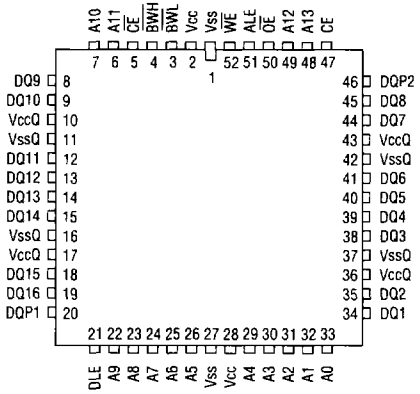
FEATURES

- Fast access times: 15, 17, 20 and 25ns
- Fast Output Enable: 6, 8 and 10ns
- Single +5V ±10% power supply
- Separate, electrically isolated output buffer power supply and ground (VccQ, VssQ)
- Optional +3.3V ±10% output buffer operation
- Separate data input latch
- Common data inputs and data outputs
- BYTE WRITE capability via dual write strobes
- Parity bits
- Address and Chip Enable input latches

OPTIONS	MARKING
• Timing	
15ns access	-15
17ns access	-17
20ns access	-20
25ns access	-25
• Packages	
52-pin PLCC	EJ
52-pin PQFP	LG
• Density	
16K x 18	MT5C2818

PIN ASSIGNMENT (Top View)

52-Pin PLCC (D-3)
52-Pin PQFP (D-5)



GENERAL DESCRIPTION

The Micron SRAM family employs high-speed, low-power CMOS designs using a four-transistor memory cell. Micron SRAMs are fabricated using double-layer metal, double-layer polysilicon technology.

The MT5C2818 SRAM integrates a 16K x 18 SRAM core with advanced peripheral circuitry consisting of address and data input latches, latched active HIGH and active LOW chip enables, separate upper and lower byte write strobes and a fast output enable. The device is ideally suited for "pipelined" systems and systems that benefit from a wide data bus. Parity bits are provided for added data integrity.

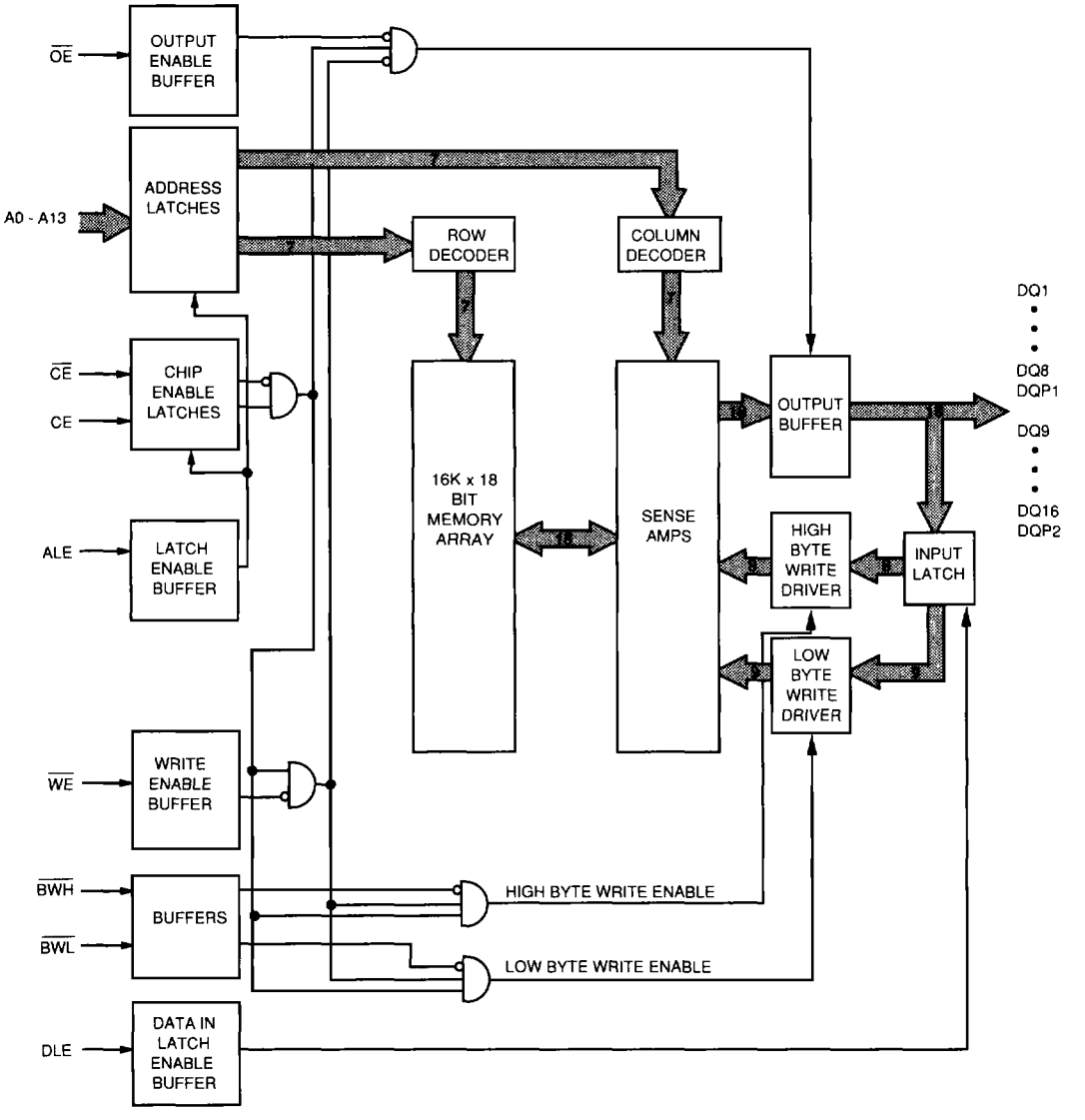
Address and chip enable latches are provided. When address latch enable (ALE) is HIGH, the address and chip enable latches are transparent, allowing the input to flow through the latch. If ALE is LOW, the address and chip enable latch inputs are disabled. This input latch simplifies READ and WRITE cycles by guaranteeing address hold time in a simple fashion.

Dual write strobes ($\overline{BWL}$ and $\overline{BWH}$) allow individual bytes to be written. $\overline{BWL}$ controls DQ1-DQ8 and DQP1, the lower bits. While $\overline{BWH}$ controls DQ9-DQ16 and DQP2, the upper bits.

A data input latch is provided. When data latch enable (DLE) is HIGH, the data latches are in the transparent mode and input data flows through the latch. When DLE is LOW, data present in the inputs are held in the latch until DLE returns HIGH. The data input latch simplifies WRITE cycles by guaranteeing data hold times.

The MT5C2818 operates from a +5V power supply. Separate and electrically isolated output buffer power (VccQ) and ground (VssQ) pins are provided to allow either +3.3V or +5V TTL operation of the output drivers.

FUNCTIONAL BLOCK DIAGRAM



PIN DESCRIPTIONS

PLCC and PQFP PIN NUMBER(S)	SYMBOL	TYPE	DESCRIPTION
33, 32, 31, 30, 29, 26, 25, 24, 23, 22, 7, 6, 49, 48	A0-A13	Input	Address Inputs: These inputs are either latched or unlatched depending on the state of ALE.
52	$\overline{WE}$	Input	Write Enable: This input determines if the cycle is a READ or WRITE cycle. $\overline{WE}$ is LOW for a WRITE cycle and HIGH for a READ cycle
51	ALE	Input	Address Latch Enable: This signal latches the address, CE, and $\overline{CE}$ inputs on its falling edge. When ALE is HIGH, the latch is transparent.
3, 4	$\overline{BWL}$, $\overline{BWH}$	Input	Byte Write Enables: These active LOW inputs allow individual bytes to be written. When $\overline{BWL}$ is LOW, data is written to the lower byte, D1-D8, DQP1. When $\overline{BWH}$ is LOW, data is written to the upper byte, D9-D16, DQP2. When both $\overline{BWH}$ and $\overline{BWL}$ are HIGH and meet the required setup time to the falling edge of $\overline{WE}$, then the WRITE cycle is aborted.
5, 47	$\overline{CE}$,CE	Input	Chip Enables: These signals are used to enable the device. Both active HIGH (CE) and active LOW ($\overline{CE}$) enables are supplied to provide on-chip address decoding when multiple devices are used, as in a dual bank configuration.
50	$\overline{OE}$	Input	Output Enable: This active LOW input enables the output drivers.
21	DLE	Input	Data Latch Enable: When DLE is HIGH, the data latch is transparent. Input data is latched into the on-chip data latch on the falling edge of DLE.
20, 46	DQP1 DQP2	Input/ Output	Parity Data I/O: These signals are data parity bits. The DQP1 is the parity bit for the lower byte, DQ1-DQ8. DQP2 is the parity bit for the upper byte, DQ9-DQ16.
34, 35, 38, 39, 40, 41, 44, 45, 8, 9, 12 13, 14, 15, 18, 19	DQ1-DQ16	Input/ Output	SRAM Data I/O: Lower byte is DQ1-DQ8; Upper byte is DQ9-DQ16. When data is latched, DQ1-DQ16 must meet the setup and hold times around DLE.
2, 28	Vcc	Supply	Power Supply: +5V ±10%
10, 17, 36, 43	VccQ	Supply	Isolated Output Buffer Supply: +5V ±10% or 3.3V ± 10%
11, 16, 37, 42	VssQ	Supply	Isolated Output Buffer Ground: GND
1, 27	Vss	Supply	Ground: GND

TRUTH TABLE

OPERATION	CE	$\overline{CE}$	$\overline{WE}$	$\overline{BWL}$	$\overline{BWH}$	ALE	DLE	$\overline{OE}$	DQ	DQP
Deselected cycle	L	X	X	X	X	X	X	X	High-Z	High-Z
Deselected	X	H	X	X	X	X	X	X	High-Z	High-Z
READ	H	L	H	X	X	H	X	H	High-Z	High-Z
READ	H	L	H	X	X	H	X	L	Q1-Q16	QP1, QP2
LATCHED READ	H	L	H	X	X	L	X	L	Q1-Q16	QP1, QP2
WORD WRITE DQ1-DQ16 transparent data-in	H	L	L	L	L	H	H	X	D1-D16	DP1, DP2
LATCHED WORD WRITE DQ1-DQ16 transparent data-in	H	L	L	L	L	L	H	X	D1-D16	DP1, DP2
WORD WRITE DQ1-DQ16 latched data-in	H	L	L	L	L	H	L	X	D1-D16	DP1, DP2
LATCHED WORD WRITE DQ1-DQ16 latched data-in	H	L	L	L	L	L	L	X	D1-D16	DP1, DP2
ABORTED WRITE	H	L	L	H	H	X	X	X	High-Z	High-Z
BYTE WRITE DQ1-DQ8 transparent data-in	H	L	L	L	H	H	H	X	D1-D8	DP1
LATCHED BYTE WRITE DQ1-DQ8 transparent data-in	H	L	L	L	H	L	H	X	D1-D8	DP1
BYTE WRITE DQ9-DQ16 transparent data-in	H	L	L	H	L	H	H	X	D9-D16	DP2
LATCHED BYTE WRITE DQ9-DQ16 transparent data-in	H	L	L	H	L	L	H	X	D9-D16	DP2
BYTE WRITE DQ1-DQ8 latched data-in	H	L	L	L	H	H	L	X	D1-D8	DP1
LATCHED BYTE WRITE DQ1-DQ8 latched data-in	H	L	L	L	H	L	L	X	D1-D8	DP1
BYTE WRITE DQ9-DQ16 latched data-in	H	L	L	H	L	H	L	X	D9-D16	DP2
LATCHED BYTE WRITE DQ9-DQ16 latched data-in	H	L	L	H	L	L	L	X	D9-D16	DP2

NOTE:
1. Latched inputs (Addresses, CE and $\overline{CE}$) must satisfy the specified setup and hold times around the falling edge of ALE. Data-in must satisfy the specified setup and hold times for DLE.
2. A transparent WRITE cycle is defined by DLE HIGH during the ^{t}DLW time.
3. A latched WRITE cycle is defined by DLE transitioning LOW during the WRITE cycle and data satisfying the specified setup and hold times for DLE.
4. This device contains circuitry that will ensure the outputs will be in High-Z during power up.

ABSOLUTE MAXIMUM RATINGS*

Voltage on V_{CC}/V_{CCQ} Supply Relative to V_{SS}/V_{SSQ} ..... -1.0V to +7.0V
Storage Temperature (Plastic) ..... -55°C to +150°C
Power Dissipation 1.5W
Short Circuit Output Current 50mA

*Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

ELECTRICAL CHARACTERISTICS AND RECOMMENDED DC OPERATING CONDITIONS

(0°C ≤ T_A ≤ 70°C; V_{CC} = 5V ±10%; V_{SS} = V_{SSQ}, unless otherwise noted)

DESCRIPTION	CONDITIONS	SYMBOL	MIN	MAX	UNITS	NOTES
Input High (Logic 1) Voltage		V_{IH}	2.2	V_{CC}+1	V	1
Input Low (Logic 0) Voltage		V_{IL}	-0.5	0.8	V	1, 2
Input Leakage Current	0V ≤ V_{IN} ≤ V_{CC}	I_{LI}	-5	5	µA	
Output Leakage Current	Output(s) Disabled 0V ≤ V_{OUT} ≤ V_{CC}	I_{LO}	-5	5	µA	
Output High Voltage	I_{OH} = -4.0mA	V_{OH}	2.4		V	1
Output Low Voltage	I_{OL} = 8.0mA	V_{OL}		0.4	V	1
Supply Voltage		V_{CC}	4.5	5.5	V	1
Output Buffer Supply Voltage	5V TTL Compatible	V_{CCQ}	4.5	5.5	V	1

DESCRIPTION	CONDITIONS	SYMBOL	TYP	MAX	UNITS	NOTES
Power Supply Current: Operating	$\overline{CE}$ ≤ V_{IL}, CE ≥ V_{IH}; V_{CC} = MAX Outputs Open f = MAX = 1/ ^tRC	I_{CC}	150	250	mA	3
Power Supply Current: Standby	CE ≤ V_{IL}, $\overline{CE}$ ≥ V_{IH}; V_{CC} = MAX Outputs Open f = MAX = 1/ ^tRC	I_{SB1}	50	80	mA	
	$\overline{CE}$ ≥ V_{CC} - 0.2V; CE ≤ V_{SS} +0.2V V_{CC} = MAX; V_{IL} ≤ V_{SS} +0.2V V_{IH} ≥ V_{CC} -0.2V; f = 0	I_{SB2}	5	15	mA	

CAPACITANCE

DESCRIPTION	CONDITIONS	SYMBOL	MAX	UNITS	NOTES
Input Capacitance	T_A = 25°C, f = 1 MHz V_{CC} = 5V	C_I	5	pF	4
Input/Output Capacitance (D/Q)		$C_{I/O}$	9	pF	4

ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

(Note 5) (0°C ≤ T_A ≤ 70°C; Vcc = VccQ = 5V ±10%)

DESCRIPTION		-15		-17		-20		-25			
	SYM	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	UNITS	NOTES
ADDRESS LATCH											
Latch cycle time	^tLC	15		17		20		25		ns	
Latch HIGH time	^tLEH	5		5		5		5		ns	
Address/Chip Enable setup to latch LOW	^tLS	2		2		2		2		ns	
Address/Chip Enable hold from latch LOW	^tLH	3		3		3		3		ns	
Address/Chip Enable setup to latch HIGH	^tLHS	0		0		0		0		ns	
Latch HIGH to output active (Low-Z)	^tLZL	2		2		2		2		ns	6, 7, 4
Latch HIGH to output in High-Z	^tHZL	2	7	2	7	2	7	2	10	ns	6, 7, 4
READ CYCLE											
READ cycle time	^tRC	15		17		20		25		ns	
Address access time	^tAA		15		17		20		25	ns	
Chip Enable access time	^tACE		15		17		20		25	ns	
Output hold from address change	^tOH	4		4		4		4		ns	
Chip Enable to output in Low-Z	^tLZCE	2		2		2		2		ns	6, 7, 4
Chip disable to output in High-Z	^tHZCE	2	7	2	7	2	7	2	10	ns	6, 7, 4
Output Enable access time	^tAOE		6		7		8		10	ns	
Output Enable to output in Low-Z	^tLZOE	0		0		0		0		ns	6, 7, 4
Output disable to output in High-Z	^tHZOE	2	6	2	7	2	8	2	10	ns	6, 7, 4
WRITE Cycle											
WRITE cycle time	^tWC	15		17		20		25		ns	
Chip Enable to end of write	^tCW	13		14		15		20		ns	
Address valid to end of write	^tAW	13		14		15		20		ns	
Address setup time	^tAS	0		0		0		0		ns	
Address hold from end of write	^tAH	0		0		0		0		ns	
WRITE pulse width	^tWP	13		14		15		20		ns	
Data setup time	^tDS	6		7		8		10		ns	
Data hold time	^tDH	0		0		0		0		ns	
Write disable to output in Low-Z	^tLZWE	5		5		5		5		ns	6, 7, 4
Write Enable to output in High-Z	^tHZWE	0	8	0	8	0	10	0	10	ns	6, 7, 4
Byte Write Enable setup time	^tBWS	6		7		8		10		ns	
Byte Write Enable hold time	^tBWH	2		2		2		2		ns	
Byte Write disable setup time	^tBWDS	0		0		0		0		ns	
Data setup to DLE LOW	^tDLS	1		1		1		1		ns	9
Data hold from DLE LOW	^tDLH	3		3		3		3		ns	9
DLE HIGH to end of write	^tDLW	6		7		8		10		ns	8
End of write to DLE HIGH	^tWDLH	0		0		0		0		ns	9
End of write to ALE HIGH	^tWLH	0		0		0		0		ns	
ALE HIGH setup time to write enable LOW	^tLWS	0		0		0		0		ns	
ALE HIGH to end of write	^tLW	13		14		15		20		ns	

AC TEST CONDITIONS

Input pulse levels	Vss to 3.0V
Input rise and fall times	3ns
Input timing reference levels	1.5V
Output reference levels	1.5V
Output load	See Figures 1 and 2

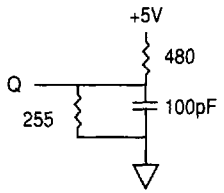


Fig. 1 OUTPUT LOAD EQUIVALENT

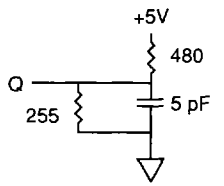
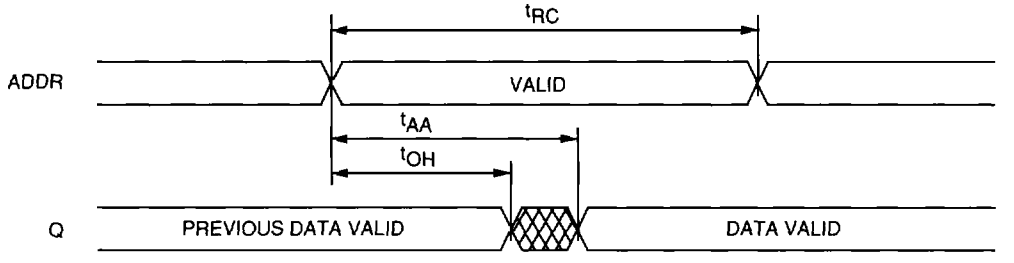


Fig. 2 OUTPUT LOAD EQUIVALENT

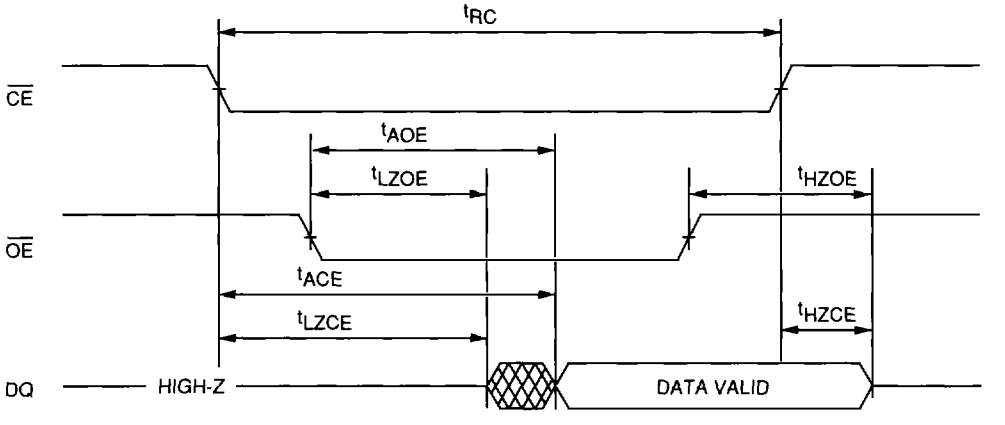
NOTES

1. All voltages referenced to Vss (GND).
2. -3V for pulse width < 20ns.
3. Icc is dependent on output loading and cycle rates.
4. This parameter is sampled.
5. Test conditions as specified with the output loading as shown in Fig. 1 unless otherwise noted.
6. Output loading is specified with CL = 5pF as in Fig. 2. Transition is measured ±500mV from steady state voltage.
7. At any given temperature and voltage condition, ^{t}HZCE is less than ^{t}LZCE, and ^{t}HZOE is less than ^{t}LZOE.
8. A transparent WRITE cycle is defined by DLE being HIGH during the WRITE cycle.
9. A latched WRITE cycle is defined by DLE transitioning LOW during the WRITE cycle and data satisfying the specified setup and hold time with respect to DLE.
10. Any combination of write enable ($\overline{WE}$) and chip enable ($\overline{CE}$) can initiate and terminate a WRITE cycle.
11. $\overline{WE}$ is HIGH for READ cycle.
12. Device is continuously selected. All chip enables are held in their active state.
13. Address valid prior to or coincident with the latest occurring chip enable.
14. CE timing is the same as $\overline{CE}$ timing. The wave form is inverted.
15. If output enable ($\overline{OE}$) is inactive (HIGH), the output will be in High-Z instead of undefined.

READ CYCLE NO. 1 [11, 12]



READ CYCLE NO. 2 [7, 11, 13, 14]

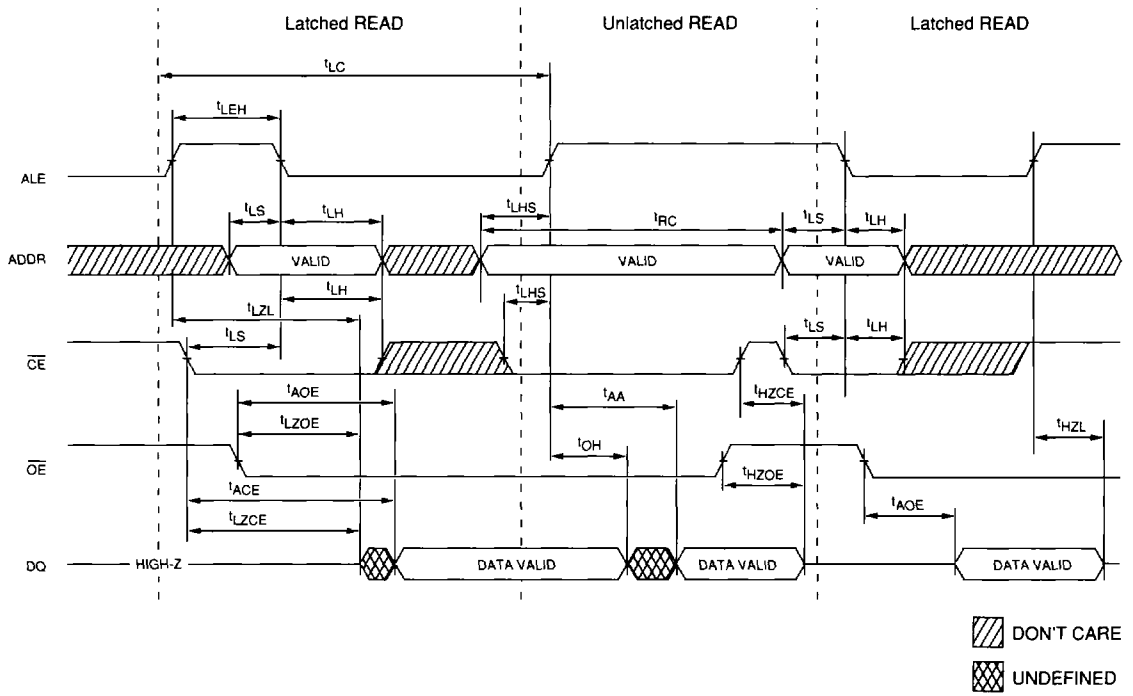


DON'T CARE

UNDEFINED

READ CYCLE NO. 3

(ALE = DLE = HIGH) [7, 11, 14]

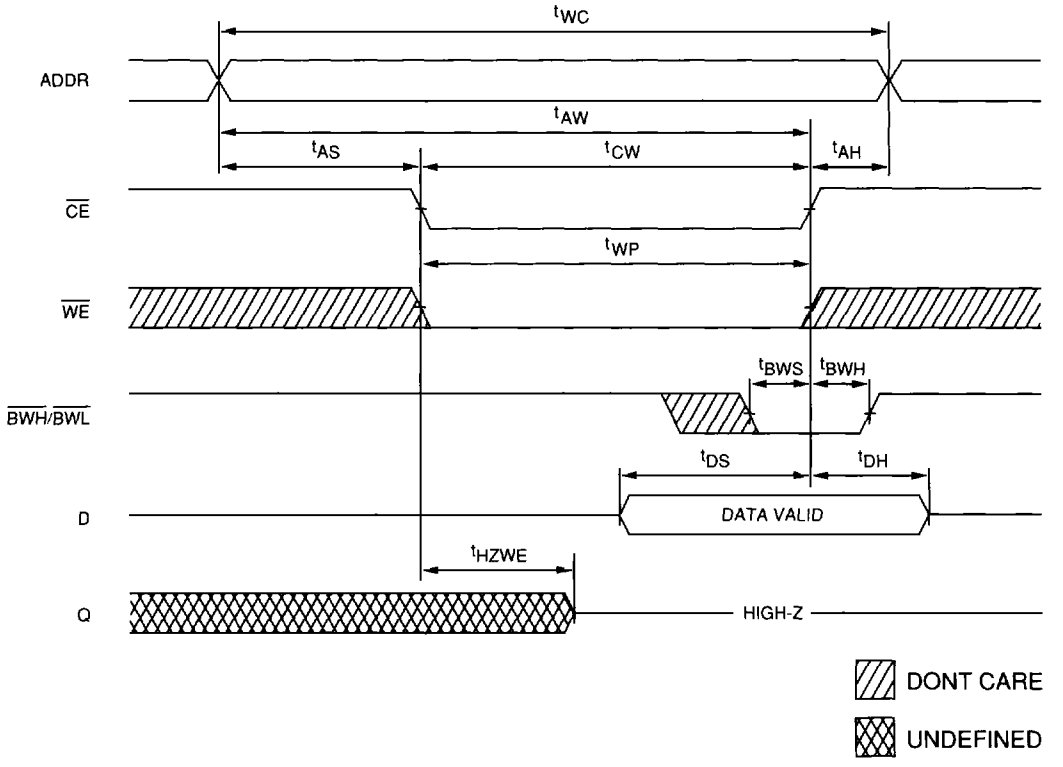


CACHE DATA/LATCHED SRAM

WRITE CYCLE NO. 1

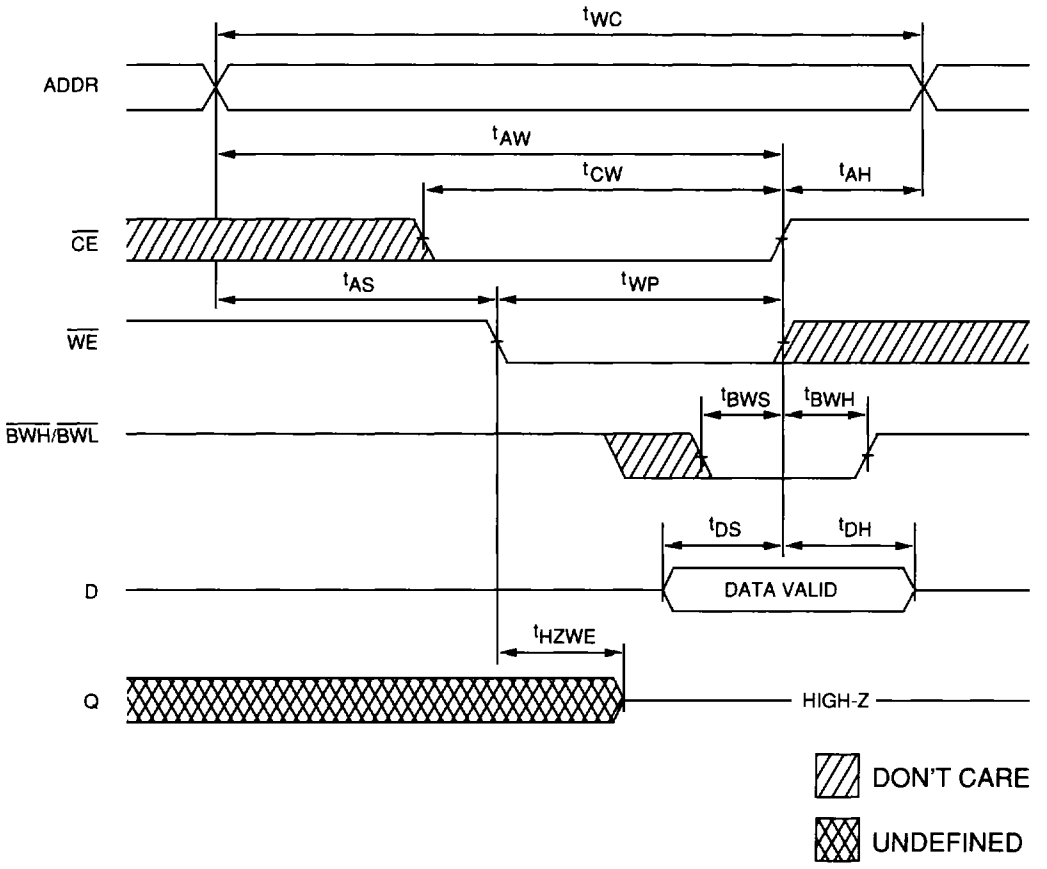
Chip Enable Controlled

(ALE = DLE = HIGH) [10, 14, 15]



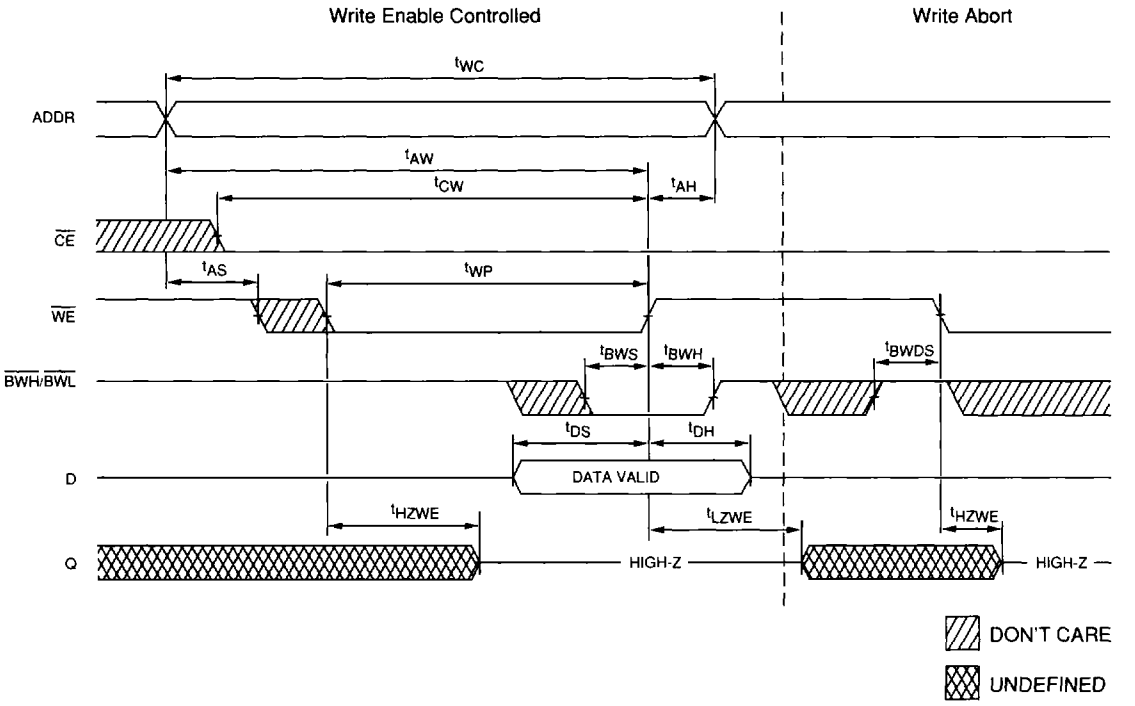
WRITE CYCLE NO. 2

Write Enable Initiated/Chip Enable Terminated
(ALE = DLE = HIGH) [10, 14, 15]



WRITE CYCLE NO. 3

(ALE = DLE = HIGH) [7, 10, 14, 15]



WRITE CYCLE NO. 4 [7, 10, 14, 15]