FLASH MEMORY CARDS

8/16-bit Data Bus
Flash Memory Card

Connector Type

Two-piece 68-pin

| MF82M1-G7DATXX |
| MF84M1-G7DATXX |
| MF88M1-G7DATXX |
| MF810M-G7DATXX |
| MF816M-G7DATXX |
| MF820M-G7DATXX |

DESCRIPTION

The MF8XXX-G7DATXXX is a flash memory card which uses eight-megabit flash electrically erasable and programmable read only memory IC's as common memory and a 64-kilobit electrically erasable and programmable read only memory as attribute memory.

- Program/erase operation by software command control
- Program/erase voltage 12V (common memory)
- 100,000 program/erase cycles
- Write protect switch

FEATURES

- 68 pin JEIDA/PCMCIA
- 8/16 controllable data bus width
- Buffered interface
- TTL interface level

APPLICATIONS

- Notebook computers
- Printers
- Industrial machines

PRODUCT LIST

Item / Type name	Memory capacity	Data bus width (bits)	Access time (ns)	Number of pins	Outline drawing
MF82M1-G7DATXX	2MB				
MF84M1-G7DATXX	4MB				
MF88M1-G7DATXX ★★	8MB	8/16	200	68	68P-002
MF810M-G7DATXX ★★	10MB				
MF816M-G7DATXX ★★	16MB				
MF820M-G7DATXX ★★	20MB				

★★ : Under development

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PIN ASSIGNMENT

Pin No.	Symbol	Function	Pin No.	Symbol	Function
1	GND	Ground	35	GND	Ground
2	D 3		36	$\overline{CD\ 1}$	Card detect 1
3	D 4		37	D11	
4	D 5	Data I/O	38	D12	
5	D 6		39	D13	Data I/O
6	D 7		40	D14	
7	$\overline{CE\ 1}$	Card enable 1	41	D15	
8	A10	Address input	42	$\overline{CE\ 2}$	Card enable 2
9	$\overline{OE}$	Output enable	43	NC	
10	A11		44	NC	No connection
11	A 9		45	NC	
12	A 8	Address input	46	A17	
13	A13		47	A18	
14	A14		48	A19	Address input
15	$\overline{WE}$	Write enable	49	A20	
16	NC	No connection	50	A21	A21 (NC for ≤ 2 MB types)
17	Vcc	Power supply voltage	51	Vcc	Power supply voltage
18	VPP 1	Programming supply voltage 1	52	VPP 2	Programming supply voltage 2
19	A16		53	A22	A22 (NC for ≤ 4 MB types) Address input
20	A15		54	A23	A23 (NC for ≤ 8 MB types)
21	A12		55	A24	
22	A 7		56	NC	
23	A 6		57	NC	
24	A 5	Address input	58	NC	No connection
25	A 4		59	NC	
26	A 3		60	NC	
27	A 2		61	$\overline{REG}$	Attribute memory select
28	A 1		62	BVD 2	Battery voltage detect 2
29	A 0		63	BVD 1	Battery voltage detect 1
30	D 0		64	D 8	
31	D 1	Data I/O	65	D 9	Data I/O
32	D 2		66	D10	
33	WP	Write protect	67	$\overline{CD\ 2}$	Card detect 2
34	GND	Ground	68	GND	Ground

BLOCK DIAGRAM (MF820M-G7DATXX)
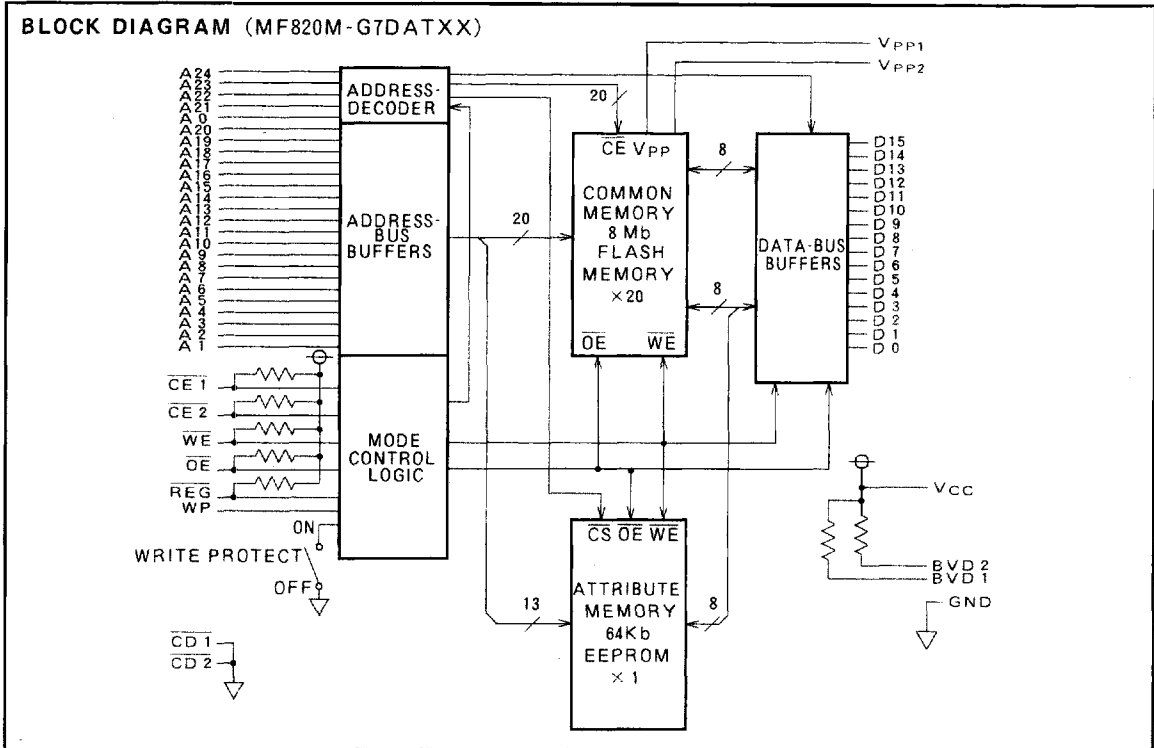
FUNCTIONAL DESCRIPTION

The operating mode of the card is determined by five active low control signals ($\overline{REG}$, $\overline{CE1}$, $\overline{CE2}$, $\overline{OE}$, $\overline{WE}$), three supply voltages (V_{CC}, V_{PP1}, V_{PP2}) and control registers located in each memory IC.

Common memory function

When the $\overline{REG}$ signal is set to a high level common memory is selected.

Read only mode

When the voltages applied to both V_{PP1} and V_{PP2} are less than the voltage applied to V_{CC} (i.e. V_{PP} =0V to V_{CC}), the control registers of each memory IC are set to read only mode.

Operation of the card then depends on the four possible combinations of $\overline{CE1}$ and $\overline{CE2}$ (note $\overline{WE}$ should be set to a high level when the device is in read only mode except during combination (4) where it's condition is unimportant):

(1) If $\overline{CE1}$ is set to a low level and $\overline{CE2}$ is set to a high level, the card will work as an eight bit data

bus width card. Data can be accessed via the lower half of the data bus (D0 to D7).

(2) If both $\overline{CE1}$ and $\overline{CE2}$ are set to a low level, data will be accessible via the full sixteen bit data bus width of the card. In this mode LSB of address bus (A0) is ignored.

(3) If $\overline{CE1}$ is set to a high level and $\overline{CE2}$ is set to a low level the odd bytes (only) can be accessed through upper half of the data bus (D8 to D15). This mode is useful when handling the odd (upper) bytes in a sixteen bit interface system. Note that A0 is also ignored in this operating condition.

(4) If $\overline{CE1}$ and $\overline{CE2}$ are set to a high level, the card will be in standby mode where it consumes low power. The data bus is kept high impedance.

When $\overline{OE}$ is set to a low level data can be read from the card, depending on the address applied and the setting of $\overline{CE1}$ and $\overline{CE2}$ as mentioned above, except under combination (4).

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When $\overline{OE}$ is set to a high level and $\overline{WE}$ is set to a high level the card is in an output disable mode and the data bus will be in a high impedance state regardless of the condition of $\overline{CE1}$ and $\overline{CE2}$.

Read/write mode

When a programming voltage (V_{PPH}) is applied to either or both of $V_{PP}1$ and $V_{PP}2$, read/write mode is enabled for the corresponding banks of memory IC's inside the card. $V_{PP}1$ enables the Even Byte bank and $V_{PP}2$ enables the Odd Byte bank.

By using the 4 combinations of $\overline{CE1}$ and $\overline{CE2}$ as described under Read only mode above the appropriate Data Out and Command/Data In bus selection can be made.

If $\overline{OE}$ is set to a high level and $\overline{WE}$ set to a low level, the control register will latch command data applied at the rising edge of the $\overline{WE}$ signal. Note that more than one bus cycle may be required to latch the command and/or the related data — please refer to the Command Definition table.

If $\overline{OE}$ is set to a low level and $\overline{WE}$ is set to a high level the card data can be read from the card depending on the condition of the control register.

After latching the command data, the card will go into programming, erasure or other operation mode. For details please refer to the Command Definition table, each individual command's definition and the programming and erasure algorithms.

Attribute memory

When the $\overline{REG}$ signal is set to a low level attribute memory is selected.

The card includes a byte wide attribute memory consisting of 8K bytes of EEPROM located at the even addresses when the card is in the 8 bit operating mode. It is located at sequential addresses on the lower half of the data bus when the card is in 16 bit operating mode i.e. A0 is ignored.

To access the attribute memory, first set $\overline{CE1}$ and $\overline{CE2}$. Set $\overline{CE1}$ to low level and $\overline{CE2}$ to high level for 8 bit mode or $\overline{CE1}$ and $\overline{CE2}$ to low level for 16 bit mode. Then select the required address. Note please take care that in 8 bit mode A0 must be set low for attribute memory access i.e. an even address is applied. In 16

bit mode it is not important whether A0 is high or low. Data can then be read by setting $\overline{OE}$ to a low level with $\overline{WE}$ set to a high level.

Writing to the attribute memory can be achieved in one of two ways, in byte mode or in page mode. The page mode write is a function which allows up to 32 bytes of data to be written in a single cycle. A page is defined as a block of 32 even bytes selected by addresses A6 through A13.

To write to attribute memory set $\overline{OE}$ to high level and $\overline{WE}$ to low level. The data to be written will be latched at the rising edge of $\overline{WE}$. Then, unless $\overline{WE}$ changes back from high level to low level within 30 μs an automatic erase/program operation starts which will complete within 10ms.

If $\overline{WE}$ makes a transition back from high to low level within 30 μs of the first data being latched then further bytes from a page of up to 32 bytes can be latched with further $\overline{WE}$ low to high transitions. The latching operation is repeated until all bytes are loaded at which point holding $\overline{WE}$ high for greater than 30 μs will initiate execution of a page erase/program operation which will complete within 10ms.

During page write data loading operations all data must be addressed within one 32 byte page i.e. the page address which is selected by A6 through A13 and must remain constant throughout the data load. Please also remember that for attribute memory A0 is not applicable and it should be set to low, even addressing only, in 8 bit mode or ignored for 16 bit mode.

Write protect mode

The card has a write protect switch on the opposite edge to the connector edge. When it is switched on, the card will be placed into a write protect mode, where data can be read from the card but it cannot be written to it. The WP output pin is set to a high level when the card is in write protect mode and V_{CC} is applied. When the card is not in write protect mode the WP output pin is set to a low level when V_{CC} is applied. By reading the state of the WP output the host system can easily check whether the card is in write protect mode or not.

FUNCTION TABLE (COMMON MEMORY) READ ONLY MODE

Mode	$\overline{REG}$	$\overline{CE2}$	$\overline{CE1}$	$\overline{OE}$	$\overline{WE}$	A0	VPP2	VPP1	I/O (D15-D8)	I/O (D7-D0)
Standby	H	H	H	X	X	X	VPPL	VPPL	High-Z	High-Z
Read A (16-bit)	H	L	L	L	H	X	VPPL	VPPL	Odd byte data out	Even byte data out
Read B (8-bit)	H	H	L	L	H	L	VPPL	VPPL	High-Z	Even byte data out
	H	H	L	L	H	H	VPPL	VPPL	High-Z	Odd byte data out
Read C (8-bit)	H	L	H	L	H	X	VPPL	VPPL	Odd byte data out	High-Z
Output disable	H	X	X	H	H	X	VPPL	VPPL	High-Z	High-Z

Note 1 : H=V_{IH}, L=V_{IL}, X=V_{IH} or V_{IL}

FUNCTION TABLE (COMMON MEMORY) READ/WRITE MODE

Mode	$\overline{REG}$	$\overline{CE2}$	$\overline{CE1}$	$\overline{OE}$	$\overline{WE}$	A0	VPP2	VPP1	I/O (D15-D8)	I/O (D7-D0)
Standby	H	H	H	X	X	X	VPPX	VPPH	High-Z	High-Z
	H	H	H	X	X	X	VPPH	VPPX	High-Z	High-Z
Read A (16-bit)	H	L	L	L	H	X	VPPH	VPPH	Odd byte data out	Even byte data out
Read B (8-bit)	H	H	L	L	H	L	VPPX	VPPH	High-Z	Even byte data out
	H	H	L	L	H	H	VPPH	VPPX	High-Z	Odd byte data out
Read C (8-bit)	H	L	H	L	H	X	VPPH	VPPX	Odd byte data out	High-Z
Write A (16-bit)	H	L	L	H	L	X	VPPH	VPPH	Command or odd byte data in	Command or even byte data in
Write B (8-bit)	H	H	L	H	L	L	VPPX	VPPH	High-Z	Command or even byte data in
	H	H	L	H	L	H	VPPH	VPPX	High-Z	Command or odd byte data in
Write C (8-bit)	H	L	H	H	L	X	VPPH	VPPX	Command or odd byte data in	High-Z
Output disable	H	X	X	H	H	X	VPPH	VPPX	High-Z	High-Z
	H	X	X	H	H	X	VPPX	VPPH	High-Z	High-Z

Note 2 : H=V_{IH}, L=V_{IL}, X=V_{IH} or V_{IL}, VPPX = VPPL or VPPH
To operate refer to the command definition, algorithms and so on.

FUNCTION TABLE (ATTRIBUTE MEMORY)

Mode	$\overline{REG}$	$\overline{CE2}$	$\overline{CE1}$	$\overline{OE}$	$\overline{WE}$	A0	VPP2	VPP1	I/O (D15-D8)	I/O (D7-D0)
Standby	L	H	H	X	X	X	Vcc	Vcc	High-impedance	High-impedance
Read A (16-bit)	L	L	L	L	H	X	Vcc	Vcc	Data out (not valid)	Even byte data out
Read B (8-bit)	L	H	L	L	H	L	Vcc	Vcc	High-impedance	Even byte data out
	L	H	L	L	H	H	Vcc	Vcc	High-impedance	Data out (not valid)
Read C (8-bit)	L	L	H	L	H	X	Vcc	Vcc	Data out (not valid)	High-impedance
Write A (16-bit)	L	L	L	H	L	X	Vcc	Vcc	Odd byte data in (not valid)	Even byte data in
Write B (8-bit)	L	H	L	H	L	L	Vcc	Vcc	High impedance	Even byte data in
	L	H	L	H	L	H	Vcc	Vcc	High impedance	Odd byte data in (not valid)
Write C (8-bit)	L	L	H	H	L	X	Vcc	Vcc	Odd byte data in (not valid)	High impedance
Output disable	L	X	X	H	H	X	Vcc	Vcc	High Impedance	High Impedance

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COMMAND DEFINITION

When either or both V_{PP1} and V_{PP2} are applied the programming voltage ($V_{PP}H$) the corresponding

memories of the card are set to read/write mode and the operation is controled by the software command written in the control register.

COMMAND DEFINITION TABLE

Command	Bus cycles	First bus cycle			Second bus cycle			
		Mode	Address	Data in	Mode	Address	Data in	Data out
Read／Reset	1	Write	ZA	FFh (FFFFh)	—	—	—	—
Programme Setup／ Programme	2	Write	PA	40h (4040h)	Write	PA	PD	—
Erase Setup／ Erase Confirm	2	Write	BA	20h (2020h)	Write	BA	D0h (DD00h)	—
Erase Suspend／ Erase Resume	2	Write	BA	B0h (B0B0h)	Write	BA	D0h (D0D0h)	—
Read Status Register	2	Write	ZA	70h (7070h)	Read	—	—	RD
Clear Status Register	1	Write	ZA	50h (5050h)	—	—	—	—
Read Device Identifier Code	2	Write	ZA	90h (9090h)	Read	DIA	—	DID

Note 3. Indicates the basic functions of commands. Refer to the algorithms to operate.
Signal status is defined in function table and bus status.
Parenthesized data shows the data for 16 bit mode operation.
ZA = an address of a memory zone (Please reser to the memory zone)
PA = Programming address
PD = Programming data
BA = An address of a memory block (Please refer to the memory block)
RD = Data of status Register
DIA = Device identifier address
000000h for manufacturer code
000002h for device code
DID = Device identifier data
manufacturer code : 89h (8989h)
device code : A2h (A2A2h)

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Read/Reset

The memory in the card is switched to read mode by writing FFh (FFFFh for 16 bit operation) into the control resister. This mode is maintained until the contents of register are changed. This mode have nothing to do with the voltage of V_{PP}.

This mode needs to be written to every memory zone to which access is required.

Programme Setup/Programme

The setup programme command sets up the card for programming. It is applied when 40h (4040h for 16 bit operation) is written to control register. Programming will take place automatically after latching the address and data which are applied at the rising edge of $\overline{WE}$.

The completion of programme can be confirmed by reading status register, after writing Read status register command 70h (7070h for 16 bit operation) to control register.

(For details please refer to the algorithm)

Erase Setup/Erase confirm

The erase setup is a command to set up the memory block for erasure. Writing setup erase command 20h (2020h for 16 bit operation) in the control register followed by erase confirm command D0h (D0D0h for 16 bit operation) will initiate a erasure opertion. Eraseing will take place automaticaly after the rising edge of $\overline{WE}$ controlled by a internal timer.

The completion of erase can be confirmed by reading status register, after writing read status register command 70h (7070h for 16 bit operation) to control register.

(For details please refer to the algorithm)

These commands will not erase all the data of a memory card and should be repeated for all the required memory blocks. At an eight bit access mode it should be noticed that the erasure of a memory block will result in odd byte or even byte erasure.

Erase Suspend/Erase Resume

The erase suspend command B0h (B0B0h for 16 bit operation) is a command to generate erase interruption and to read data from another block of selected memory zone.

By writing in the control register erase resume command D0h (D0D0h for 16 bit operation), the memory block will continue the erase operation.

These commands must be executed in erase algo-

rithm.

(For details please refer to the algorithm)

Read Status Register

The Read status register is a command to read the status register's data and to make sure programme or earse operations complete successfully. The data of status register can be read after writing 70h (7070h for 16 bit operation) in the control register. The register's read data is latched on the falling edge of $\overline{OE}$. At programme or erase, the status register's data must be read to verify the results.

Clear Status Register

The clear status register command will clear data of status register. It is applied when 50h (5050h for 16 bit operation) is written to the control register.

If an error occured during programme or erase, the status register must be cleared before retrying programme or erase.

Read Device Identifier Codes

The read device identifier codes command is implemented by writing 90h (9090h for 16 bit operation) to the command register. After writing the command, manufacturer code can be read at the address of 000000h of the zone and device code can be read at the address 000002h of the zone. Each card uses the same type of memory throughout and each memory zone will respond the same code.

(Do not apply high voltage to A10 pin in order to try and read the device identifier codes as this will result in the card being destroyed.)

FLASH MEMORY CARDS

STATUS REGISTER

When operating programme or erase, it is necessary to read status register data and to transact these bit. Each memory IC used in this card has internal status register to make sure programme or erase operations complete successfully.

7 (15) BIT	6 (14) BIT	5 (13) BIT	4 (12) BIT	3 (11) BIT	2~0 (10~8) BIT
Programme / Erase Status Bit	Erase Suspend Bit	Erase Error Bit	Programme Error Bit	Vpp Error Bit	Reserved

Note 4 . () ; for 16 bit operation

Bit ; Field name

7(15) BIT ; Programme/Erase Status Bit
    0 = Busy (in programming/erasing)
    1 = Ready

6(14) BIT ; Erase Suspend Bit
    1 = Erase Suspended

5(13) BIT ; Erase Error Bit
    1 = Erase Error

4(12) BIT ; Programme Error Bit
    1 = Programme Error

3(11) BIT ; Vpp Error
    1 = Error of voltage at Vpp

2(10) BIT
~
0(8) BIT ; Reserved for future

MEMORY ZONE AND BLOCK

8 bit mode   1 zone = 64KB * 16 blocks

Even byte		Odd byte			
0000000h	Zone 0	0000001h	Zone 1	000001h	Block 0
01FFFFEh		01FFFFFh		01FFFFh	
0200000h	Zone 2	0200001h	Zone 3	020001h	Block 1
03FFFFEh		03FFFFFh		03FFFFh	
0400000h	Zone 4	0400001h	Zone 5	.	.
05FFFFEh		05FFFFFh		.	.
0600000h	Zone 6	0600001h	Zone 7	.	.
07FFFFEh		07FFFFFh		1E0001h	Block15
0800000h	Zone 8	0800001h	Zone 9	1FFFFFh	
09FFFFEh		09FFFFFh			
0A00000h	Zone10	0A00001h	Zone11		
0BFFFFEh		0BFFFFFh			
0C00000h	Zone12	0C00001h	Zone13		
0DFFFFEh		0DFFFFFh			
0E00000h	Zone14	0E00001h	Zone15		
0FFFFFEh		0FFFFFFh			
1000000h	Zone16	1000001h	Zone17		
11FFFFEh		11FFFFFh			
1200000h	Zone18	1200001h	Zone19		
13FFFFEh		13FFFFFh			

↑ Connected to Vpp 1   ↑ Connected to Vpp 2

Zone 2 to 19 do not exist in 2 MB
Zone 4 to 19 do not exist in 4 MB
Zone 8 to 19 do not exist in 8 MB
Zone 10 to 19 do not exist in 10MB
Zone 16 to 19 do not exist in 16MB

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16 bit mode

1 zone＝64K W ＊16 blocks

	Even byte	Odd byte
0000000h	Zone 0	
01FFFFFh		
0200000h	Zone 1	
03FFFFFh		
0400000h	Zone 2	
05FFFFFh		
0600000h	Zone 3	
07FFFFFh		
0800000h	Zone 4	
09FFFFFh		
0A00000h	Zone 5	
0BFFFFFh		
0C00000h	Zone 6	
0DFFFFFh		
0E00000h	Zone 7	
0FFFFFFh		
1000000h	Zone 8	
11FFFFFh		
1200000h	Zone 9	
13FFFFFh		

000000h	Block 0
01FFFFh	
020000h	Block 1
03FFFFh	
.	. . .
.	. . .
.	. . .
1E0000h	Block 15
1FFFFFh	

↑ Connected to Vpp 1   ↑ Connected to Vpp 2

A0 signal is ignored at 16 bit mode.

Zone 1 to 9 do not exist in   2 MB
Zone 2 to 9 do not exist in   4 MB
Zone 4 to 9 do not exist in   8 MB
Zone 5 to 9 do not exist in 10MB
Zone 8 to 9 do not exist in 16MB

PROGRAMME SEQUENCE

8 bit Operation

First apply $V_{PP}H$ to $V_{PP}1$ and/or $V_{PP}2$. Then the write programme setup command (40h) to the address to be programmed. The next write sequence will initiate the programming operation which will end automatically as this period being controlled by an internal timer and the data will be programmed. To make sure that the data is programmed correctly write a read status register command (70h) and read data. (Reading should be waited more than $6\mu s$ after the programme setup command)

If the data is programed step address and program me data according to the above sequence.

The next address to be programmed should be written with in a memory zone whose V_{PP} voltage is set to $V_{PP}H$. If not write the reset command (FFh) and then drop the V_{PP} voltage to $V_{PP}L$.

Then apply V_{PP} for the desired memory zone and proceed with programming.

In applications where $V_{PP}1$ and $V_{PP}2$ are shorted together all addresses can be programmed without there being any need for the programming algorithm to take account of the cards memory zone architecture.

16 bit operation

The algorithm of 16 bit programming is almost same as the 8 bit programming. (Please refer to the algorithm and the status of bus at programming)

ERASE SEQUENCE

ERASE
8 bit Operation

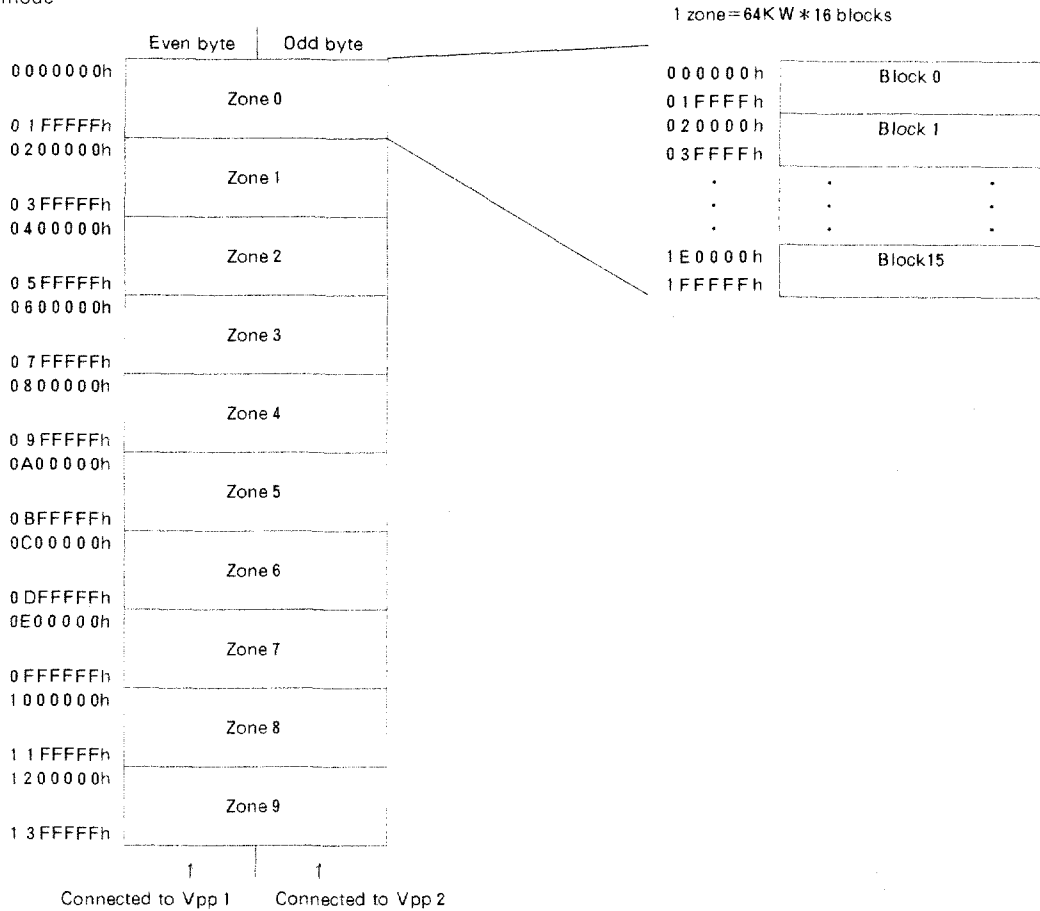First apply $V_{PP}H$ to $V_{PP}1$ and/or $V_{PP}2$. Then write the erase setup command (20h) and erase cofirm command (D0h) for the applicable block address.

An erasure operation will then commence which will be finished in 1.6s typical or less this being automatically controlled by an internal timer.

To make sure that the data is erased correctly write the read status register command (70h) and read data (Reading should be waited more than 300ms after the erase confirm command). After erasure has been completed write the reset command (FFh) to the control register, set $V_{PP}1$ and/or $V_{PP}2$ to $V_{PP}L$ as applicable and proceed with the erase operation for the next memory block.

16 bit Operation

Most of the algorithm of 16 bit erasure is same as the one of the 8 bit erasure.
(Please refer to the algorithm and the state of bus at erasure.)

ERASE SUSPEND
8 bit Operation

The erase suspend is a command to generate block erase interruption in order to read data from another block of the selected memory zone. It is necessary to write the erase suspend command (B0h) in the erase algorithm. The excecution of the erase suspend can be confirmed by reading data of the status register, after writing the read status register command (70h).

Then it is necessary to write the read command (FFh) in control register in order to read data, after reading the status register's data.

After the erase resume command (D0h) is written in the control register, the memory block will continue erase operation.

16 bit Operation

Most of the algorithm of 16 bit erase suspending is same as the one of the 8 bit erase suspending.
(Please refer to the algorithm and the state of bus at erase suspending.)

PROGRAMME ALGORITHM
8 bit mode

PROGRAMME START

$V_{CC} = 5\,V$, $V_{PP} = V_{PPH}$

ADDRESS = FIRST LOCATION

WRITE PROGRAMME SETUP COMMAND (40h)

WRITE PROGRAMME DATA

WRITE STATUS REGISTER READ COMMAND (70h)

READ STATUS REGISTER

CHECK PROGRAMME STATUS BIT — BIT 7 = "0"

BIT 7 = "1"

CHECK V_{PP} ERROR BIT — BIT 3 = "1"

BIT 3 = "0"

CHECK PROGRAMME ERROR BIT — BIT 4 = "1"

BIT 4 = "0"

LAST ADDRESS? — NO → ADDRESS = NEXT ADDRESS

YES

WRITE RESET COMMAND (FFh)

$V_{PP} = V_{PPL}$

PROGRAMME PASSED

WRITE STATUS REGISTER CLEAR COMMAND (50h)

PROGRAMME FAILED

Note 5 . . This is programme algorithm for a memory zone and not for a card.
. If V_{PP} error bit is detected, try to programme again at V_{PPH} level.

PROGRAMME ALGORITHM
16 bit mode

```
                    ┌─────────────────────┐
                    │  PROGRAMME START    │
                    └─────────────────────┘
                              ↓
                   ( Vcc = 5 V,  Vpp = VppH )
                              ↓
                   ( ADDRESS = FIRST LOCATION )
                              ↓
                   ( WRITE PROGRAMME SETUP
                     COMMAND (4040h)    )
                              ↓
                   ( WRITE PROGRAMME DATA )
                              ↓
                   ( WRITE STATUS REGISTER
                     READ COMMAND (7070h) )
                              ↓
                   ( READ STATUS REGISTER )
                              ↓
                         CHECK PROGRAMME        BIT 7. .AND. 15 = "0"
                         STATUS BIT
                              ↓ BIT 7. .AND. 15 = "1"

                         CHECK Vpp              BIT 3. .OR. 11 = "1"
                         ERROR BIT
                              ↓ BIT 3. .OR. 11 = "0"

                         CHECK PROGRAMME        BIT 4. .OR. 12 = "1"
                         ERROR BIT
                              ↓ BIT 4. .OR. 12 = "0"

   ( ADDRESS = NEXT ADDRESS ) ←NO─ LAST ADDRESS?        ( WRITE STATUS REGISTER
                                        ↓ YES             CLEAR COMMAND (5050h) )
                              ( WRITE RESET
                                COMMAND (FFFFh) )
                                        ↓
                              ( Vpp = VppL )
                                        ↓
                    ┌─────────────────────┐      ┌─────────────────────┐
                    │  PROGRAMME PASSED   │      │  PROGRAMME FAILED   │
                    └─────────────────────┘      └─────────────────────┘
```

Note 6. If Vpp error bit is detected, try to programme again at VppH level.
.This is programme algorithm for a memory zone and not for a card.
..OR.:= Logical or   ;   .AND.:= Logical and

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ERASE ALGORITHM
8 bit mode

```
                    ┌─────────────────────────┐
                    │      ERASE START        │
                    └─────────────────────────┘
                    ( V_cc = 5 V,  V_pp = V_ppH )
                    ( ADDRESS=BLOCK  ADDRESS )
                    ( WRITE ERASE SETUP
                      COMMAND (20h) )
                    ( WRITE ERASE COMMAND (D0h) )
                    ( WRITE STATUS REGISTER               ( ERASE SUSPEND
                      READ COMMAND (70h) )                  LOOP ① )
                    ( READ STATUS REGISTER )

           CHECK ERASE      BIT 7 " 0 "        NO
           STATUS BIT  ───────────────►    ERASE        YES
                                          SUSPEND? ────────►
                │ BIT 7 = " 1 "
           CHECK V_pp        BIT 3 = " 1 "
           ERROR BIT  ────────────────────────────────────►
                │ BIT 3 = " 0 "
           CHECK CONTROL     BIT 4 . AND. 5 = " 1 "
           COMMAND BIT ──────────────────────►
                │ BIT 4 . AND. 5 = " 0 "
           CHECK ERASE       BIT 5 = " 1 "
           ERROR BIT  ──────────────►
                │ BIT 5 = " 0 "                ( WRITE STATUS REGISTER CLEAR COMMAND (50h) )
           ( WRITE RESET COMMAND (FFh) )
           ( V_pp = V_ppL )
           ┌─────────────────┐      ┌──────────────┐  ┌──────────────────┐  ┌──────────────┐
           │  ERASE PASSED   │      │ ERASE FAILED │  │ CONTROL COMMAND  │  │ VPP VOLTAGE  │
           └─────────────────┘      └──────────────┘  │ FAILED           │  │ FAILED       │
                                                       └──────────────────┘  └──────────────┘
```
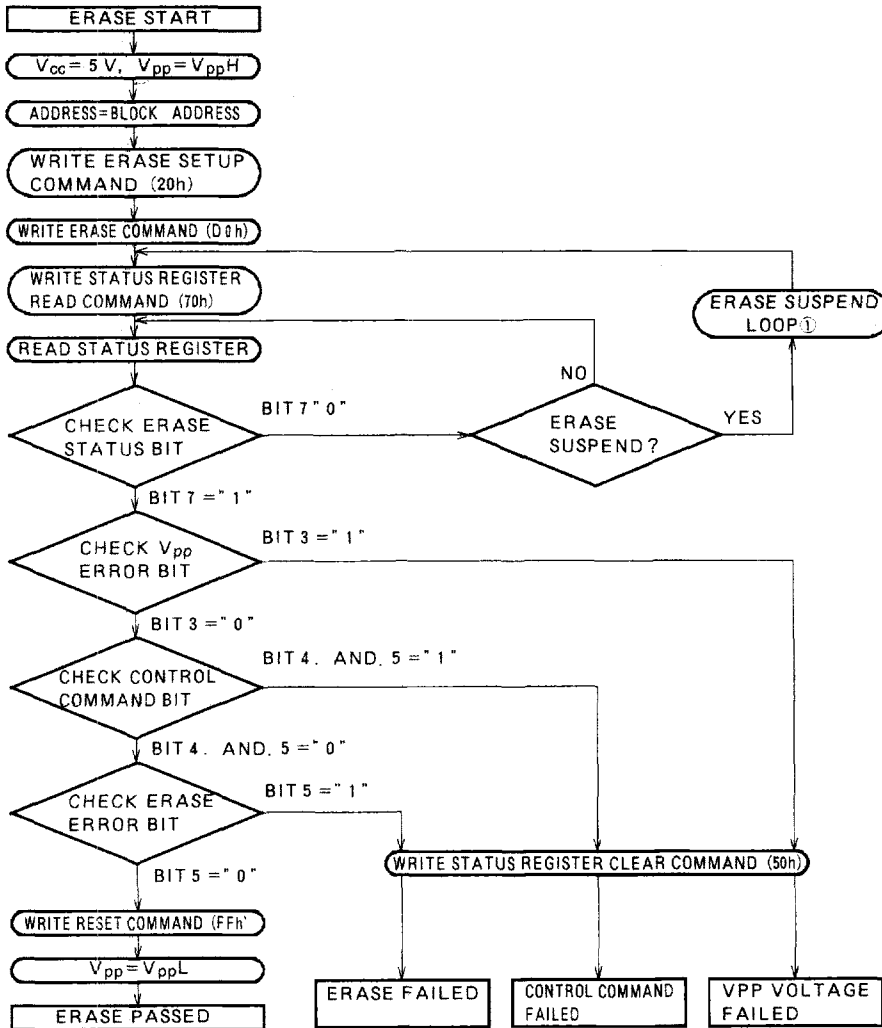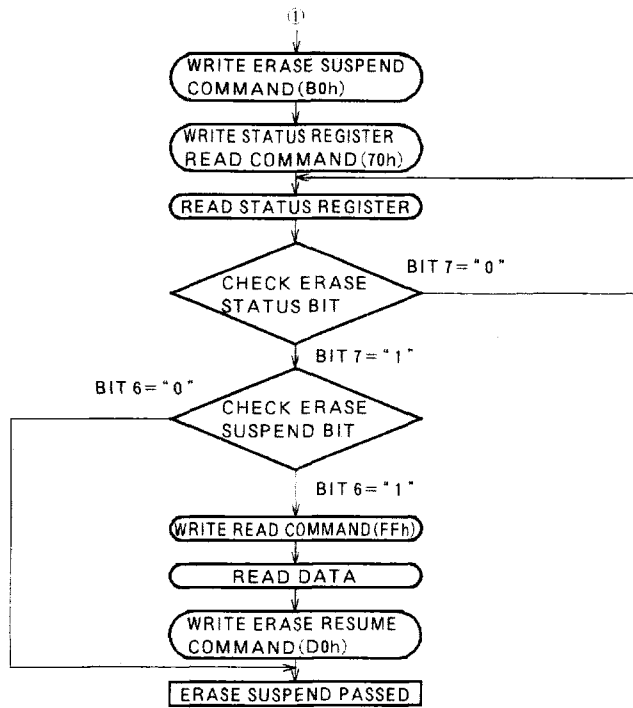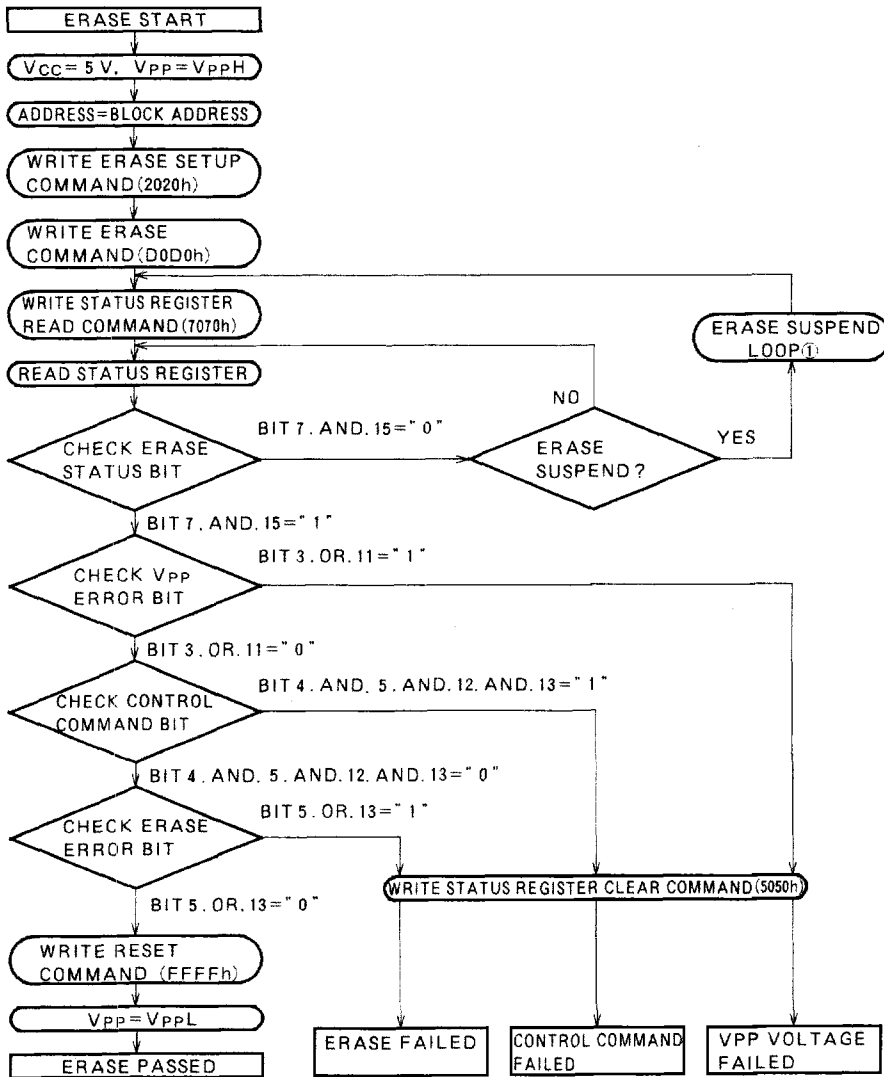
Note 7 . If V_pp error bit is detected, try to programme again at VppH level.
. This is an erase algorithm for a memory block and not for a card.
.. OR. : = Logical or

(1)

WRITE ERASE SUSPEND COMMAND(B0h)

↓

WRITE STATUS REGISTER READ COMMAND(70h)

↓

READ STATUS REGISTER

↓

CHECK ERASE STATUS BIT — BIT 7="0"

BIT 7="1"

↓

CHECK ERASE SUSPEND BIT

BIT 6="0"

BIT 6="1"

↓

WRITE READ COMMAND(FFh)

↓

READ DATA

↓

WRITE ERASE RESUME COMMAND(D0h)

↓

ERASE SUSPEND PASSED

Note 8. Reading data from block other than the suspended block the in zone generating erase suspend.

MITSUBISHI ELECTRIC

ERASE ALGORITHM

16 bit mode

ERASE START

$V_{CC} = 5 V,$ $V_{PP} = V_{PPH}$

ADDRESS = BLOCK ADDRESS

WRITE ERASE SETUP
COMMAND (2020h)

WRITE ERASE
COMMAND (D0D0h)

WRITE STATUS REGISTER
READ COMMAND (7070h)

READ STATUS REGISTER

ERASE SUSPEND
LOOP①

CHECK ERASE
STATUS BIT

BIT 7. AND. 15 = "0"

ERASE
SUSPEND ?

NO

YES

BIT 7. AND. 15 = "1"

CHECK V_PP
ERROR BIT

BIT 3. OR. 11 = "1"

BIT 3. OR. 11 = "0"

CHECK CONTROL
COMMAND BIT

BIT 4. AND. 5. AND. 12. AND. 13 = "1"

BIT 4. AND. 5. AND. 12. AND. 13 = "0"

CHECK ERASE
ERROR BIT

BIT 5. OR. 13 = "1"

WRITE STATUS REGISTER CLEAR COMMAND (5050h)

BIT 5. OR. 13 = "0"

WRITE RESET
COMMAND (FFFFh)

$V_{PP} = V_{PPL}$

ERASE PASSED

ERASE FAILED

CONTROL COMMAND
FAILED

VPP VOLTAGE
FAILED

Note 9 . If V_PP error bit is detected, try to programme again at V_PPH level.
. This is an erase algorithm for a memory block and not for a card.
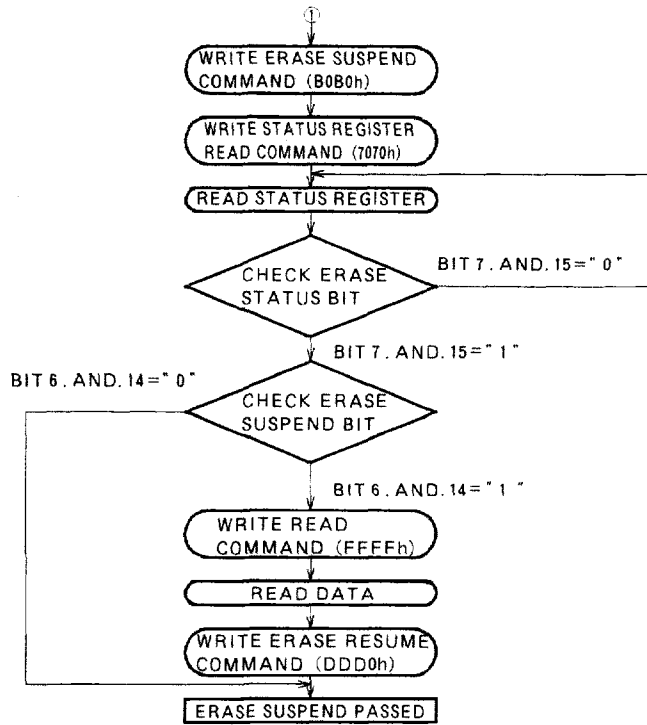. . OR. : = Logical or   ; . AND. : = Logical and

```
                        ①
              ┌─────────────────────────┐
             (  WRITE ERASE SUSPEND      )
              (  COMMAND (B0B0h)         )
              └─────────────────────────┘
              ┌─────────────────────────┐
             (  WRITE STATUS REGISTER    )
              (  READ COMMAND (7070h)    )
              └─────────────────────────┘
              ┌─────────────────────────┐
             (   READ STATUS REGISTER    )◄──────────────┐
              └─────────────────────────┘                │
                         │                                │
                    ╱─────────╲         BIT 7 . AND. 15=" 0"  │
                   ╱ CHECK ERASE╲───────────────────────────┘
                   ╲  STATUS BIT ╱
                    ╲─────────╱
                         │  BIT 7 . AND. 15=" 1 "
   BIT 6 . AND. 14=" 0" │
   ┌─────────────────╱─────────╲
   │                ╱ CHECK ERASE ╲
   │                ╲ SUSPEND BIT ╱
   │                 ╲─────────╱
   │                      │  BIT 6 . AND. 14=" 1 "
   │         ┌─────────────────────────┐
   │        (   WRITE READ              )
   │         (   COMMAND (FFFFh)        )
   │         └─────────────────────────┘
   │         ┌─────────────────────────┐
   │        (      READ DATA            )
   │         └─────────────────────────┘
   │         ┌─────────────────────────┐
   │        (  WRITE ERASE RESUME       )
   │         (  COMMAND (DDD0h)         )
   │         └─────────────────────────┘
   │                      │
   └──────────────────────┤
              ┌─────────────────────────┐
              │  ERASE SUSPEND PASSED    │
              └─────────────────────────┘
```

Note 10. Reading data from block other than the suspended block the in zone generating erase suspend.
   . AND. : = Logical and

ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Conditions	Ratings	Unit
V_{CC}	V_{CC} Supply voltage		$-0.5 \sim 6.0$	V
V_{PP}	V_{PP} Supply voltage	With respect to GND	$-0.5 \sim 14.0$	V
V_I	Input voltage		$-0.3 \sim V_{CC}+0.3$	V
V_O	Output voltage		$0 \sim V_{CC}$	V
T_{opr}	Operating temperature	Read/Write Operation	$0 \sim 70$	℃
T_{stg}	Storage temperature		$-40 \sim 80$	℃

RECOMMENDED OPERATING CONDITIONS (Ta = 0 ~55℃, unless otherwise noted)

Symbol	Parameter		Limits			Unit
			Min.	Typ.	Max.	
V_{CC}	V_{CC} supply voltage		4.75	5.0	5.25	V
V_{PPL}	V_{PP} supply voltage during READ only mode		0	V_{CC}	$V_{CC}+1.0$	V
V_{PPH}	V_{PP} supply voltage during READ WRITE mode		11.4	12.0	12.6	V
V_{IH}	High input voltage		2.4		V_{CC}	V
V_{IL}	Low input voltage		0		0.8	V
N_{ACT}	Number of simultaneous activated memory zones/blocks	Programme			1	Zone
		Erase			1	Block

ELECTRICAL CHARACTERISTICS (T$_a$=0~55℃, V$_{CC}$= 5 V ± 5 %, V$_{PP}$=V$_{PPL}$ or V$_{PPH}$, unless otherwise noted)

Symbol	Parameter	Conditions		Limits			Unit
				Min.	Typ.	Max.	
V$_{OH}$	High output voltage	I$_{OH}$ = −0.1mA, BVDn		2.4			V
		I$_{OH}$ = −1.0mA, Other outputs		2.4			
V$_{OL}$	Low output voltage	I$_{OL}$ =2mA		0		0.4	V
I$_{IH}$	High input current	V$_I$ = V$_{CC}$ V				10	µ A
I$_{IL}$	Low input current	V$_I$ = 0 V	$\overline{CE1}$, $\overline{CE2}$, $\overline{OE}$, $\overline{WE}$, $\overline{REG}$	−10		−70	µ A
			Other inputs			−10	
I$_{OZH}$	High output current in off state	$\overline{CE1}$ = $\overline{CE2}$ = V$_{IH}$ or $\overline{OE}$ = V$_{IH}$, V$_O$(Dm) = V$_{CC}$				10	µ A
I$_{OZL}$	Low output current in off state	$\overline{CE1}$ = $\overline{CE2}$ = V$_{IH}$ or $\overline{OE}$ = V$_{IH}$, V$_O$(Dm) = 0 V				−10	µ A
I$_{CC1·1}$	Active V$_{CC}$ supply current 1	$\overline{CE1}$ = $\overline{CE2}$ = V$_{IL}$, Other inputs = V$_{IH}$ or V$_{IL}$, Outputs = open			100	200	mA
I$_{CC1·2}$	Active V$_{CC}$ supply current 2	$\overline{CE1}$ = $\overline{CE2}$ ≦0.2V, Other inputs≦0.2V or ≧V$_{CC}$ −0.2V, Outputs = open			90	180	mA
I$_{CC2·1}$	Standby V$_{CC}$ supply current 1	$\overline{CE1}$ = $\overline{CE2}$ = V$_{IH}$, Other inputs = V$_{IH}$ or V$_{IL}$	2 MB			9.0	mA
			4 MB			13	
			8 MB			21	
			10MB			25	
			16MB			37	
			20MB			45	
I$_{CC2·2}$	Standby V$_{CC}$ supply current 2	$\overline{CE1}$ = $\overline{CE2}$ ≧V$_{CC}$ −0.2V, Other inputs≦0.2V or ≧V$_{CC}$ −0.2V	2 MB		0.1	1.2	mA
			4 MB		0.2	1.4	
			8 MB		0.4	1.8	
			10MB		0.5	2.0	
			16MB		0.7	2.6	
			20MB		0.8	3.0	
I$_{PP1}$	V$_{PP}$ supply current 1 (each V$_{PP}$ pin)	V$_{PP}$ = V$_{PPL}$ ≦V$_{CC}$	2 MB		10	20	µ A
			4 MB		20	30	
			8 MB		30	50	
			10MB		40	60	
			16MB		50	90	
			20MB		70	110	
I$_{PP2}$	V$_{PP}$ supply current 2 (each V$_{PP}$ pin)	V$_{PP}$ = V$_{PPH}$ (standby, read)	2 MB			0.3	mA
			4 MB			0.5	
			8 MB			0.9	
			10MB			1.1	
			16MB			1.7	
			20MB			2.1	
I$_{PP3}$	V$_{PP}$ supply current 3 (each V$_{PP}$ pin)	V$_{PP}$ = V$_{PPH}$ (programme, erase)			10	35	mA

Note 11. Currents flowing into the card are taken as positive (unsigned).
Typical values are measured at V$_{CC}$ = 5.0V, V$_{PPL}$ = 5 V, V$_{PPH}$ = 12V, Ta = 25℃.
The card consumes active current at programming, erasure even if both $\overline{CE1}$ and $\overline{CE2}$ are high level.

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CAPACITANCE

Symbol	Parameter	Test conditions	Limits			Unit
			Min.	Typ.	Max.	
C_i	Input capacitance	$V_i = GND$, $v_i = 25mVrms$, $f = 1 MHz$, $T_a = 25°C$			45	pF
C_O	Output capacitance	$V_O = GND$, $v_o = 25mVrms$, $f = 1 MHz$, $T_a = 25°C$			45	pF

Note 12 : These parameters are not 100% tested.

SWITCHING CHARACTERISTICS (COMMON MEMORY)

Read Cycle ($T_a = 0 \sim 55°C$, $V_{CC} = 5 V \pm 5 \%$, $V_{PP} = V_{PPL}$ or V_{PPH}, unless otherwise noted)

Symbol	Parameter	Limits			Unit
		Min.	Typ.	Max.	
tRC	Read cycle time	200			ns
ta(A)	Address access time			200	ns
ta(CE)	Card enable access time			200	ns
ta(OE)	Output enable access time			100	ns
tdis(CE)	Output disable time (from $\overline{CE}$)			90	ns
tdis(OE)	Output disable time (from $\overline{OE}$)			90	ns
ten(CE)	Output enable time (from $\overline{CE}$)	5			ns
ten(OE)	Output enable time (from $\overline{OE}$)	5			ns
tV(A)	Data valid time after address change	0			ns

TIMING REQUIREMENTS (COMMON MEMORY)
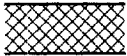
Write Cycle ($T_a = 0 \sim 55°C$, $V_{CC} = 5 V \pm 5 \%$, $V_{PP} = V_{PPH}$, unless otherwise noted)

Symbol	Parameter	Limits			Unit
		Min.	Typ.	Max.	
tWC	Write cycle time	200			ns
tAS	Address setup time	20			ns
tAH	Address hold time	30			ns
tDS	Data setup time	60			ns
tDH	Data hold time	30			ns
tWRR	Write recovery time before read	10			ns
tCS	Card enable setup time before write	20			ns
tCH	Card enable hold time	30			ns
tWP	Write pulse width	120			ns
tWPH	Write pulse width high	40			ns
tDP	Duration of programming operation	6			μs
tDE	Duration of erase operation	300			ms
tVSC	VPP setup time to card enable low	1			μs
tVRW	VPP recovery time to card enable high	150			ns
tASH	Address setup time to write enable high	140			ns

Note 13 : Refer to switching characteritics for read parameters

TIMING DIAGRAM
Common Memory Read

$\overline{REG}$ = "H" level
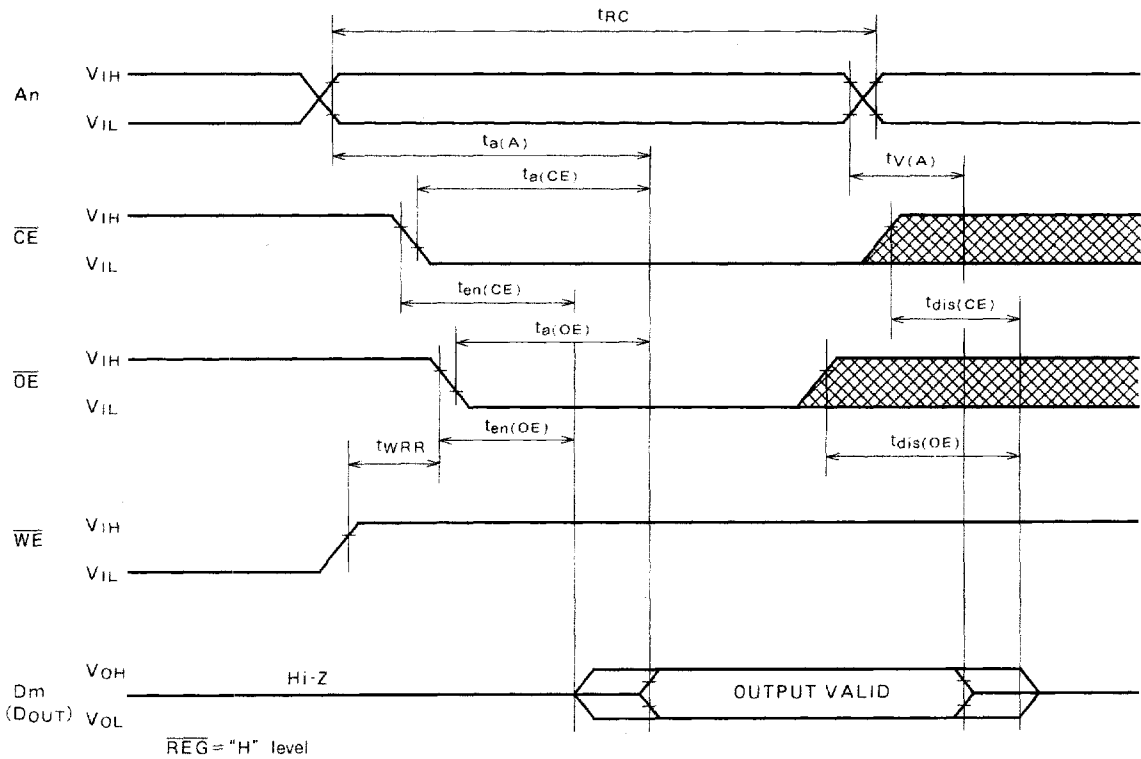
Note 14 : ▓▓▓ Indicates the don't care input.

MITSUBISHI ELECTRIC

TIMING DIAGRAM (COMMON MEMORY)
Programme Mode

$\overline{REG}$ = "H" level
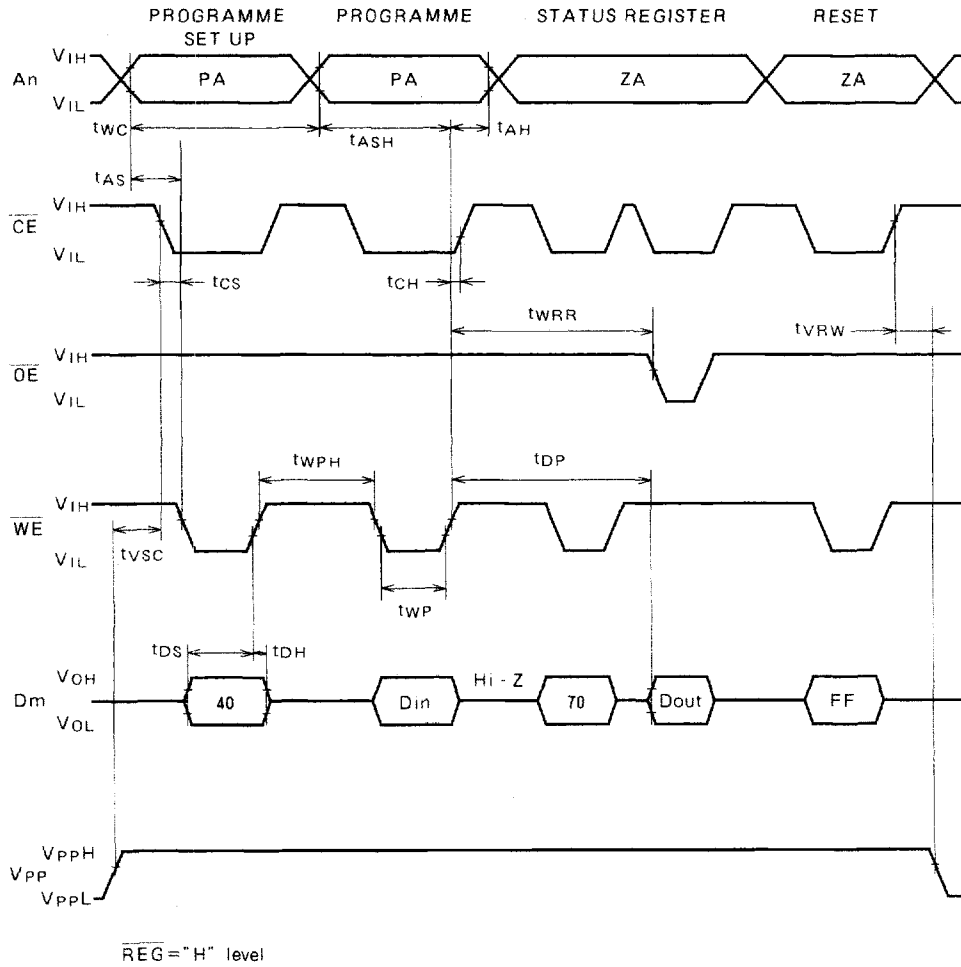
TIMING DIAGRAM (COMMON MEMORY)
Erase Mode

$\overline{REG}$ = "H" level

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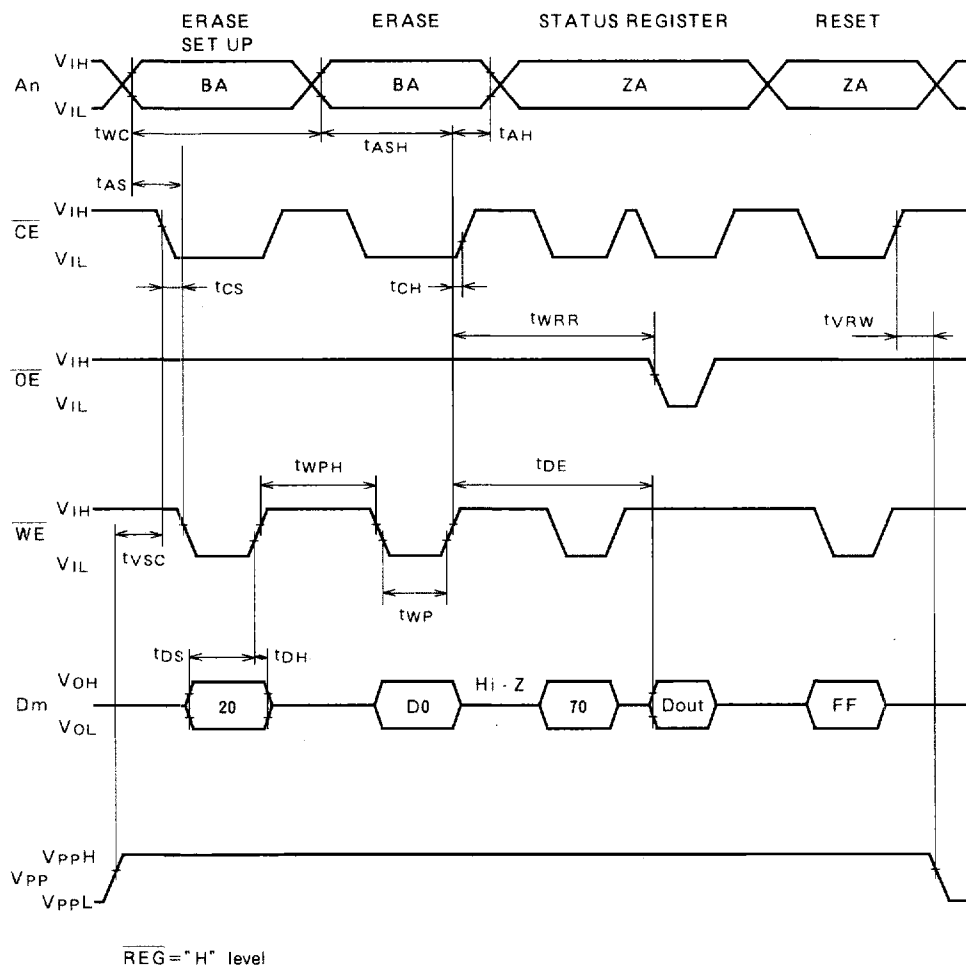
SWITCHING CHARACTERISTICS

Read Cycle ($T_a = 0 \sim 55°C$, $V_{CC} = 5\,V \pm 5\,\%$, $V_{PP} = V_{CC}$, unless otherwise noted)

Symbol	Parameter	Limits			Unit
		Min.	Typ.	Max.	
t_{RCR}	Read cycle time	300			ns
$t_{a(A)R}$	Address access time			300	ns
$t_{a(CE)R}$	Card enable access time			300	ns
$t_{a(OE)R}$	Output enable access time			150	ns
$t_{dis(CE)R}$	Output disable time (from $\overline{CE}$)			100	ns
$t_{dis(OE)R}$	Output disable time (from $\overline{OE}$)			100	ns
$t_{en(CE)R}$	Output enable time (from $\overline{CE}$)	5			ns
$t_{en(OE)R}$	Output enable time (from $\overline{OE}$)	5			ns
$t_{V(A)R}$	Data valid time after address change	0			ns

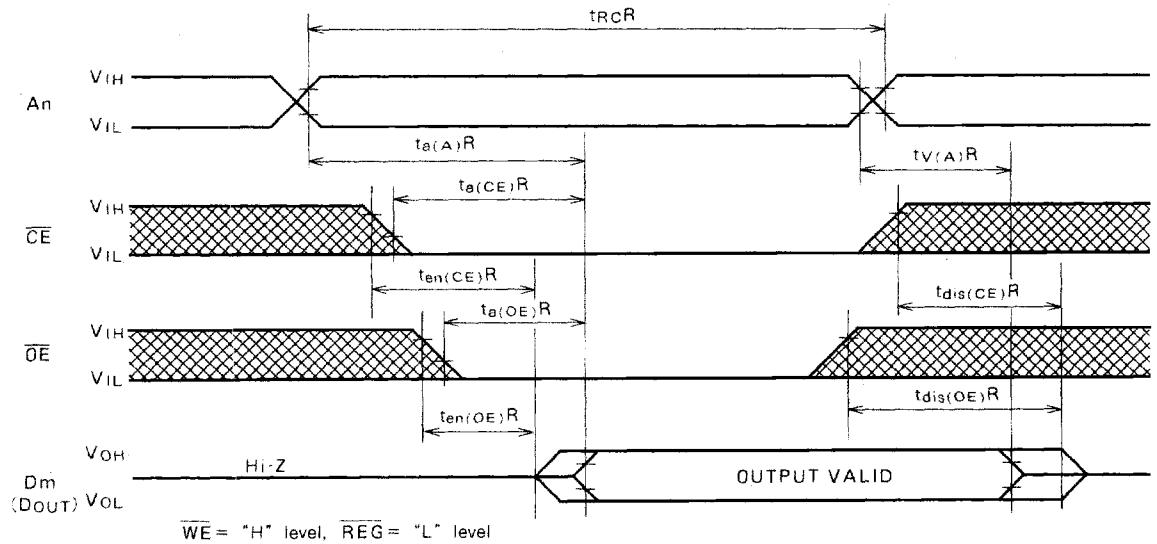## TIMING REQUIREMENTS (ATTRIBUTE MEMORY)

Write Cycle ($T_a = 0 \sim 55°C$, $V_{CC} = 5V \pm 5\%$, $V_{PP} = V_{CC}$, unless otherwise noted)

Symbol	Parameter	Limits			Unit
		Min.	Typ.	Max.	
$t_{AS}R$	Address setup time	30			ns
$t_{AH}R$	Address hold time	30			ns
$t_{CS}R$	$\overline{CE}$ setup time	40			ns
$t_{CH}R$	$\overline{CE}$ hold time	30			ns
$t_{DS}R$	Data setup time	120			ns
$t_{DH}R$	Data hold time	40			ns
$t_{OES}R$	$\overline{OE}$ setup time	30			ns
$t_{OEH}R$	$\overline{OE}$ hold time	40			ns
$t_{WP}R$	Write pulse width	170			ns
$t_{DL}R$	Data latch time	120			ns
$t_{BLC}R$	Byte load cycle time	0.3		30	μs
$t_{WC}R$	Write cycle time	10			ms
$t_{en(OE)}R$	Output enable time (from $\overline{OE}$)	5			ns
$t_{dis(OE)}R$	Output disable time (from $\overline{OE}$)	0		100	ns

TIMING DIAGRAM (Attribute Memory)
Read

$\overline{WE} = $ "H" level, $\overline{REG} = $ "L" level

Byte Write

$\overline{REG}$ = "L" level

Page Mode Write

An (A6~A13) VIH / VIL

An (A0~A5) VIH / VIL   0   2   4   60   62

$\overline{CE}$ VIH / VIL

$\overline{WE}$ VIH / VIL

tcsR twPR tDLR tCHR

tASR tAHR tBLCR

tOESR tOEHR

$\overline{OE}$ VIH / VIL

tDSR tDHR

Dm (DIN) VIH / VIL   Hi-Z

tdis(OE)R   ten(OE)R

Dm (DOUT) VOH / VOL   Hi-Z

$\overline{REG}$ = "L" level
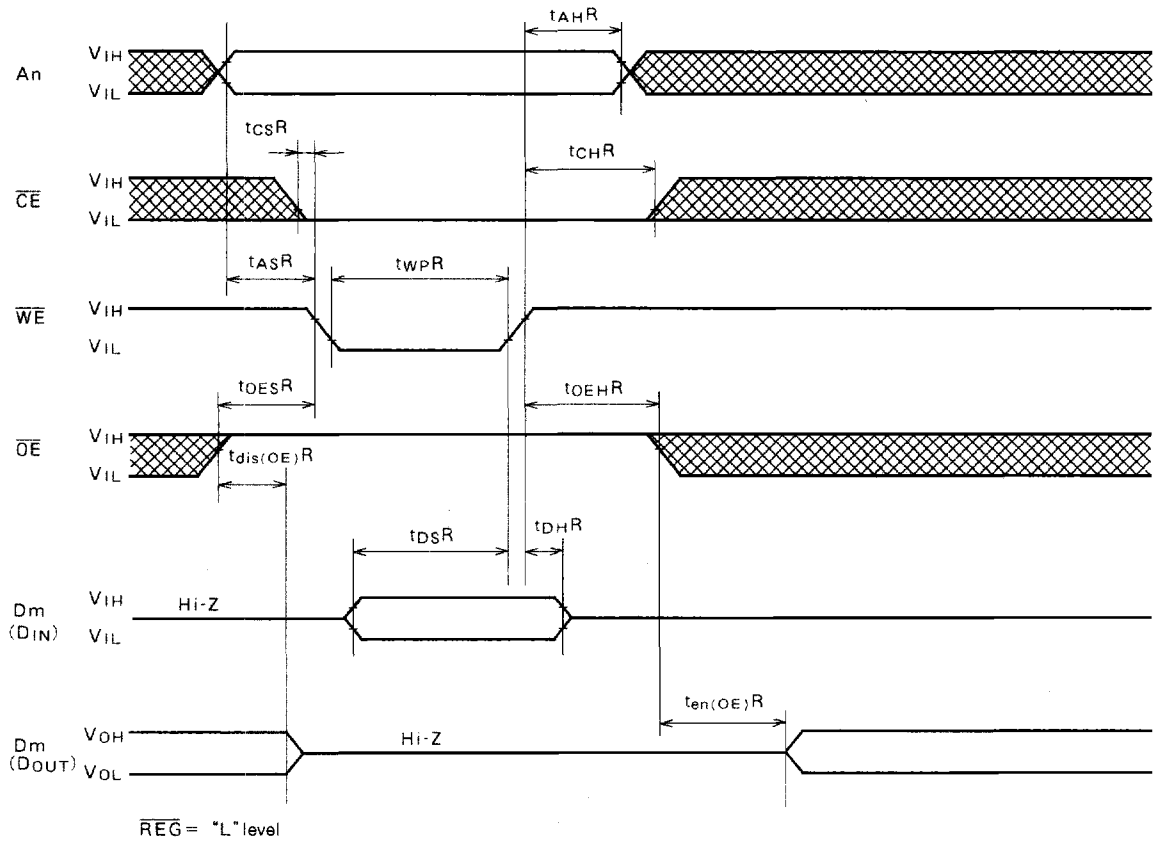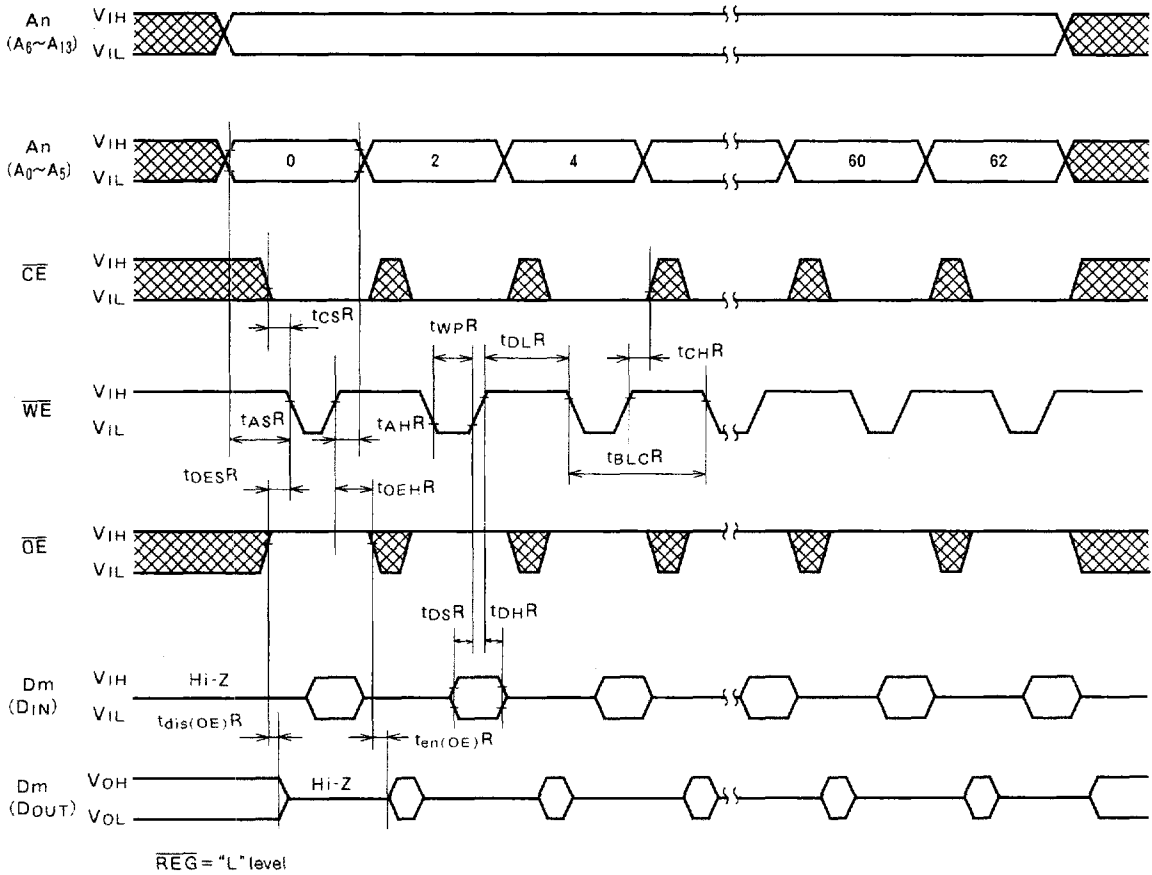
Note 15 : AC Test Conditions
   Input pulse levels : $V_{IL} = 0.4V$, $V_{IH} = 2.8V$
   Input pulse rise, fall time : $t_r = t_f = 10ns$
   Reference voltage
      Input : $V_{IL} = 0.8V$, $V_{IH} = 2.4V$
      Output : $V_{OL} = 0.8V$, $V_{OH} = 2.0V$
         (t_{en} and t_{dis} are measured when output voltage is ±500mV from steady state.)
      Load :   100pF + 1 TTL gate
                5pF + 1 TTL gate (at t_{en} and t_{dis} measuring)

16 : The data write is performed during the interval when both $\overline{CE}$ and $\overline{WE}$ are "L" level.

17 : Do not apply inverted phase signal externally when Dm pin is in output mode.

18 : $\overline{CE}$ is indicated as follows :
      Read A/Write A : $\overline{CE} = \overline{CE1} = \overline{CE2}$
      Read B/Write B : $\overline{CE} = \overline{CE1}$, $\overline{CE2}$ = "H" level
      Read C/Write C : $\overline{CE} = \overline{CE2}$, $\overline{CE1}$ = "H" level

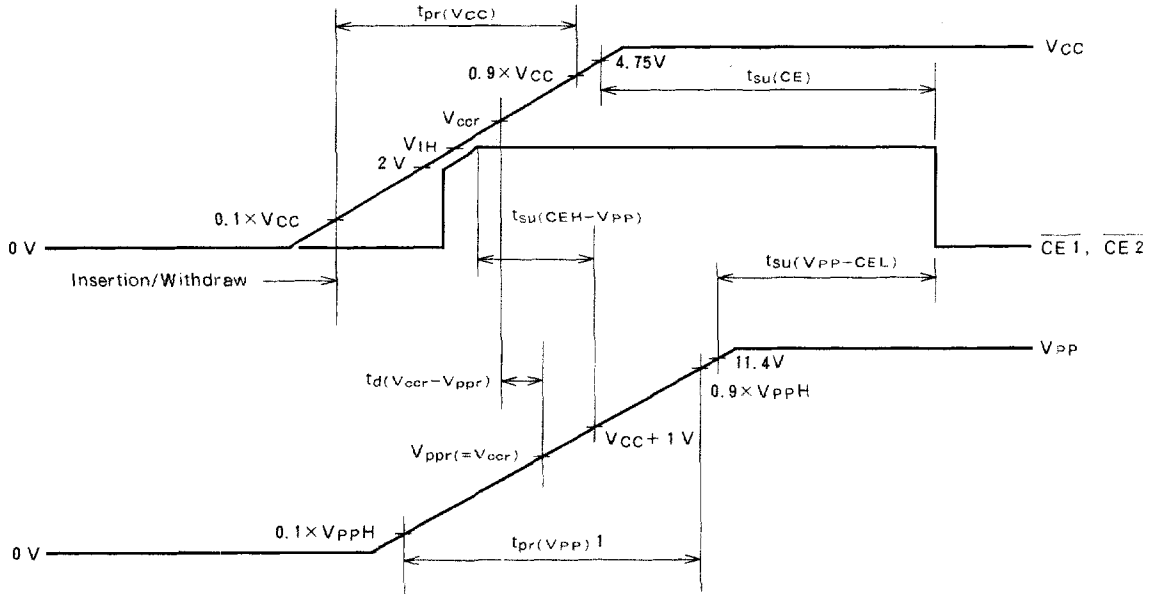MITSUBISHI ELECTRIC

RECOMMENDED POWER UP/DOWN CONDITIONS ($T_a = 0 \sim 55°C$, unless otherwise noted)

Symbol	Parameter	Conditions	Limits			Unit
			Min.	Typ.	Max.	
Vi (CE)	$\overline{CE}$ input voltage	$0\,V \leq V_{CC} < 2\,V$	0		V_{CC}	V
		$2\,V \leq V_{CC} < 2.4\,V$	V_{CC}-0.1	V_{CC}	V_{CC}+0.1	V
		$2.4V \leq V_{CC}$	2.4		V_{CC}+0.1	V
$t_{su(CE)}$	$\overline{CE}$ setup time		1			ms
$t_{rec(CE)}$	$\overline{CE}$ recovery time		1			μs
$t_{pr(VCC)}$	V_{CC} rise time		0.1		300	ms
$t_{pf(VCC)}$	V_{CC} fall time		3		300	ms
$t_{su(CEH-VPP)}$	Setup time before V_{PP} rise		0.15			μs
$t_{su(VPP-CEL)}$	Setup time after V_{PP} rise		1			μs
$t_{rec(CEH-VPP)}$	Recovery time before V_{PP} fall		0.15			μs
$t_{rec(VPP-CEL)}$	Recovery time after V_{PP} fall		1			μs
$t_{pr(VPP)}1$	V_{PP} rise time 1		0.24		300	ms
$t_{pf(VPP)}1$	V_{PP} fall time 1		7.2		300	ms
$t_{pr(VPP)}2$	V_{PP} rise time 2		0.1		300	ms
$t_{pf(VPP)}2$	V_{PP} fall time 2		3		300	ms
$t_{d(VCCr-VPPr)}$	$V_{PP}r$ delay time after $V_{CC}r$	$0\,V \leq V_{CC} \leq 4.75V$	0			μs
$t_{d(VPPf-VCCf)}$	$V_{CC}f$ delay time after $V_{PP}f$	$0\,V \leq V_{CC} \leq 4.75V$	0			μs

POWER UP TIMING DIAGRAM

V_{PP} 1 step

$t_{pr(VCC)}$

V_{CC}

0.9×V_{CC} 4.75V

$t_{su(CE)}$

V_{ccr}

V_{IH}

2 V

0.1×V_{CC}

$t_{su(CEH-VPP)}$

0 V

$\overline{CE\,1}$, $\overline{CE\,2}$

$t_{su(VPP-CEL)}$

Insertion/Withdraw

V_{PP}

11.4V

$t_{d(Vccr-Vppr)}$

0.9×$V_{PP}H$

$V_{ppr(=Vccr)}$ V_{CC}+1 V

0.1×$V_{PP}H$

$t_{pr(VPP)}$1

0 V

V_{PP} 2 steps

$t_{pr(VCC)}$

V_{CC}

0.9×V_{CC} 4.75V

$t_{su(CE)}$

V_{ccr}

V_{IH}

2 V

0.1×V_{CC}

0 V

$\overline{CE\,1}$, $\overline{CE\,2}$

Insertion/Withdraw

$t_{su(CEH-VPP)}$ $t_{su(VPP-CEL)}$

$V_{PP}H$

V_{PP}

11.4V

0.9×$V_{PP}H$

$t_{d(Vccr-Vppr)}$

$V_{PP}L$

V_{CC}+1 V

$V_{ppr(=Vccr)}$

$t_{pr(VPP)}$2

0 V

Note 19 : V_{ccr} and $V_{ppr}(=V_{ccr})$ indicates any voltage when V_{CC} voltage is in the range of 0 V to 4.75V

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FLASH MEMORY CARDS

POWER DOWN TIMING DIAGRAM

V_{PP} 1 step

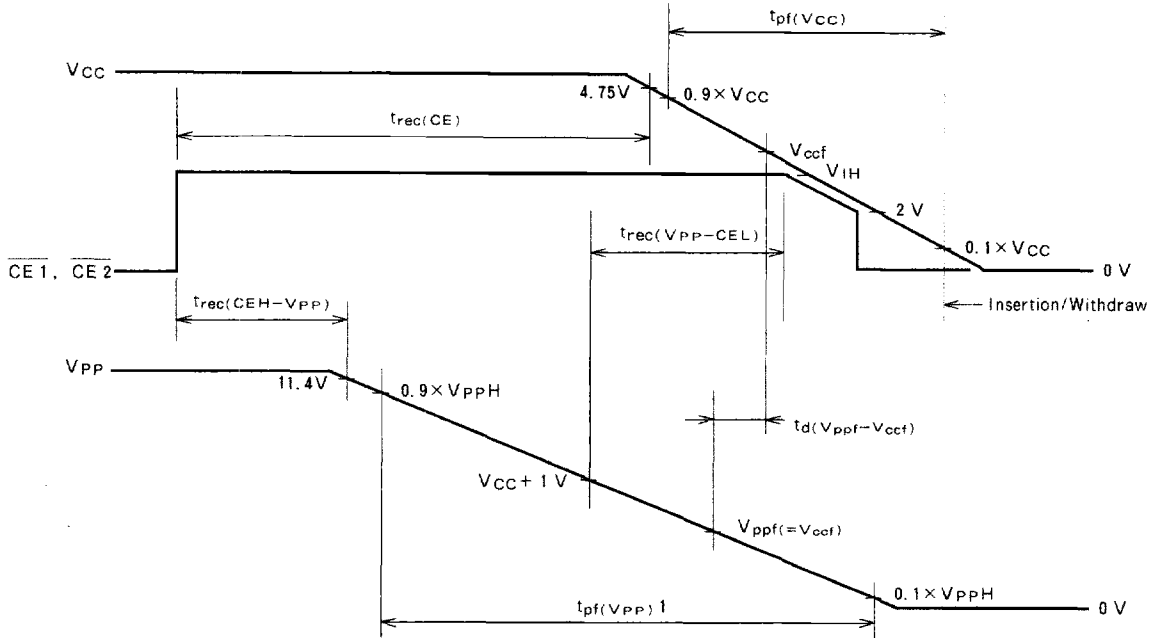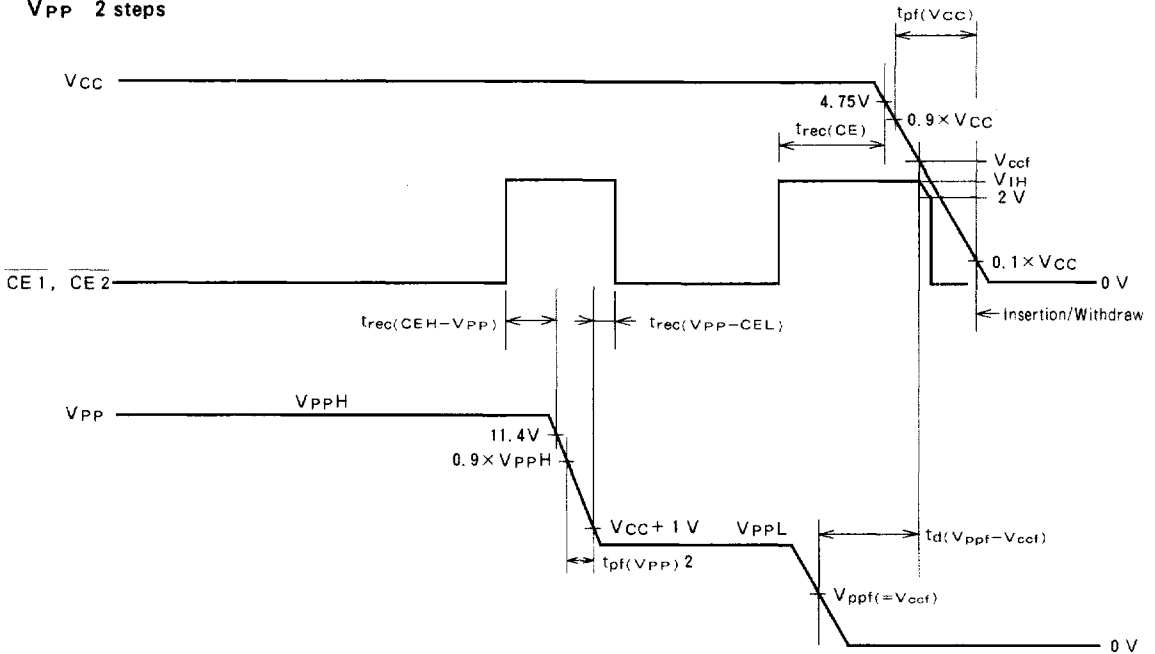### V_{PP} 2 steps

Note 20 : V_{ccr} and $V_{ppr}(=V_{ccr})$ indicates any voltage when V_{CC} voltage is in the range of 0 V to 4.75V

BLOCK PROGRAM/ERASE TIME

Parameters	Limits		Unit
	Typ.	Max.	
Block erase time	1. 6	10	s
Block program time	0. 6	2. 1	s

Note 21: At Ta = 25℃, V_{pp} = 12V

22: Byte/word program time is about 9 μs (typical), but not guaranteed.

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