

*1x1Mx32bit DRAM Card*  
*2x1Mx32bit DRAM Card*

**MF14M1-J17ATXX**  
**MF18M1-J17ATXX**

Connector Type

*Two-piece 88-pin*

**DESCRIPTION**

These DRAM CARDS are developed based on JEIDA DRAM CARD GUIDELINE Ver 2.0. These cards are made using industry standard 1Mx4 Dynamic RAM and interface IC's in TSOP.

- 88pin 2 piece connector type.
- RAS only refresh mode. CAS before RAS refresh mode and Page mode functions are available.
- Self refresh mode is available. (128ms/1024cycle)

**FEATURES**

- Operating Voltage :  $V_{cc} = 3V \pm 5\%$
- All inputs except RAS inputs are buffered.
- Standard card size : 54 mm (W) x 85.6 mm (L) x 3.3mm (T)

**APPLICATIONS**

Main/expansion memory unit for Personal Computer, Laser-Printer, FAX etc.

**PRODUCT LIST**

Product No.	Item Type name	Memory capacity	Data bus width (bits)	Access time (tRAC) (ns)	Connector type	Number of pins	Outline drawing
No. 1	MF14M1-J17ATXX	4 MB	32	70	Two-piece	88	88P-002
No. 2	MF18M1-J17ATXX	8 MB					

DYNAMIC RAM CARDS

PIN ASSIGNMENT (No.1)

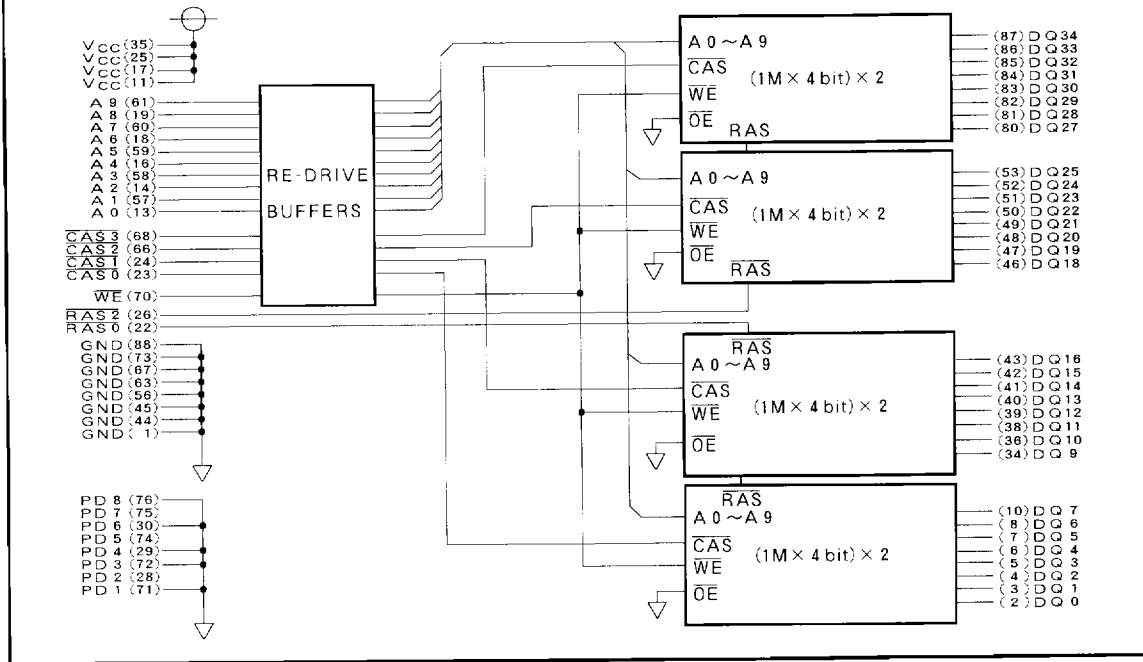
Pin No.	Symbol	Function	Pin No.	Symbol	Function
1	GND	Ground	45	GND	Ground
2	DQ 0	Data I/O	46	DQ18	Data I/O
3	DQ 1		47	DQ19	
4	DQ 2		48	DQ20	
5	DQ 3		49	DQ21	
6	DQ 4		50	DQ22	
7	DQ 5		51	DQ23	
8	DQ 6		52	DQ24	
9	N.C.		No connection	53	
10	DQ 7	Data I/O	54	N.C.	
11	V <sub>cc</sub>	Power supply voltage	55	N.C.	Ground
12	N.C.	No connection	56	GND	
13	A 0	Address input	57	A 1	Address input
14	A 2		58	A 3	
15	N.C.		No connection	59	
16	A 4	Address input	60	A 7	No connection
17	V <sub>cc</sub>	Power supply voltage	61	A 9	
18	A 6	Address input	62	N.C.	No connection
19	A 8		63	GND	Ground
20	N.C.	No connection	64	N.C.	No connection
21	N.C.		65	N.C.	No connection
22	RAS 0	Row address strobe 0	66	CAS 2	Column address strobe 2
23	CAS 0	Column address strobe 0	67	GND	Ground
24	CAS 1	Column address strobe 1	68	CAS 3	Column address strobe 3
25	V <sub>cc</sub>	Power supply voltage	69	N.C.	No connection
26	RAS 2	Row address strobe 2	70	WE	Write enable
27	N.C.	No connection	71	PD 1 (GND)	Presence detect 1
28	PD 2 (N.C.)	Presence detect 2	72	PD 3 (GND)	Presence detect 3
29	PD 4 (GND)	Presence detect 4	73	GND	Ground
30	PD 6 (GND)	Presence detect 6	74	PD 5 (N.C.)	Presence detect 5
31	N.C.	No connection	75	PD 7 (N.C.)	Presence detect 7
32	N.C.		76	PD 8 (GND)	Presence detect 8
33	N.C.	Data I/O	77	N.C.	No connection
34	DQ 9		78	N.C.	
35	V <sub>cc</sub>	Power supply voltage	79	N.C.	Data I/O
36	DQ10	Data I/O	80	DQ27	
37	N.C.	No connection	81	DQ28	
38	DQ11	Data I/O	82	DQ29	
39	DQ12		83	DQ30	
40	DQ13		84	DQ31	
41	DQ14		85	DQ32	
42	DQ15		86	DQ33	
43	DQ16		87	DQ34	
44	GND		Ground	88	GND

## DYNAMIC RAM CARDS

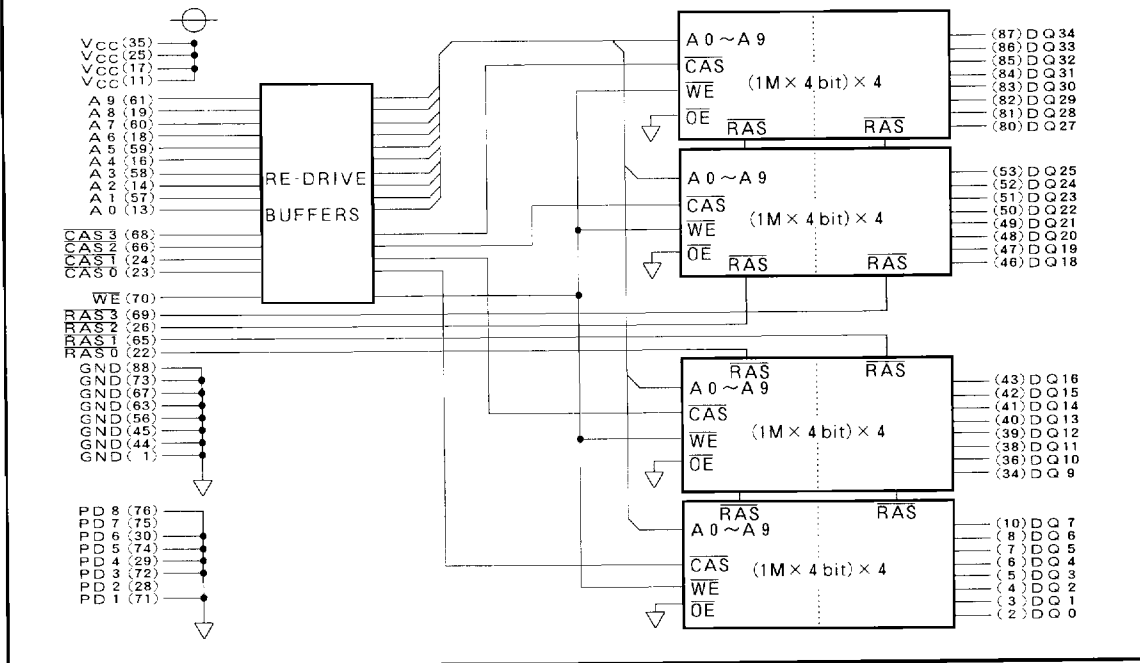
## PIN ASSIGNMENT (No.2)

Pin No.	Symbol	Function	Pin No.	Symbol	Function	
1	GND	Ground	45	GND	Ground	
2	DQ 0	Data I/O	46	DQ18	Data I/O	
3	DQ 1		47	DQ19		
4	DQ 2		48	DQ20		
5	DQ 3		49	DQ21		
6	DQ 4		50	DQ22		
7	DQ 5		51	DQ23		
8	DQ 6		52	DQ24		
9	N.C.		No connection	53		DQ25
10	DQ 7	Data I/O	54	N.C.	No connection	
11	Vcc	Power supply voltage	55	N.C.		
12	N.C.	No connection	56	GND	Ground	
13	A 0	Address input	57	A 1	Address input	
14	A 2		58	A 3		
15	N.C.		No connection	59		A 5
16	A 4		Address input	60		A 7
17	Vcc	Power supply voltage	61	A 9	No connection	
18	A 6	Address input	62	N.C.		
19	A 8		Address input	63	GND	Ground
20	N.C.	No connection	64	N.C.	No connection	
21	N.C.		No connection	65	RAS 1	Row address strobe 1
22	RAS 0	Row address strobe 0	66	CAS 2	Column address strobe 2	
23	CAS 0	Column address strobe 0	67	GND	Ground	
24	CAS 1	Column address strobe 1	68	CAS 3	Column address strobe 3	
25	Vcc	Power supply voltage	69	RAS 3	Row address strobe 3	
26	RAS 2	Row address strobe 2	70	WE	Write enable	
27	N.C.	No connection	71	PD 1 (GND)	Presence detect 1	
28	PD 2 (N.C.)	Presence detect 2	72	PD 3 (GND)	Presence detect 3	
29	PD 4 (GND)	Presence detect 4	73	GND	Ground	
30	PD 6 (GND)	Presence detect 6	74	PD 5 (GND)	Presence detect 5	
31	N.C.	No connection	75	PD 7 (N.C.)	Presence detect 7	
32	N.C.		No connection	76	PD 8 (GND)	Presence detect 8
33	N.C.		No connection	77	N.C.	No connection
34	DQ 9	Data I/O	78	N.C.		
35	Vcc	Power supply voltage	79	N.C.	Data I/O	
36	DQ10	Data I/O	80	DQ27		
37	N.C.	No connection	81	DQ28		
38	DQ11	Data I/O	82	DQ29		
39	DQ12		83	DQ30		
40	DQ13		84	DQ31		
41	DQ14		85	DQ32		
42	DQ15		86	DQ33		
43	DQ16		87	DQ34		
44	GND	Ground	88	GND	Ground	

BLOCK DIAGRAM (No.1)



BLOCK DIAGRAM (No.2)



DYNAMIC RAM CARDS

FUNCTION TABLE

Operation	Input					input/output		Refresh	Note
	RAS	CAS	WE	Row Address	Column Address	input	output		
Read	ACT	ACT	NAC	APD	APD	OPD	VLD	YES	Page mode identical
Early write	ACT	ACT	ACT	APD	APD	VLD	OPN	YES	
RAS-only refresh	ACT	NAC	DNC	APD	DNC	DNC	OPN	YES	
CAS before RAS refresh	ACT	ACT	NAC	DNC	DNC	DNC	OPN	YES	
Self refresh	ACT	ACT	NAC	DNC	DNC	DNC	OPN	YES	
Standby	NAC	DNC	DNC	DNC	DNC	DNC	OPN	NO	

Note 1 : ACT : active, NAC : nonactive, DNC : don't care, VLD : valid, APD : applied, OPN : open  
 Odd numbered RAS signals (RAS1, RAS3) and even numbered RAS signals (RAS0, RAS2) should not be active at the same time during Read and Early Write cycles.  
 This comment does not apply to MF14M1-J17ATXXseries cards.

ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Conditions	Ratings	Unit
V <sub>CC</sub>	Supply voltage		-0.5~4.6	V
V <sub>I</sub>	Input voltage	With respect to GND	-0.5~4.6	V
V <sub>O</sub>	Output voltage		-0.5~4.6	V
I <sub>O</sub>	Output current		50	mA
P <sub>d</sub>	Power dissipation	T <sub>a</sub> = 25°C	No.1 8	No.2 16 W
T <sub>opr</sub>	Operating temperature		0~55	°C
T <sub>stg</sub>	Storage temperature		-40~80	°C

RECOMMENDED OPERATING CONDITIONS (T<sub>a</sub> = 0 ~ 55°C, unless otherwise noted) : (Note 2)

Symbol	Parameter	Limits			Unit
		Min.	Typ.	Max.	
V <sub>CC</sub>	Supply voltage	3.315	3.3	3.465	V
GND	Supply voltage	0	0	0	V
V <sub>IH</sub>	High input voltage	2.0		V <sub>CC</sub>	V
V <sub>IL</sub>	Low input voltage	0		0.8	V

Note 2 : With respect to GND

DYNAMIC RAM CARDS

**ELECTRICAL CHARACTERISTICS** ( $T_a = 0 \sim 55^\circ\text{C}$ ,  $V_{CC} = 3.3\text{V} \pm 5\%$ ,  $\text{GND} = 0\text{V}$ ) : (Note 3)

Symbol	Parameter	Test condition	Limits			Unit
			Min.	Typ.	Max.	
$V_{OH}$	High-level output voltage	$I_{OH} = -2\text{mA}$	2.4		$V_{CC}$	V
$V_{OL}$	Low-level output voltage	$I_{OL} = 2\text{mA}$	0		0.4	V
$I_{OZ}$	Off-state output current	$0\text{V} \leq V_{out} \leq V_{CC}$	No.1 -10	No.2 -20	No.1 10 No.2 20	$\mu\text{A}$
$I_I$	Input current	$0\text{V} \leq V_{in} \leq V_{CC}$ other input pins = 0V	-40		40	$\mu\text{A}$
$I_{CC1(AV)}$	Average supply current from $V_{CC}$ , operating (Note 4, 5, 6)	$\overline{\text{RAS}}, \overline{\text{CAS}}$ cycling $t_{RC} = t_{WC} = \text{min}$ , output open			No.1 600 No.2 610	mA
$I_{CC2(AV)}$	Supply current from $V_{CC}$ , Standby (Note 7)	$\overline{\text{RAS}} = \overline{\text{CAS}} \geq V_{CC} - 0.2\text{V}$ other input pins $\geq V_{CC} - 0.2\text{V}$ or $\leq 0.2\text{V}$ , output open			No.1 0.5 No.2 0.9	mA
$I_{CC3(AV)}$	Average supply current from $V_{CC}$ , refreshing (Note 4, 6)	$\overline{\text{RAS}}$ cycling, $\overline{\text{CAS}} = V_{IH}$ $t_{RC} = \text{min}$ , output open			No.1 590 No.2 1160	mA
$I_{CC4(AV)}$	Average supply current from $V_{CC}$ , Page-mode (Note 4, 5, 6)	$\overline{\text{RAS}} = V_{IL}$ , $\overline{\text{CAS}}$ cycling $t_{RC} = \text{min}$ , output open			No.1 560 No.2 580	mA
$I_{CC6(AV)}$	Average supply current from $V_{CC}$ , CAS before RAS refresh mode (Note 4, 6)	$\overline{\text{CAS}}$ before $\overline{\text{RAS}}$ refresh cycling $t_{RC} = \text{min}$ , output open			No.1 490 No.2 970	mA
$I_{CC8(AV)}$	Average supply current from $V_{CC}$ , Extended refresh mode (Note 7)	$\overline{\text{CAS}}$ before RAS refresh cycling $\overline{\text{WE}} \geq V_{CC} - 0.2\text{V}$ other input pins $\geq V_{CC} - 0.2\text{V}$ or $\leq 0.2\text{V}$ , output open $t_{RC} = 125\mu\text{s}$ , $t_{RAS} = t_{RAS}(\text{min})$ $\sim 1\mu\text{s}$			No.1 1 No.2 2	mA
$I_{CC9(AV)}$	Average supply current from $V_{CC}$ , Self refresh mode (Note 7)	$\overline{\text{RAS}} = \overline{\text{CAS}} \leq 0.2\text{V}$ , $\overline{\text{WE}} \geq V_{CC} - 0.2\text{V}$ output open			No.1 1 No.2 2	mA

- Note 3 : Current flowing into a CARD is positive, out is negative.  
 4 :  $I_{CC1(AV)}$ ,  $I_{CC3(AV)}$ ,  $I_{CC4(AV)}$  and  $I_{CC6(AV)}$  are dependent on cycle rate.  
 Specified values are obtained at the fastest cycle rate.  
 5 :  $I_{CC1(AV)}$  and  $I_{CC4(AV)}$  are dependent on output loading.  
 Specified values are obtained with the outputs open.  
 6 : Column Address can be changed once or less while  $\overline{\text{RAS}} = V_{IL}$  and  $\overline{\text{CAS}} = V_{IH}$ .

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**SWITCHING CHARACTERISTICS** ( $T_a = 0 \sim 55^\circ\text{C}$ ,  $V_{CC} = 3.3\text{V} \pm 5\%$ ,  $GND = 0\text{V}$ ) : (Note 7)

Symbol	Parameter	Limits		Unit
		Min.	Max.	
tCAC	Access time from CAS (Note 8, 9)		27	ns
tRAC	Access time from RAS (Note 8, 10)		70	ns
tCAA	Column Address access time (Note 8, 11)		42	ns
tOFF	Output disable time after CAS high (Note 12)	0	27	ns

Note 7 : An initial pause of  $500\ \mu\text{s}$  is required after power-up followed by any 8 RAS or RAS/CAS cycles before proper device operation is achieved.

Note that RAS may be cycled during the initial pause. And any 8 RAS or RAS/CAS cycles are required after prolonged periods of RAS inactivity before proper device operation is achieved.

8 : Measured with a load circuit equivalent to  $100\text{pF}$  and  $V_{OH} = 2.4\text{V}$  ( $I_{OH} = -2\text{mA}$ ),  $V_{OL} = 0.4\text{V}$  ( $I_{OL} = 2\text{mA}$ ). The reference levels for measuring of output signals are  $2.0\text{V}$  ( $V_{OH}$ ) and  $0.8\text{V}$  ( $V_{OL}$ ).

9 : Assumes that  $t_{RCD} \geq t_{RCD}(\text{max})$  and  $t_{ASC} \geq t_{ASC}(\text{max})$ .

10 : Assumes that  $t_{RCD} \leq t_{RCD}(\text{max})$  and  $t_{RAD} \leq t_{RAD}(\text{max})$ .

11 : Assumes that  $t_{RAD} \geq t_{RAD}(\text{max})$  and  $t_{ASC} \leq t_{ASC}(\text{max})$ .

12 : tOFF (max) defines the time at which the output achieves the high impedance state (MF14M1-J17ATXX :  $I_{outI} \leq 10\ \mu\text{A}$ , MF18M1-J17ATXX :  $I_{outI} \leq 20\ \mu\text{A}$ ) and are not reference to  $V_{OH}(\text{min})$  or  $V_{OL}(\text{max})$ .

**TIMING REQUIREMENTS** ( $T_a = 0 \sim 55^\circ\text{C}$ ,  $V_{CC} = 3.3\text{V} \pm 5\%$ ,  $GND = 0\text{V}$ ) : (Note 13, 14)

Symbol	Parameter	Limits		Unit
		Min.	Max.	
tREF	Refresh cycle time		128	ms
tRP	RAS high pulse width	50		ns
tRCD	Delay time, RAS low to CAS low (Note15)	20	43	ns
tCRP	Delay time, CAS high to RAS low (Note16)	17		ns
tRPC	Precharge to CAS active time.	0		ns
tCPN	CAS high pulse width	10		ns
tRAD	Column address delay time from RAS low (Note 17)	17	28	ns
tASR	Row address setup time before RAS low	10		ns
tASC	Column address setup time before CAS low (Note18)	5	10	ns
tRAH	Row address hold time after RAS low	10		ns
tCAH	Column address hold time after CAS low	15		ns
tT	Transition time (Note19)	3	50	ns

Note 13 : The timing requirements are assumed  $t_T = 5\text{ ns}$ .

14 :  $V_{IH}(\text{min})$  and  $V_{IL}(\text{max})$  are reference levels for measuring timing of input signals.

15 : tRCD(max) is specified as a reference point only.

If  $t_{RCD} \geq t_{RCD}(\text{max})$ , access time is defined as tCAC and tCAA.

16 : tCRP requirement is applicable for all RAS/CAS cycles.

17 : tRAD(max) is specified as a reference point only.

If  $t_{RAD} \geq t_{RAD}(\text{max})$  and  $t_{ASC} \leq t_{ASC}(\text{max})$ , access time is assumed by tCAA for read cycle.

18 : tASC(max) is specified as a reference point only of address access time.

19 : tT is measured between  $V_{IH}(\text{min})$  and  $V_{IL}(\text{max})$ .

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Read and Refresh Cycles

Symbol	Parameter	Limits		Unit
		Min.	Max.	
t <sub>RC</sub>	Read cycle time	130		ns
t <sub>RAS</sub>	RAS low pulse width	70	10000	ns
t <sub>CAS</sub>	CAS low pulse width	20	10000	ns
t <sub>CSH</sub>	CAS hold time after RAS low	70		ns
t <sub>RSH</sub>	RAS hold time after CAS low	27		ns
t <sub>RSC</sub>	Read setup time before CAS low	5		ns
t <sub>RCH</sub>	Read hold time after CAS high	0		ns
t <sub>RRH</sub>	Read hold time after RAS high	10		ns

Write Cycle (Early Write)

Symbol	Parameter	Limits		Unit
		Min.	Max.	
t <sub>WC</sub>	Write cycle time	130		ns
t <sub>RAS</sub>	RAS low pulse width	70	10000	ns
t <sub>CAS</sub>	CAS low pulse width	20	10000	ns
t <sub>CSH</sub>	CAS hold time after RAS low	70		ns
t <sub>RSH</sub>	RAS hold time after CAS low	27		ns
t <sub>WCS</sub>	Write setup time before CAS low	5		ns
t <sub>WCH</sub>	Write hold time after CAS low	15		ns
t <sub>DS</sub>	Data setup time	10		ns
t <sub>DH</sub>	Data hold time after CAS low	22		ns

Page Mode Cycle (Read, Early Write)

Symbol	Parameter	Limits		Unit
		Min.	Max.	
t <sub>PC</sub>	Read, Write cycle time	55		ns
t <sub>CP</sub>	CAS high pulse width	10		ns
t <sub>TRAS</sub>	RAS low pulse width ( Note 20)	125	100000	ns

Note 20 : t<sub>TRAS</sub>(min) is specified by the following formula as two cycles of CAS input are executed.  
 $t_{TRAS}(min) = t_{CSH}(min) + t_{PC}(min)$ .

CAS before RAS Refresh Cycle (Note 21)

Symbol	Parameter	Limits		Unit
		Min.	Max.	
t <sub>CSR</sub>	CAS setup time for CAS before RAS refresh	20		ns
t <sub>CHR</sub>	CAS hold time for CAS before RAS refresh	15		ns

Note 21 : Eight or more CAS before RAS cycles are necessary for proper operation of CAS before RAS refresh mode.

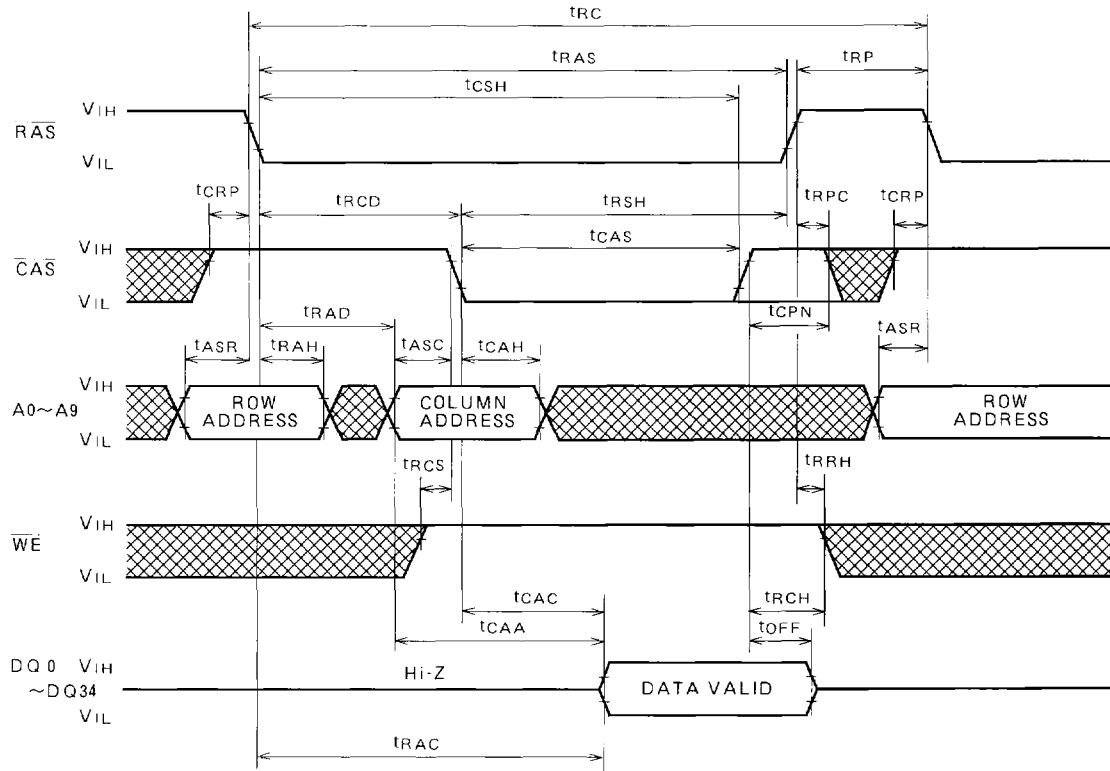
Self Refresh Cycle

Symbol	Parameter	Limits		Unit
		Min.	Max.	
t <sub>TRAS</sub>	RAS low pulse width	100		μs
t <sub>RPS</sub>	CAS high pulse width	130		ns
t <sub>CHS</sub>	RAS hold time after RAS high	-50		ns



Timing Diagrams (Note 22)

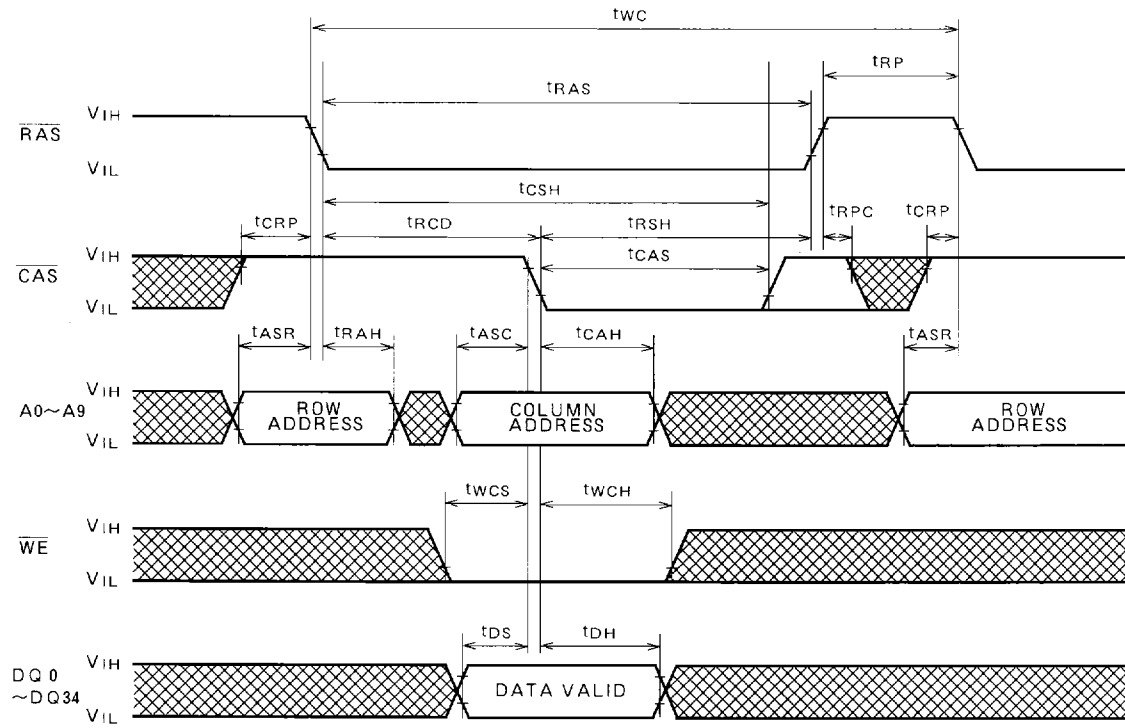
Read cycle



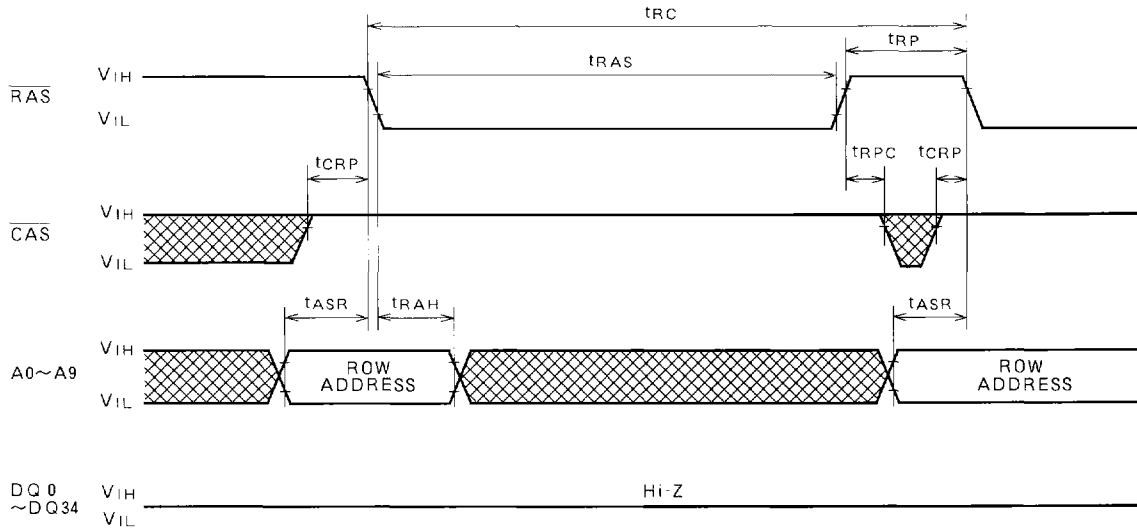
Note 22 :  indicates the don't care input

DYNAMIC RAM CARDS

Early Write Cycle

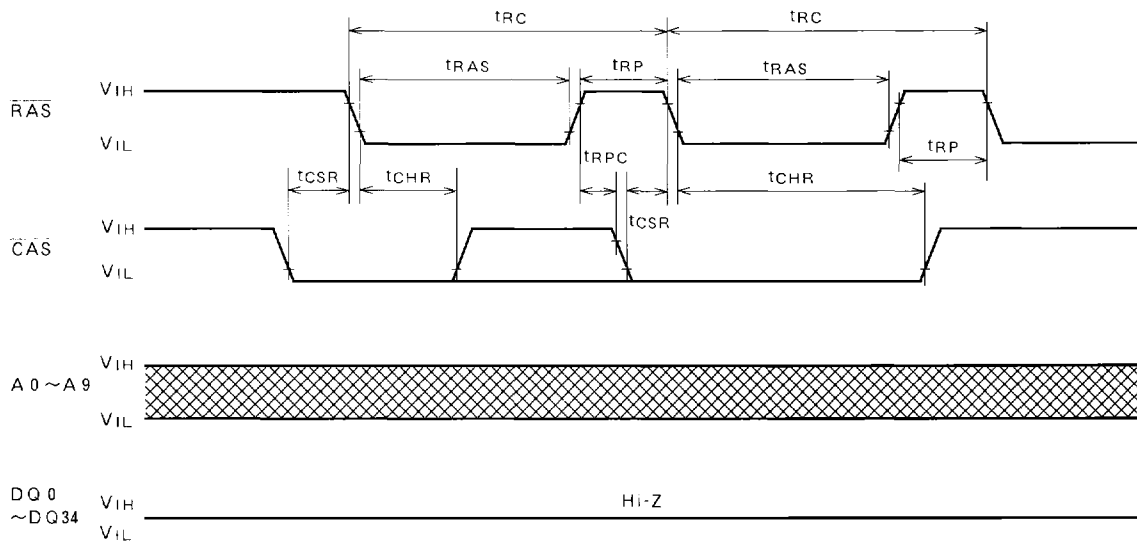


**$\overline{\text{RAS}}$  only Refresh Cycle** (Note 23)



Note 23 :  $\overline{\text{WE}}$  = don't care

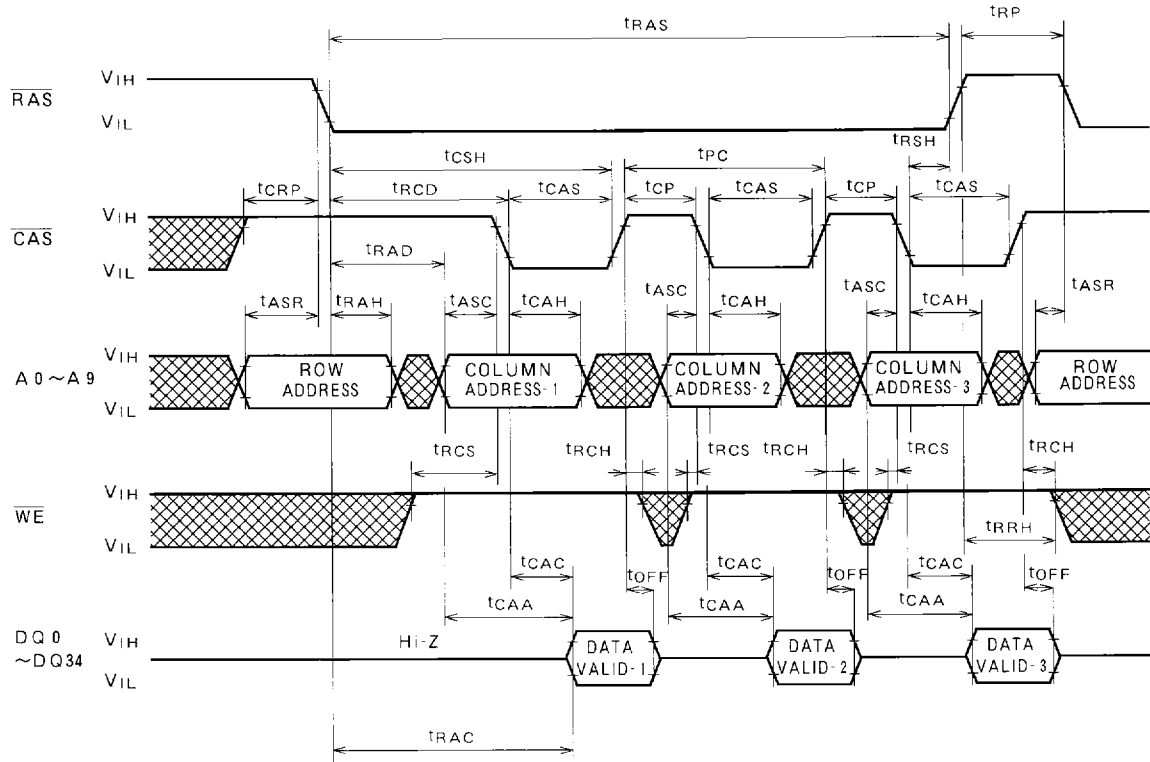
**$\overline{\text{CAS}}$  before  $\overline{\text{RAS}}$  Refresh Cycle** (Note 24)



Note 24 :  $\overline{\text{WE}} = V_{IH}$

DYNAMIC RAM CARDS

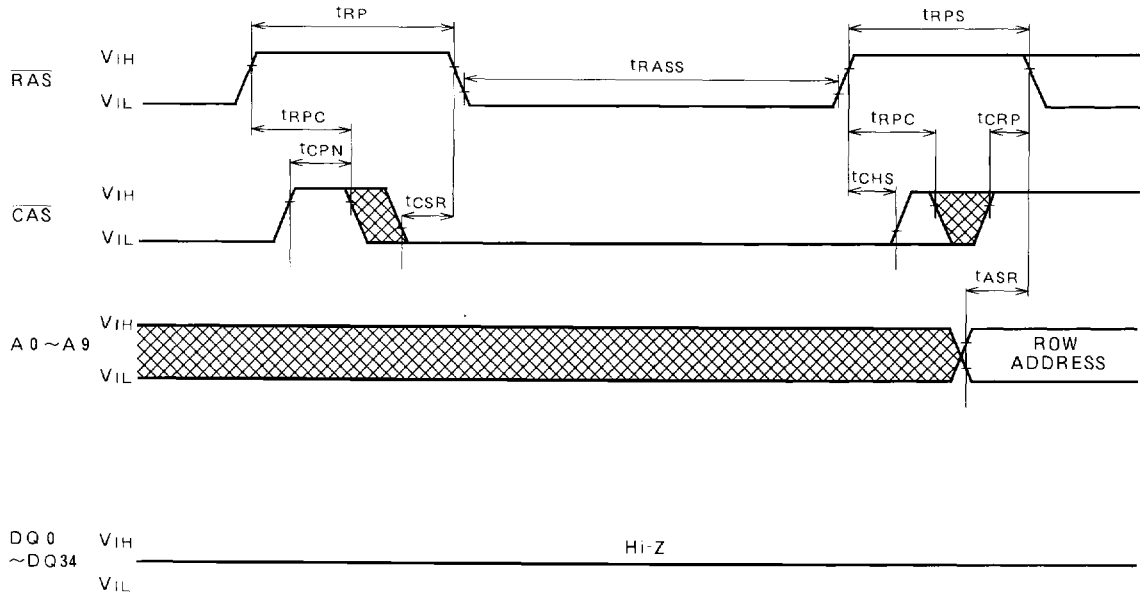
Page-Mode Read Cycle





DYNAMIC RAM CARDS

Self Refresh Cycle ( Note 25, 26 )



Note 25 :  $\overline{WE} = V_{IH}$

Note 26 : Self refresh sequence

Two refresh methods can be selected depending on the low pulse width ( $t_{RASS}$ ) of  $\overline{RAS}$  signal during the self refresh period.

1. In case of  $t_{RASS} < 300ms$

1. 1 Distributed refresh during Read/Write operation

(A) Timing diagram

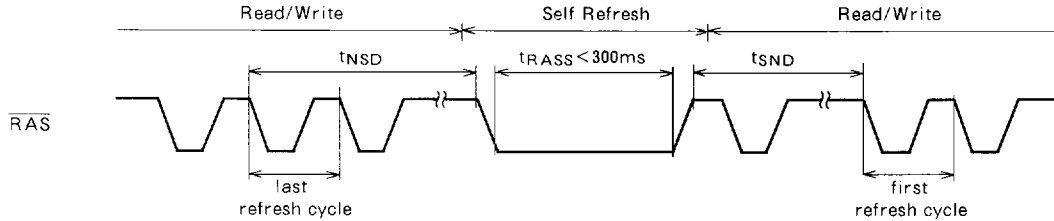
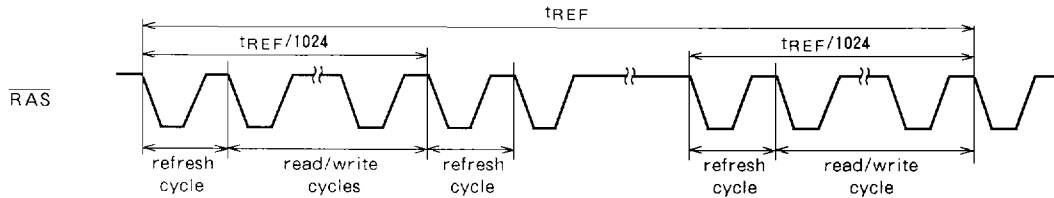


Table 1

Read/Write	Read/Write→ Self refresh	Self refresh→ Read/Write
CBR distributed refresh	$t_{NSD} + t_{SND} \leq 16.4ms$	
RAS only distributed refresh	$t_{NSD} \leq 16 \mu s$	$t_{SND} \leq 16 \mu s$

(B) Definition of distributed refresh



Definition of CBR distributed refresh

The CBR distributed refresh performs more than 1024 constant period ( $125 \mu s$  max) CBR cycles within 128 ms.

Definition of RAS only distributed refresh

All combinations of ten row address signals ( $A_0 \sim A_9$ ) are selected during 1024 constant period ( $16 \mu s$  max)  $\overline{RAS}$  only refresh cycles within 16.4ms.

Note :

$\overline{RAS}/\overline{CAS}$  refresh may be used instead of  $\overline{RAS}$  only refresh.

1. 1. 1 CBR distributed refresh

- Switching from read/write operation to self refresh operation.

The time interval from the falling edge of  $\overline{RAS}$  signal in the last CBR refresh cycle during read/write operation period to the falling edge of  $\overline{RAS}$  signal at the start of self refresh operation should be set within  $t_{NSD}$  (shown in table1).

- Switching from self refresh operation to read/write operation.

The time interval from the rising edge of  $\overline{RAS}$  signal at the end of self refresh operation to the falling edge of  $\overline{RAS}$  signal in the first CBR refresh cycle during read/write operation period should be set within  $t_{SND}$  (shown in table 1).

1. 1. 2  $\overline{RAS}$  only distributed refresh

- Switching from read/write operation to self refresh operation.

The time interval  $t_{NSD}$  from the falling edge of  $\overline{RAS}$  signal in the last  $\overline{RAS}$  only refresh cycle during read/write operation period to the falling edge of  $\overline{RAS}$  signal at the start of self refresh operation should be set within  $16 \mu s$ .

- Switching from self refresh operation to read/write operation.

The time interval  $t_{SND}$  from the rising edge of  $\overline{RAS}$  signal at the end of self refresh operation to the falling edge of  $\overline{RAS}$  signal in the first CBR refresh cycle during read/write operation period should be set within  $16 \mu s$ .

1. 2 Burst refresh during Read/Write operation

(A) Timing diagram

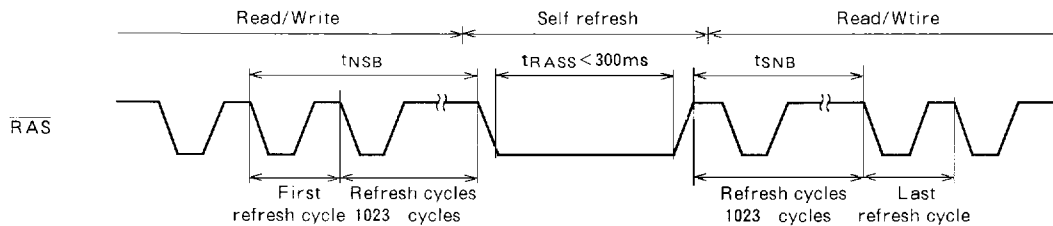
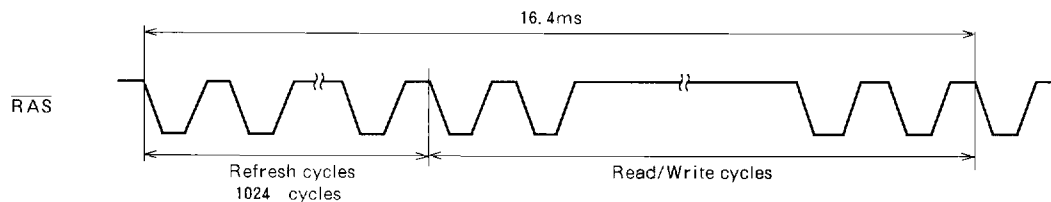


Table 2

Read/Write	Read/Write → Self refresh	Self refresh → Read/Write
CBR burst refresh	$t_{NSB} \leq 16.4ms$	$t_{SNB} \leq 16.4ms$
RAS only burst refresh	$t_{NSB} + t_{SNB} \leq 16.4ms$	

(B) Definition of burst refresh



Definition of CBR burst refresh

The CBR burst refresh performs more than 1024 continuous CBR cycles within 16.4ms.

Definition of  $\overline{RAS}$  only burst refresh

All combinations of ten row address signals ( $A_0 \sim A_9$ ) are selected during 1024 continuous  $\overline{RAS}$  only refresh cycles within 16.4ms.

1. 2. 1 CBR burst refresh

- Switching from read/write operation to self refresh operation.

The time interval  $t_{NSB}$  from the falling edge of  $\overline{RAS}$  signal in the first CBR refresh cycle during read/write operation period to the falling edge of  $\overline{RAS}$  signal at the start of self refresh operation should be set within 16.4ms.

- Switching from self refresh operation to read/write operation.

The time interval  $t_{SNB}$  from the rising edge of  $\overline{RAS}$  signal at the end of self refresh operation to the falling edge of  $\overline{RAS}$  signal in the last CBR refresh cycle during read/write operation period should be set within 16.4ms.

1. 2. 2  $\overline{RAS}$  only burst refresh

- Switching from read/write operation to self refresh operation.

The time interval from the falling edge of  $\overline{RAS}$  signal in the first  $\overline{RAS}$  only refresh cycle during read/write operation period to the falling edge of  $\overline{RAS}$  signal at the start of self refresh operation should be set within  $t_{NSB}$  (shown in table 2).

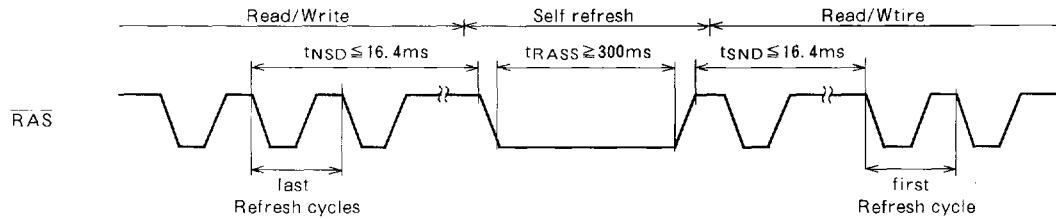
- Switching from self refresh operation to read/write operation.

The time interval from the rising edge of  $\overline{RAS}$  signal at the end of self refresh operation to the falling edge of  $\overline{RAS}$  signal in the last  $\overline{RAS}$  only refresh cycle during read/write operation period should be set within  $t_{SNB}$  (shown in table 2).



2. In case of  $t_{RASS} \geq 300ms$

(A) Timing diagram-A



Timing diagram-B

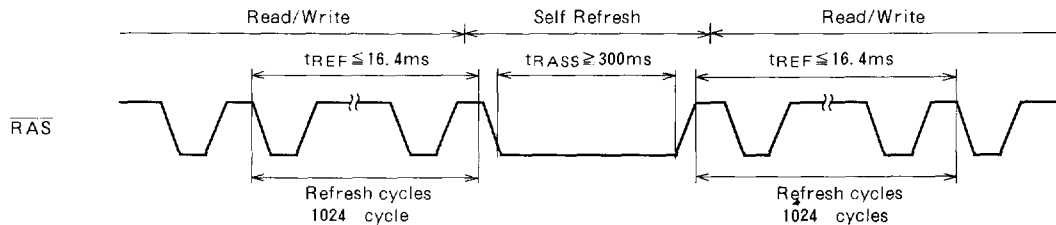


Table 3

Read/Write	Read/Write→Self refresh	Self refresh→Read/Write
CBR distributed refresh	Timing diagram-A	Timing diagram-A
RAS only distributed refresh CBR burst refresh RAS only burst refresh	Timing diagram-B	Timing diagram-B

(B) Definition of refresh

The same as 1. 1 -(B) and 1. 2 -(B)

2. 1. 1 CBR distributed refresh

- Switching from read/write operation to self refresh operation.

The time interval t<sub>NSD</sub> from the falling edge of RAS signal in the last CBR refresh cycle during read/write operation period to the falling edge of RAS signal at the start of self refresh operation should be set within 16.4ms.

- Switching from self refresh operation to read/write operation.

The time interval t<sub>NSD</sub> from the rising edge of RAS signal at the end of self refresh operation to the falling edge of RAS signal in the first CBR refresh cycle during read/write operation period should be set within 16.4ms.

2. 1. 2 RAS only distributed, CBR burst, RAS only burst refresh

- Before and after the self refresh, 1024 refresh cycles should be executed within 16.4ms for each refresh operation.