


# Complete Isolated RS485/RS422 $\mu$ Module Transceiver + Power

## FEATURES

- **UL Rated RS485/RS422 Transceiver: 2500V<sub>RMS</sub>**  
UL Recognized  File #E151738
- **Isolated DC Power: 5V at Up to 200mA**
- **No External Components Required**
- **20Mbps or Low EMI 250kbps Data Rate**
- **High ESD:  $\pm 15$ kV HBM on Transceiver Interface**
- **High Common Mode Transient Immunity: 30kV/ $\mu$ s**
- **Integrated Selectable 120 $\Omega$  Termination**
- 3.3V (LTM2881-3) or 5.0V (LTM2881-5) Operation
- 1.62V to 5.5V Logic Supply Pin for Flexible Digital Interface
- Common Mode Working Voltage: 560V<sub>PEAK</sub>
- High Input Impedance Failsafe RS485 Receiver
- Current Limited Drivers and Thermal Shutdown
- Compatible with TIA/EIA-485-A Specification
- High Impedance Output During Internal Fault Condition
- Low Current Shutdown Mode (< 10 $\mu$ A)
- General Purpose CMOS Isolated Channel
- Small, Low Profile (15mm  $\times$  11.25mm)  
Surface Mount BGA and LGA Packages

## APPLICATIONS

- Isolated RS485/RS422 Interface
- Industrial Networks
- Breaking RS485 Ground Loops

## DESCRIPTION

The LTM<sup>®</sup>2881 is a complete galvanically isolated full-duplex RS485/RS422  $\mu$ Module<sup>®</sup> transceiver. No external components are required. A single supply powers both sides of the interface through an integrated, isolated, low noise, efficient 5V output DC/DC converter.

Coupled inductors and an isolation power transformer provide 2500V<sub>RMS</sub> of isolation between the line transceiver and the logic interface. This device is ideal for systems where the ground loop is broken allowing for large common mode voltage variation. Uninterrupted communication is guaranteed for common mode transients greater than 30kV/ $\mu$ s.

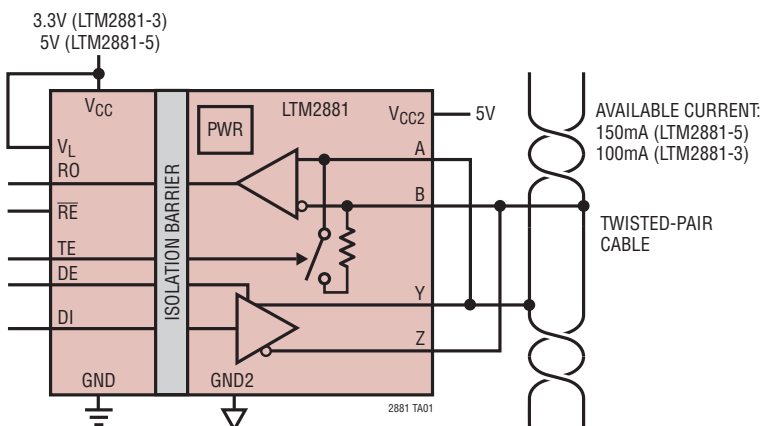
Maximum data rates are 20Mbps or 250kbps in slew limited mode. Transmit data, DI and receive data, RO, are implemented with event driven low jitter processing. The receiver has a one-eighth unit load supporting up to 256 nodes per bus. A logic supply pin allows easy interfacing with different logic levels from 1.62V to 5.5V, independent of the main supply.

Enhanced ESD protection allows this part to withstand up to  $\pm 15$ kV (human body model) on the transceiver interface pins to isolated supplies and  $\pm 10$ kV through the isolation barrier to logic supplies without latch-up or damage.

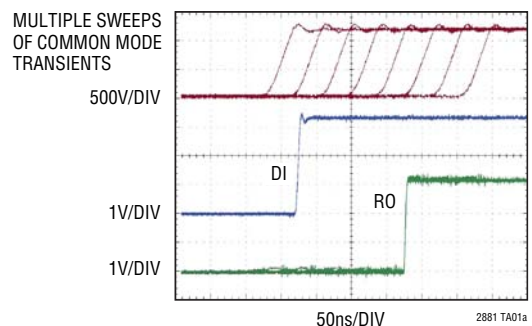
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## TYPICAL APPLICATION

Isolated Half-Duplex RS485  $\mu$ Module Transceiver



LTM2881 Operating Through 35kV/ $\mu$ s CM Transients



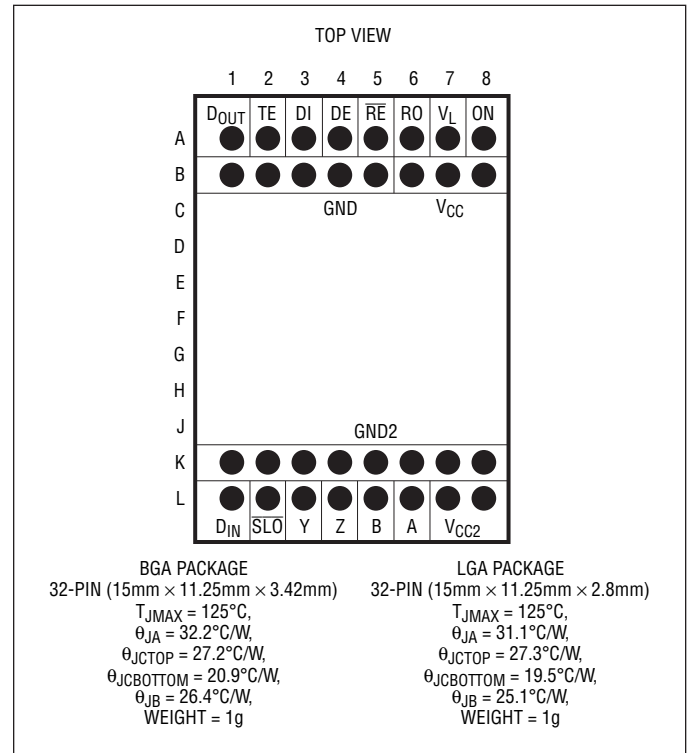
# LTM2881

## ABSOLUTE MAXIMUM RATINGS

(Note 1)

$V_{CC}$ to GND .....	-0.3V to 6V	
$V_{CC2}$ to GND2.....	-0.3V to 6V	
$V_L$ to GND .....	-0.3V to 6V	
Interface Voltages		
(A, B, Y, Z) to GND2.....	$V_{CC2}$ -15V to 15V	
(A-B) with Terminator Enabled.....	$\pm 6V$	
Signal Voltages ON, RO, DI, DE,		
$\overline{RE}$ , TE, $D_{OUT}$ to GND.....	-0.3V to $V_L + 0.3V$	
Signal Voltages $\overline{SLO}$ ,		
$D_{IN}$ to GND2.....	-0.3V to $V_{CC2} + 0.3V$	
Operating Temperature Range		
LTM2881C .....	0°C to 70°C	
LTM2881I.....	-40°C to 85°C	
LTM2881H .....	-40°C to 105°C	
Maximum Internal Operating Temperature .....		125°C
Storage Temperature Range .....		-55°C to 125°C
Peak Reflow Temperature (Soldering, 10 sec).....		245°C

## PIN CONFIGURATION



## ORDER INFORMATION

LEAD FREE FINISH	TRAY	PART MARKING*	PACKAGE DESCRIPTION	TEMPERATURE RANGE
LTM2881CY-3#PBF	LTM2881CY-3#PBF	LTM2881Y-3	32-Pin (15mm × 11.25mm × 3.42mm) BGA	0°C to 70°C
LTM2881IY-3#PBF	LTM2881IY-3#PBF	LTM2881Y-3	32-Pin (15mm × 11.25mm × 3.42mm) BGA	-40°C to 85°C
LTM2881HY-3#PBF	LTM2881HY-3#PBF	LTM2881Y-3	32-Pin (15mm × 11.25mm × 3.42mm) BGA	-40°C to 105°C
LTM2881CY-5#PBF	LTM2881CY-5#PBF	LTM2881Y-5	32-Pin (15mm × 11.25mm × 3.42mm) BGA	0°C to 70°C
LTM2881IY-5#PBF	LTM2881IY-5#PBF	LTM2881Y-5	32-Pin (15mm × 11.25mm × 3.42mm) BGA	-40°C to 85°C
LTM2881HY-5#PBF	LTM2881HY-5#PBF	LTM2881Y-5	32-Pin (15mm × 11.25mm × 3.42mm) BGA	-40°C to 105°C
LTM2881CV-3#PBF	LTM2881CV-3#PBF	LTM2881V-3	32-Pin (15mm × 11.25mm × 2.8mm) LGA	0°C to 70°C
LTM2881IV-3#PBF	LTM2881IV-3#PBF	LTM2881V-3	32-Pin (15mm × 11.25mm × 2.8mm) LGA	-40°C to 85°C
LTM2881CV-5#PBF	LTM2881CV-5#PBF	LTM2881V-5	32-Pin (15mm × 11.25mm × 2.8mm) LGA	0°C to 70°C
LTM2881IV-5#PBF	LTM2881IV-5#PBF	LTM2881V-5	32-Pin (15mm × 11.25mm × 2.8mm) LGA	-40°C to 85°C

Consult LTC Marketing for parts specified with wider operating temperature ranges. \*The temperature grade is identified by a label on the shipping container.

For more information on lead free part marking, go to: <http://www.linear.com/leadfree/>

This product is only offered in trays. For more information go to: <http://www.linear.com/packaging/>

**ELECTRICAL CHARACTERISTICS** The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at  $T_A = 25^\circ\text{C}$ . LTM2881-3  $V_{CC} = 3.3\text{V}$ , LTM2881-5  $V_{CC} = 5.0\text{V}$ ,  $V_L = 3.3\text{V}$ ,  $\text{GND} = \text{GND2} = 0\text{V}$ ,  $\text{ON} = V_L$  unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS	
<b>Power Supply</b>							
$V_{CC}$	$V_{CC}$ Supply Voltage	LTM2881-3	●	3.0	3.3	3.6	V
		LTM2881-5	●	4.5	5.0	5.5	V
$V_L$	$V_L$ Supply Voltage		●	1.62		5.5	V
$I_{CCPOFF}$	$V_{CC}$ Supply Current in Off Mode	$\text{ON} = 0\text{V}$	●		0	10	$\mu\text{A}$
$I_{CCS}$	$V_{CC}$ Supply Current in On Mode	LTM2881-3 $\text{DE} = 0\text{V}$ , $\overline{\text{RE}} = V_L$ , No Load	●		20	25	$\text{mA}$
		LTM2881-5 $\text{DE} = 0\text{V}$ , $\overline{\text{RE}} = V_L$ , No Load	●		15	19	$\text{mA}$
		LTM2881-5, H-Grade	●			20	$\text{mA}$
$V_{CC2}$	Regulated $V_{CC2}$ Output Voltage, Loaded	LTM2881-3 $\text{DE} = 0\text{V}$ , $\overline{\text{RE}} = V_L$ , $I_{\text{LOAD}} = 100\text{mA}$	●	4.75	5.0		V
		LTM2881-5 $\text{DE} = 0\text{V}$ , $\overline{\text{RE}} = V_L$ , $I_{\text{LOAD}} = 150\text{mA}$	●	4.75	5.0		V
		LTM2881-3, H-Grade, $I_{\text{LOAD}} = 90\text{mA}$	●	4.75			V
$V_{CC2\text{NOLOAD}}$	Regulated $V_{CC2}$ Output Voltage, No Load	$\text{DE} = 0\text{V}$ , $\overline{\text{RE}} = V_L$ , No Load		4.8	5.0	5.35	V
		Efficiency			62		%
$I_{CC2S}$	$V_{CC2}$ Short-Circuit Current	$\text{DE} = 0\text{V}$ , $\overline{\text{RE}} = V_L$ , $V_{CC2} = 0\text{V}$	●			250	$\text{mA}$
<b>Driver</b>							
$ V_{OD} $	Differential Driver Output Voltage	$R = \infty$ (Figure 1)	●			$V_{CC2}$	V
		$R = 27\Omega$ (RS485) (Figure 1)	●	1.5		$V_{CC2}$	V
		$R = 50\Omega$ (RS422) (Figure 1)	●	2		$V_{CC2}$	V
$\Delta V_{OD} $	Difference in Magnitude of Driver Differential Output Voltage for Complementary Output States	$R = 27\Omega$ or $R = 50\Omega$ (Figure 1)	●			0.2	V
$V_{OC}$	Driver Common Mode Output Voltage	$R = 27\Omega$ or $R = 50\Omega$ (Figure 1)	●			3	V
$\Delta V_{OC} $	Difference in Magnitude of Driver Common Mode Output Voltage for Complementary Output States	$R = 27\Omega$ or $R = 50\Omega$ (Figure 1)	●			0.2	V
$I_{OZD}$	Driver Three-State (High Impedance) Output Current on Y and Z	$\text{DE} = 0\text{V}$ , (Y or Z) = $-7\text{V}$ , $+12\text{V}$	●			$\pm 10$	$\mu\text{A}$
		H-Grade	●			$\pm 50$	$\mu\text{A}$
$I_{OSD}$	Maximum Driver Short-Circuit Current	$-7\text{V} \leq (\text{Y or Z}) \leq 12\text{V}$ (Figure 2)	●	-250		250	$\text{mA}$
<b>Receiver</b>							
$R_{IN}$	Receiver Input Resistance	$\overline{\text{RE}} = 0\text{V}$ or $V_L$ , $V_{IN} = -7\text{V}$ , $-3\text{V}$ , $3\text{V}$ , $7\text{V}$ , $12\text{V}$ (Figure 3)	●	96	125		$\text{k}\Omega$
		$\overline{\text{RE}} = 0\text{V}$ or $V_L$ , $V_{IN} = -7\text{V}$ , $-3\text{V}$ , $3\text{V}$ , $7\text{V}$ , $12\text{V}$ (Figure 3), H-Grade	●	48	125		
$R_{TE}$	Receiver Termination Resistance Enabled	$\text{TE} = V_L$ , $V_{AB} = 2\text{V}$ , $V_B = -7\text{V}$ , $0\text{V}$ , $10\text{V}$ (Figure 8)	●	108	120	156	$\Omega$
$I_{IN}$	Receiver Input Current (A, B)	$\text{ON} = 0\text{V}$ $V_{CC2} = 0\text{V}$ or $5\text{V}$ , $V_{IN} = 12\text{V}$ (Figure 3)	●			125	$\mu\text{A}$
		$\text{ON} = 0\text{V}$ $V_{CC2} = 0\text{V}$ or $5\text{V}$ , $V_{IN} = 12\text{V}$ (Figure 3), H-Grade	●			250	$\mu\text{A}$
		$\text{ON} = 0\text{V}$ $V_{CC2} = 0\text{V}$ or $5\text{V}$ , $V_{IN} = -7\text{V}$ (Figure 3)	●	-100			$\mu\text{A}$
		$\text{ON} = 0\text{V}$ $V_{CC2} = 0\text{V}$ or $5\text{V}$ , $V_{IN} = -7\text{V}$ (Figure 3), H-Grade	●	-145			$\mu\text{A}$
$V_{TH}$	Receiver Differential Input Threshold Voltage (A-B)	$-7\text{V} \leq B \leq 12\text{V}$	●	-0.2		0.2	V
$\Delta V_{TH}$	Receiver Input Failsafe Hysteresis	$B = 0\text{V}$			25		$\text{mV}$
	Receiver Input Failsafe Threshold	$B = 0\text{V}$		-0.2	-0.05	0	V

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SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
<b>Logic</b>						
$V_{IL}$	Logic Input Low Voltage	$1.62\text{V} \leq V_L \leq 5.5\text{V}$	●		0.4	V
$V_{IH}$	Logic Input High Voltage	$D_{IN}$	●	$0.67 \cdot V_{CC2}$		V
		$\overline{SLO}$	●	2		V
		$D_I, TE, DE, \text{ON}, \overline{RE}$ :	●	$0.67 \cdot V_L$		V
		$V_L \geq 2.35\text{V}$ $1.62\text{V} \leq V_L < 2.35\text{V}$	●	$0.75 \cdot V_L$		V
$I_{INL}$	Logic Input Current		●	0	$\pm 1$	$\mu\text{A}$
$V_{HYS}$	Logic Input Hysteresis	(Note 2)		150		mV
$V_{OH}$	Output High Voltage	Output High, $I_{LOAD} = -4\text{mA}$ (Sourcing), $5.5\text{V} \geq V_L \geq 3\text{V}$	●	$V_L - 0.4$		V
		Output High, $I_{LOAD} = -1\text{mA}$ (Sourcing), $1.62\text{V} \leq V_L < 3\text{V}$	●	$V_L - 0.4$		V
$V_{OL}$	Output Low Voltage	Output Low, $I_{LOAD} = 4\text{mA}$ (Sinking), $5.5\text{V} \geq V_L \geq 3\text{V}$	●		0.4	V
		Output High, $I_{LOAD} = 1\text{mA}$ (Sinking), $1.62\text{V} \leq V_L < 3\text{V}$	●		0.4	V
$I_{OZR}$	Three-State (High Impedance) Output Current on RO	$\overline{RE} = V_L, 0\text{V} \leq RO \leq V_L$	●		$\pm 1$	$\mu\text{A}$
$I_{OSR}$	Short-Circuit Current	$0\text{V} \leq (RO \text{ or } D_{OUT}) \leq V_L$	●		$\pm 85$	mA

**SWITCHING CHARACTERISTICS** The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at  $T_A = 25^\circ\text{C}$ . LTM2881-3  $V_{CC} = 3.3\text{V}$ , LTM2881-5  $V_{CC} = 5.0\text{V}$ ,  $V_L = 3.3\text{V}$ ,  $\text{GND} = \text{GND2} = 0\text{V}$ ,  $\text{ON} = V_L$  unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
<b>Driver <math>\overline{SLO} = V_{CC2}</math></b>						
$f_{MAX}$	Maximum Data Rate	(Note 3)		20		Mbps
$t_{PLHD}$ $t_{PHLD}$	Driver Input to Output	$R_{DIFF} = 54\Omega, C_L = 100\text{pF}$ (Figure 4)	●	60	85	ns
$\Delta t_{PD}$	Driver Input to Output Difference $ t_{PLHD} - t_{PHLD} $	$R_{DIFF} = 54\Omega, C_L = 100\text{pF}$ (Figure 4)	●	1	8	ns
$t_{SKEWD}$	Driver Output Y to Output Z	$R_{DIFF} = 54\Omega, C_L = 100\text{pF}$ (Figure 4)	●	1	$\pm 8$	ns
$t_{RD}$ $t_{FD}$	Driver Rise or Fall Time	$R_{DIFF} = 54\Omega, C_L = 100\text{pF}$ (Figure 4)	●	4	12.5	ns
$t_{ZLD}, t_{ZHD},$ $t_{LZD}, t_{HZD}$	Driver Output Enable or Disable Time	$R_L = 500\Omega, C_L = 50\text{pF}$ (Figure 5)	●		170	ns
<b>Driver <math>\overline{SLO} = \text{GND2}</math></b>						
$f_{MAX}$	Maximum Data Rate	(Note 3)		250		kbps
$t_{PLHD}$ $t_{PHLD}$	Driver Input to Output	$R_{DIFF} = 54\Omega, C_L = 100\text{pF}$ (Figure 4)		1	1.55	$\mu\text{s}$
$\Delta t_{PD}$	Driver Input to Output Difference $ t_{PLHD} - t_{PHLD} $	$R_{DIFF} = 54\Omega, C_L = 100\text{pF}$ (Figure 4)		50	500	ns
$t_{SKEWD}$	Driver Output Y to Output Z	$R_{DIFF} = 54\Omega, C_L = 100\text{pF}$ (Figure 4)		$\pm 200$	$\pm 500$	ns

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SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
$t_{RD}$ $t_{FD}$	Driver Rise or Fall Time	$R_{DIFF} = 54\Omega$ , $C_L = 100\text{pF}$ (Figure 4)	●	0.9	1.5	$\mu\text{s}$
$t_{ZLD}$ , $t_{ZHD}$ , $t_{LZD}$ , $t_{HZD}$	Driver Output Enable or Disable Time	$R_L = 500\Omega$ , $C_L = 50\text{pF}$ (Figure 5)	●		400	ns
<b>Receiver</b>						
$t_{PLHR}$ $t_{PHLR}$	Receiver Input to Output	$C_L = 15\text{pF}$ , $V_{CM} = 2.5\text{V}$ , $ V_{AB}  = 1.4\text{V}$ , $t_R$ and $t_F < 4\text{ns}$ , (Figure 6)	●	100	140	ns
$t_{SKEWR}$	Differential Receiver Skew $ t_{PLHR} - t_{PHLR} $	$C_L = 15\text{pF}$ (Figure 6)	●	1	8	ns
$t_{RR}$ $t_{FR}$	Receiver Output Rise or Fall Time	$C_L = 15\text{pF}$ (Figure 6)	●	3	12.5	ns
$t_{ZLR}$ , $t_{ZHR}$ , $t_{LZR}$ , $t_{HZR}$	Receiver Output Enable Time	$R_L = 1\text{k}\Omega$ , $C_L = 15\text{pF}$ (Figure 7)	●		50	ns
$t_{RTEN}$ , $t_{RTZ}$	Termination Enable or Disable Time	$\overline{RE} = 0\text{V}$ , $DE = 0\text{V}$ , $V_{AB} = 2\text{V}$ , $V_B = 0\text{V}$ (Figure 8)	●		100	$\mu\text{s}$
<b>Generic Logic Input</b>						
$t_{PLHL1}$ $t_{PHLL1}$	$D_{IN}$ to $D_{OUT}$ Input to Output	$C_L = 15\text{pF}$ , $t_R$ and $t_F < 4\text{ns}$	●	60	100	ns
<b>Power Supply Generator</b>						
	$V_{CC2} - \text{GND2}$ Supply Start-Up Time (0V to 4.5V)	$\text{ON} \rightarrow V_L$ , No Load	●	325	800	$\mu\text{s}$

**ISOLATION CHARACTERISTICS**  $T_A = 25^\circ\text{C}$ , LTM2881-3  $V_{CC} = 3.3\text{V}$ , LTM2881-5  $V_{CC} = 5.0\text{V}$ ,  $V_L = 3.3\text{V}$  unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
$V_{ISO}$	Rated Dielectric Insulation Voltage	1 Minute (Derived from 1 Second Test)	2500			$V_{RMS}$
		1 Second (Note 5)	$\pm 4400$			$V_{DC}$
	Common Mode Transient Immunity	LTM2881-3 $V_{CC} = 3.3\text{V}$ , LTM2881-5 $V_{CC} = 5\text{V}$ , $V_L = \text{ON} = 3.3\text{V}$ , $V_{CM} = 1\text{kV}$ , $\Delta t = 33\text{ns}$ (Note 2)	$\pm 30$			$\text{kV}/\mu\text{s}$
$V_{IORM}$	Maximum Working Insulation Voltage	(Notes 2, 5)	560			$V_{PEAK}$
			400			$V_{RMS}$
	Partial Discharge	$V_{PR} = 1050 V_{PEAK}$ (Note 2)			5	pC
	Input to Output Resistance	(Notes 2, 5)	$10^9$			$\Omega$
	Input to Output Capacitance	(Notes 2, 5)		6		pF
	Creepage Distance	(Notes 2, 5)		9.48		mm

**Note 1:** Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. Exposure to any Absolute Maximum Rating condition for extended periods may affect device reliability and lifetime.

**Note 2:** Guaranteed by design and not subject to production test.

**Note 3:** Maximum Data rate is guaranteed by other measured parameters and is not tested directly.

**Note 4:** This  $\mu$ Module transceiver includes overtemperature protection that is intended to protect the device during momentary overload conditions. Junction temperature will exceed  $125^\circ\text{C}$  when overtemperature protection is active. Continuous operation above specified maximum operating junction temperature may result in device degradation or failure.

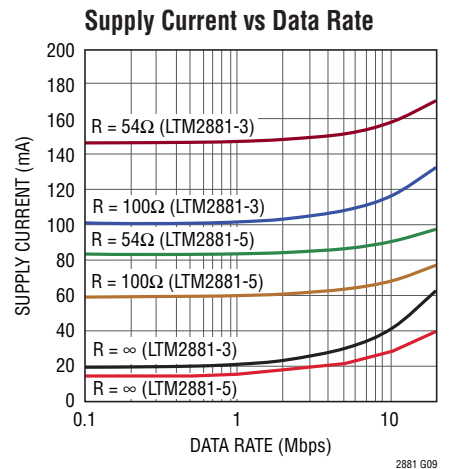
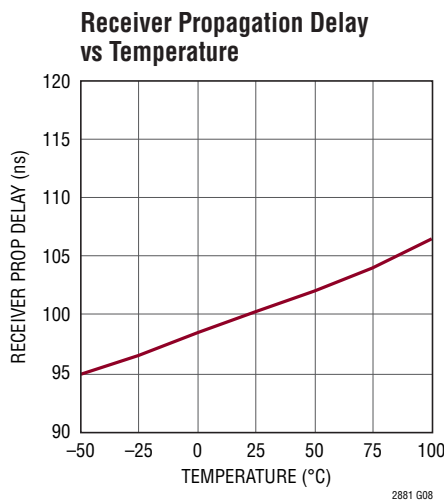
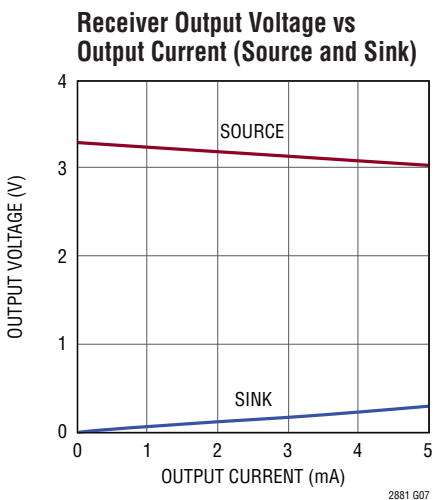
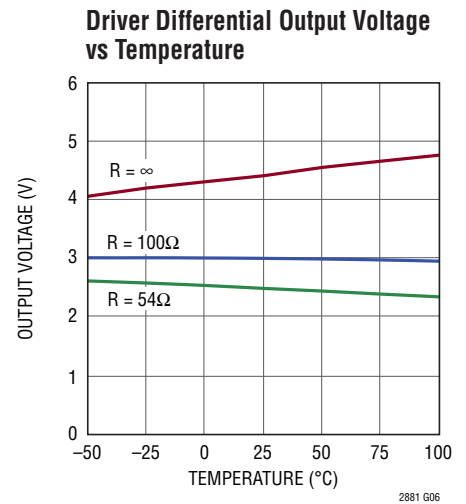
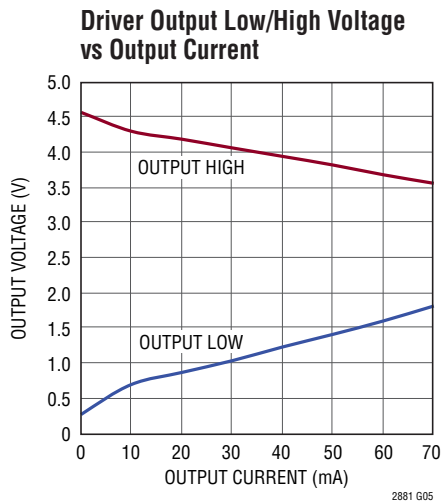
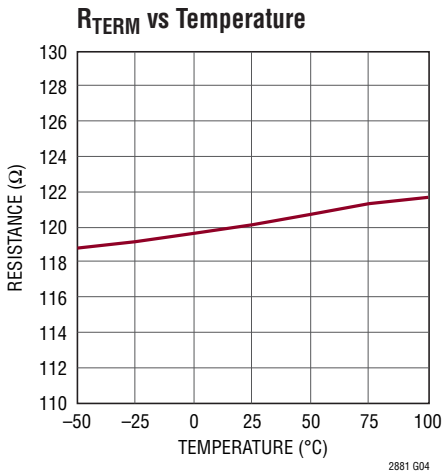
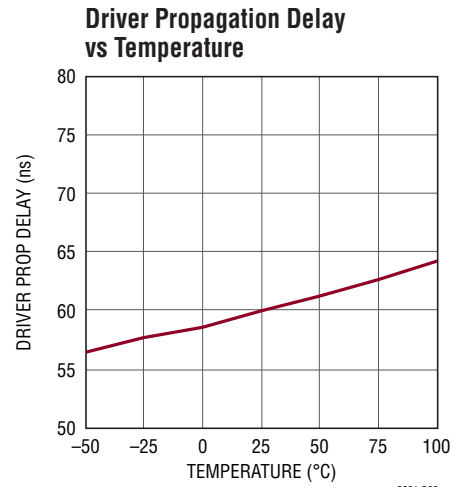
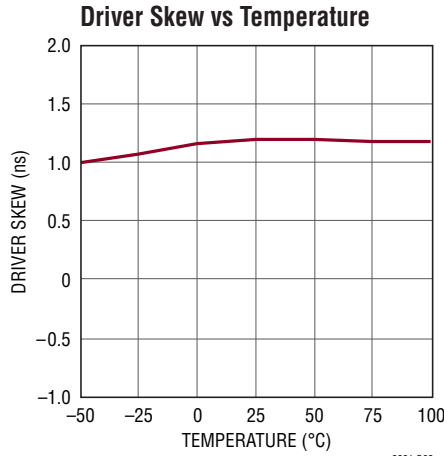
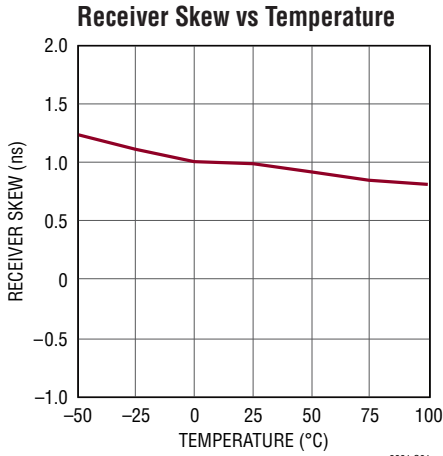
**Note 5:** Device considered a 2-terminal device. Pin group A1 through B8 shorted together and pin group K1 through L8 shorted together.

# LTM2881

## TYPICAL PERFORMANCE CHARACTERISTICS

$V_{CC} = 5.0V$ ,  $V_L = 3.3V$  unless otherwise noted.

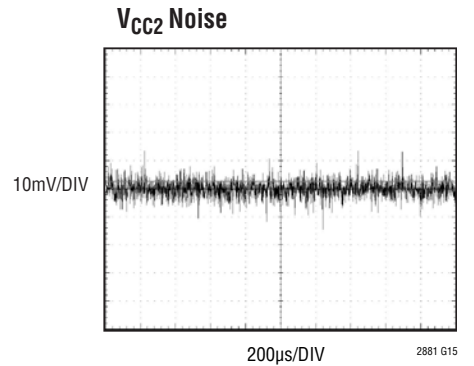
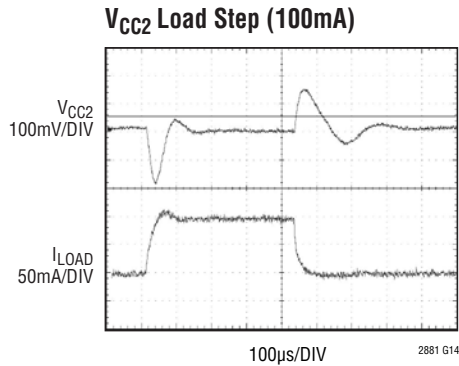
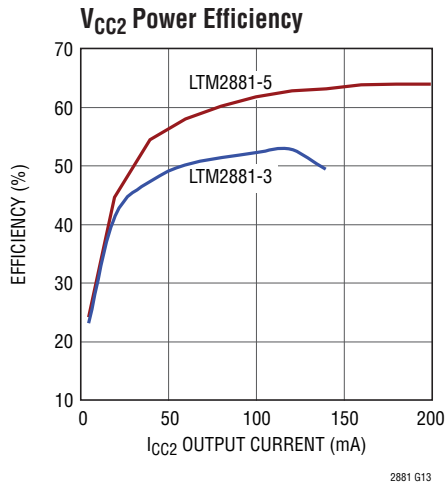
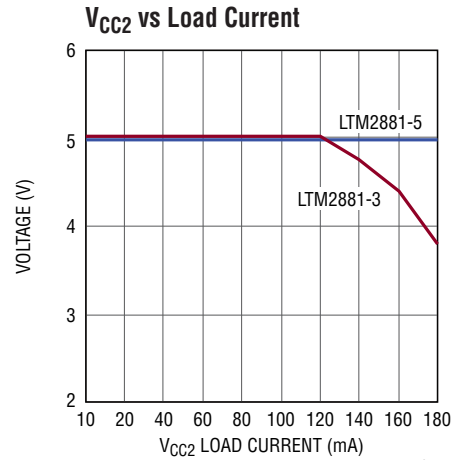
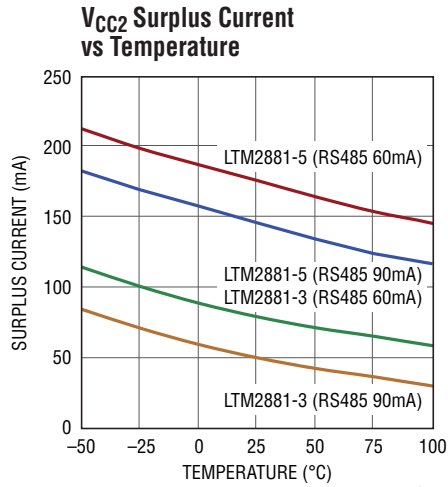
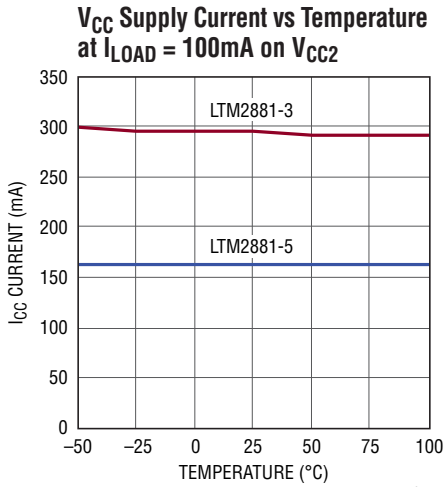
$T_A = 25^\circ C$ , LTM2881-3  $V_{CC} = 3.3V$ , LTM2881-5



**TYPICAL PERFORMANCE CHARACTERISTICS**

$V_{CC} = 5.0V$ ,  $V_L = 3.3V$  unless otherwise noted.

$T_A = 25^\circ C$ , LTM2881-3  $V_{CC} = 3.3V$ , LTM2881-5



## PIN FUNCTIONS

### LOGIC SIDE ( $V_{CC}$ , $V_L$ , GND)

**D<sub>OUT</sub> (Pin A1):** General Purpose Logic Output. Logic output connected through isolation path to D<sub>IN</sub>. Under the condition of an isolation communication failure D<sub>OUT</sub> is in a high impedance state.

**TE (Pin A2):** Terminator Enable. A logic high enables a termination resistor (typically 120Ω) between pins A and B.

**DI (Pin A3):** Driver Input. If the driver outputs are enabled (DE high), then a low on DI forces the driver noninverting output (Y) low and the inverting output (Z) high. A high on DI, with the driver outputs enabled, forces the driver noninverting output (Y) high and inverting output (Z) low.

**DE (Pin A4):** Driver Enable. A logic low disables the driver leaving the outputs Y and Z in a high impedance state. A logic high enables the driver.

**$\overline{RE}$  (Pin A5):** Receiver Enable. A logic low enables the receiver output. A logic high disables RO to a high impedance state.

**RO (Pin A6):** Receiver Output. If the receiver output is enabled ( $\overline{RE}$  low) and if  $A - B$  is  $> 200\text{mV}$ , RO is a logic high, if  $A - B$  is  $< -200\text{mV}$  RO is a logic low. If the receiver inputs are open, shorted, or terminated without a valid signal, RO will be high. Under the condition of an isolation communication failure RO is in a high impedance state.

**V<sub>L</sub> (Pin A7):** Logic Supply. Interface supply voltage for pins RO,  $\overline{RE}$ , TE, DI, DE, D<sub>OUT</sub>, and ON. Recommended operating voltage is 1.62V to 5.5V. Internally bypassed to GND with 2.2μF.

**ON (Pin A8):** Enable. Enables power and data communication through the isolation barrier. If ON is high the part is enabled and power and communications are functional to the isolated side. If ON is low the logic side is held in reset and the isolated side is unpowered.

**GND (Pins B1-B5):** Circuit Ground.

**V<sub>CC</sub> (Pins B6-B8):** Supply Voltage. Recommended operating voltage is 3V to 3.6V for LTM2881-3 and 4.5V to 5.5V for LTM2881-5. Internally bypassed to GND with 2.2μF.

### ISOLATED SIDE ( $V_{CC2}$ , GND2)

**D<sub>IN</sub> (Pin L1):** General Purpose Isolated Logic Input. Logic input on the isolated side relative to  $V_{CC2}$  and GND2. A logic high on D<sub>IN</sub> will generate a logic high on D<sub>OUT</sub>. A logic low on D<sub>IN</sub> will generate a logic low on D<sub>OUT</sub>.

**$\overline{SLO}$  (Pin L2):** Driver Slew Rate Control. A low input, relative to GND2, will force the driver into a reduced slew rate mode for reduced EMI. A high input, relative to GND2, puts the driver into full speed mode to support maximum data rates.

**Y (Pin L3):** Non Inverting Driver Output. High impedance when the driver is disabled.

**Z (Pin L4):** Inverting Driver Output. High impedance when the driver is disabled.

**B (Pin L5):** Inverting Receiver Input. Impedance is  $> 96\text{k}\Omega$  in receive mode with TE low or unpowered.

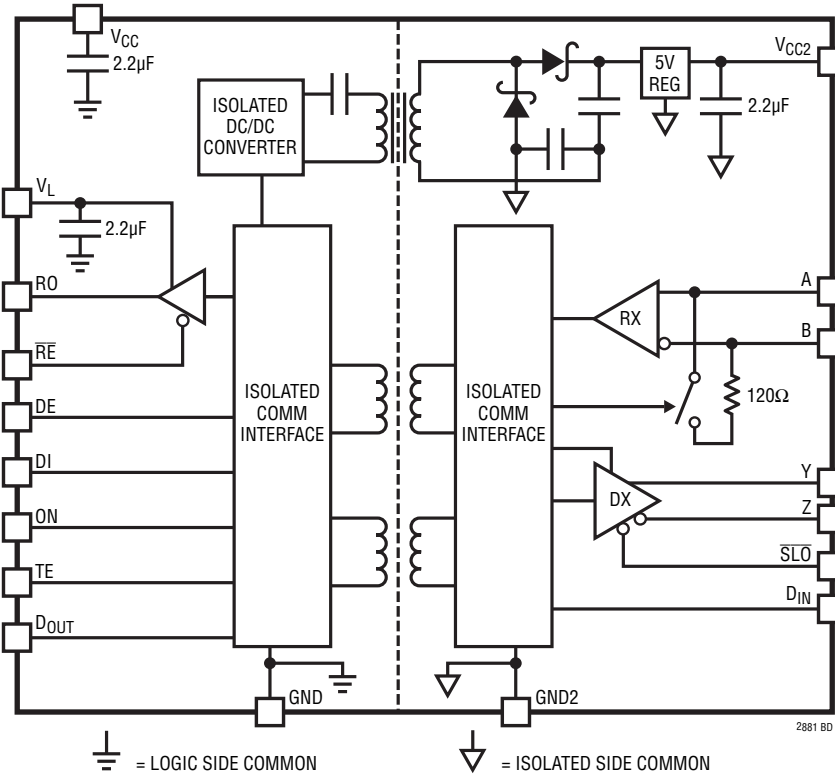
**A (Pin L6):** Non Inverting Receiver Input. Impedance is  $> 96\text{k}\Omega$  in receive mode with TE low or unpowered.

**V<sub>CC2</sub> (Pins L7-L8):** Isolated Supply Voltage. Internally generated from  $V_{CC}$  by an isolated DC/DC converter and regulated to 5V. Internally bypassed to GND2 with 2.2μF.

**GND2 (Pins K1-K8):** Isolated Side Circuit Ground. The pads should be connected to the isolated ground and/or cable shield.



# BLOCK DIAGRAM



# TEST CIRCUITS

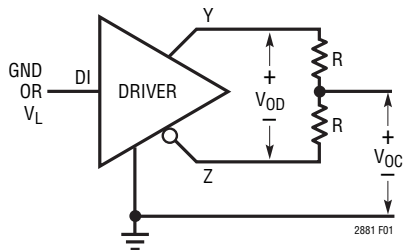


Figure 1. Driver DC Characteristics

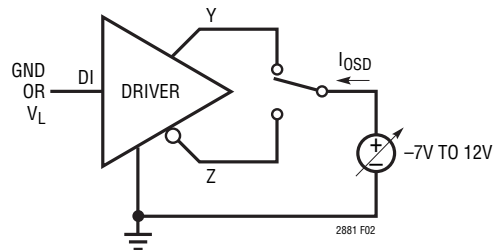


Figure 2. Driver Output Short-Circuit Current

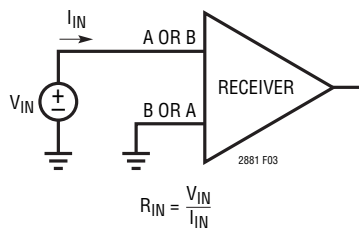


Figure 3. Receiver Input Current and Input Resistance

TEST CIRCUITS

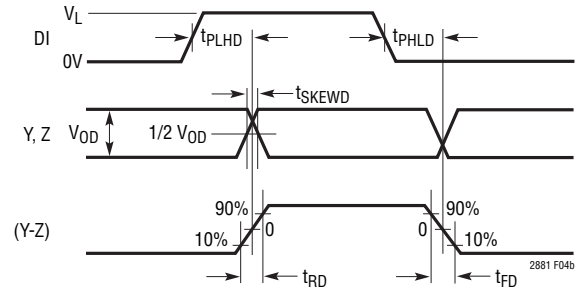
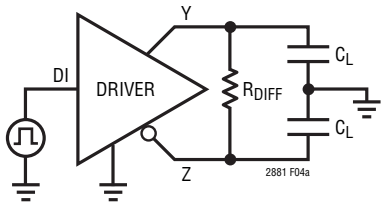


Figure 4. Driver Timing Measurement

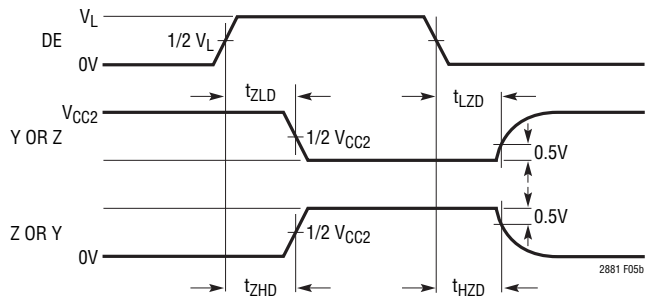
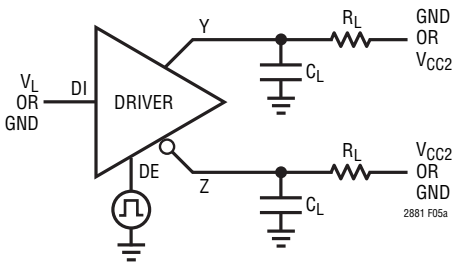


Figure 5. Driver Enable and Disable Timing Measurements

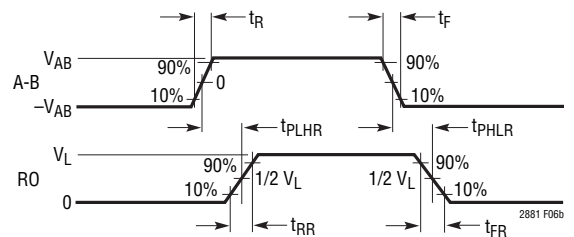
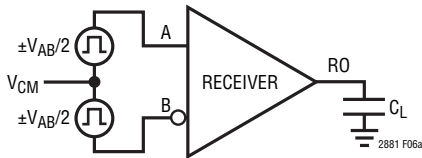


Figure 6. Receiver Propagation Delay Measurements

## TEST CIRCUITS

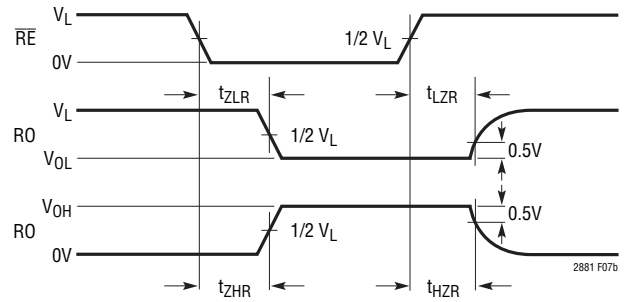
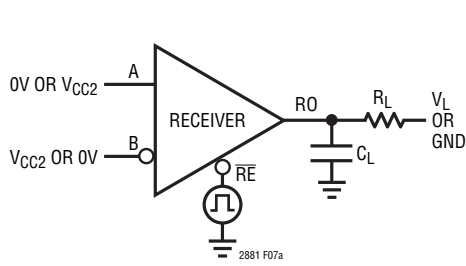


Figure 7. Receiver Enable/Disable Time Measurements

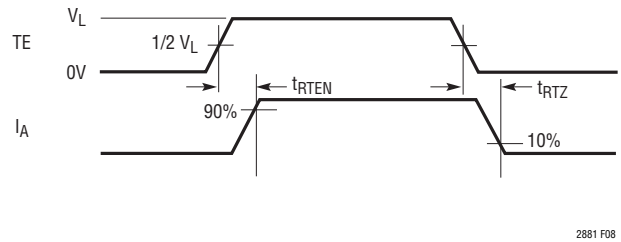
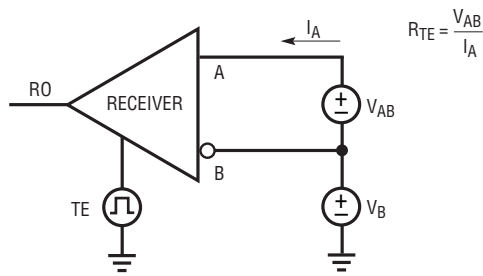


Figure 8. Termination Resistance and Timing Measurements

## FUNCTIONAL TABLE

LOGIC INPUTS				MODE	A, B	Y, Z	RO	DC/DC CONVERTER	TERMINATOR
ON	RE	TE	DE						
1	0	0	0	Receive	R <sub>IN</sub>	Hi-Z	Enabled	On	Off
1	0	0	1	Transceiver	R <sub>IN</sub>	Driven	Enabled	On	Off
1	1	0	1	Transmit	R <sub>IN</sub>	Driven	Hi-Z	On	Off
1	0	1	0	Receive + Term On	R <sub>TE</sub>	Hi-Z	Enabled	On	On
0	X	X	X	Off	R <sub>IN</sub>	Hi-Z	Hi-Z	Off	Off

## APPLICATIONS INFORMATION

### Overview

The LTM2881  $\mu$ Module transceiver provides a galvanically-isolated robust RS485/RS422 interface, powered by an integrated, regulated DC/DC converter, complete with decoupling capacitors. A switchable termination resistor is integrated at the receiver input to provide proper termination to the RS485 bus. The LTM2881 is ideal for use in networks where grounds can take on different voltages. Isolation in the LTM2881 blocks high voltage differences and eliminates ground loops and is extremely tolerant of common mode transients between ground potentials. Error free operation is maintained through common mode events greater than 30kV/ $\mu$ s providing excellent noise isolation.

### $\mu$ Module Technology

The LTM2881 utilizes isolator  $\mu$ Module technology to translate signals and power across an isolation barrier. Signals on either side of the barrier are encoded into pulses and translated across the isolation boundary using coreless transformers formed in the  $\mu$ Module substrate. This system, complete with data refresh, error checking, safe shutdown on fail, and extremely high common mode immunity, provides a robust solution for bidirectional signal isolation. The  $\mu$ Module technology provides the means to combine the isolated signaling with our RS485 transceiver and powerful isolated DC/DC converter in one small package.

### DC/DC Converter

The LTM2881 contains a fully integrated isolated DC/DC converter, including the transformer, so that no external components are necessary. The logic side contains a full-bridge driver, running about 2MHz, and is AC-coupled to a single transformer primary. A series DC blocking capacitor prevents transformer saturation due to driver duty cycle imbalance. The transformer scales the primary voltage, and is rectified by a full-wave voltage doubler. This topology eliminates transformer saturation caused by secondary imbalances.

The DC/DC converter is connected to a low dropout regulator (LDO) to provide a regulated low noise 5V output.

The internal power solution is sufficient to support the transceiver interface at its maximum specified load and data

rate, and external pins are supplied for extra decoupling (optional) and heat dissipation. The logic supplies,  $V_{CC}$  and  $V_L$  have a 2.2 $\mu$ F decoupling capacitance to GND and the isolated supply  $V_{CC2}$  has a 2.2 $\mu$ F decoupling capacitance to GND2 within the  $\mu$ Module package.

### $V_{CC2}$ Output

The on-board DC/DC converter provides isolated 5V power to output  $V_{CC2}$ .  $V_{CC2}$  is capable of supplying up to 1W of power at 5V in the LTM2881-5 option and up to 600mW of power in the LTM2881-3 option. This surplus current is available to external applications. The amount of surplus current is dependent upon the implementation and current delivered to the RS485 driver and line load. An example of available surplus current is shown in the Typical Performance Characteristics graph,  $V_{CC2}$  Surplus Current vs Temperature. Figure 19 demonstrates a method of using the  $V_{CC2}$  output directly and with a switched power path that is controlled with the isolated RS485 data channel.

### Driver

The driver provides full RS485 and RS422 compatibility. When enabled, if DI is high, Y-Z is positive. When the driver is disabled, both outputs are high impedance with less than 10 $\mu$ A of leakage current over the entire common mode range of -7V to 12V, with respect to GND2.

### Driver Overvoltage and Overcurrent Protection

The driver outputs are protected from short circuits to any voltage within the absolute maximum range of ( $V_{CC2}$  -15V) to (GND2 +15V) levels. The maximum  $V_{CC2}$  current in this condition is 250mA. If the pin voltage exceeds about  $\pm$ 10V, current limit folds back to about half of the peak value to reduce overall power dissipation and avoid damaging the part.

The device also features thermal shutdown protection that disables the driver and receiver output in case of excessive power dissipation (See Note 4 in the Electrical Characteristics section).

### $\overline{SLO}$ Mode

The LTM2881 features a logic-selectable reduced slew rate mode ( $\overline{SLO}$  mode) that softens the driver output edges to

## APPLICATIONS INFORMATION

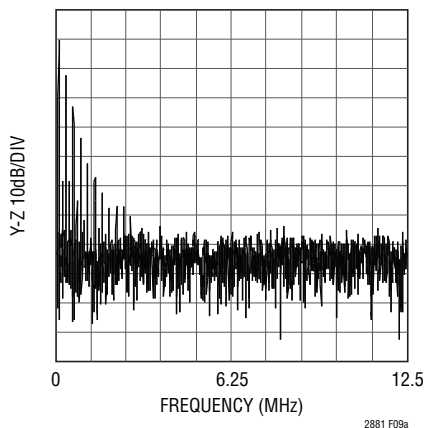


Figure 9a. Frequency Spectrum  $\overline{\text{SLO}}$  Mode 125kHz Input

reduce EMI emissions from equipment and data cables. The reduced slew rate mode is entered by taking the  $\overline{\text{SLO}}$  pin low to GND2, where the data rate is limited to about 250kbps. Slew limiting also mitigates the adverse effects of imperfect transmission line termination caused by stubs or mismatched cables.

Figures 9a and 9b show the frequency spectrums of the LTM2881 driver outputs in normal and  $\overline{\text{SLO}}$  mode operating at 250kbps.  $\overline{\text{SLO}}$  mode significantly reduces the high frequency harmonics.

### Receiver and Failsafe

With the receiver enabled, when the absolute value of the differential voltage between the A and B pins is greater than 200mV, the state of RO will reflect the polarity of (A-B). During data communication the receiver detects the state of the input with symmetric thresholds around 0V. The symmetric thresholds preserve duty cycle for attenuated signals with slow transition rates on high capacitive busses, or long cable lengths. The receiver incorporates a failsafe feature that guarantees the receiver output to be a logic-high during an idle bus, when the inputs are shorted, left open or terminated, but not driven. The failsafe feature eliminates the need for system level integration of network pre-biasing by guaranteeing a logic-high on RO under the conditions of an idle bus. Further network biasing constructed to condition transient noise during an idle state is unnecessary due to the common mode transient rejection of the LTM2881. The failsafe detector monitors A and B in parallel with the receiver and detects the state

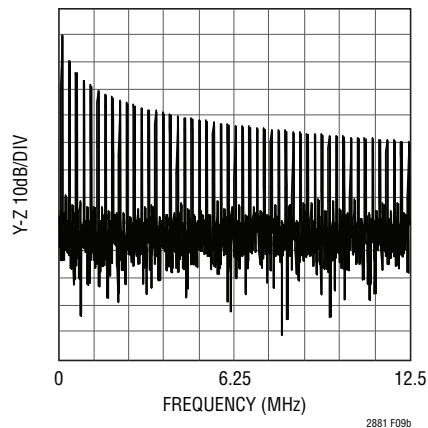


Figure 9b. Normal Mode Frequency Spectrum 125kHz Input

of the bus when A-B is above the input failsafe threshold for longer than about  $3\mu\text{s}$  with a hysteresis of 25mV. This failsafe feature is guaranteed to work for inputs spanning the entire common mode range of  $-7\text{V}$  to  $12\text{V}$ .

The receiver output is internally driven high (to  $V_L$ ) or low (to GND) with no external pull-up needed. When the receiver is disabled the RO pin becomes Hi-Z with leakage of less than  $\pm 1\mu\text{A}$  for voltages within the supply range.

### Receiver Input Resistance

The receiver input resistance from A or B to GND2 is greater than 96k permitting up to a total of 256 receivers per system without exceeding the RS485 receiver loading specification. High temperature H-/MP-Grade operation reduces the input resistance to 48k permitting 128 receivers on the bus. The input resistance of the receiver is unaffected by enabling/disabling the receiver or by powering/unpowering the part. The equivalent input resistance looking into A and B is shown in Figure 10.

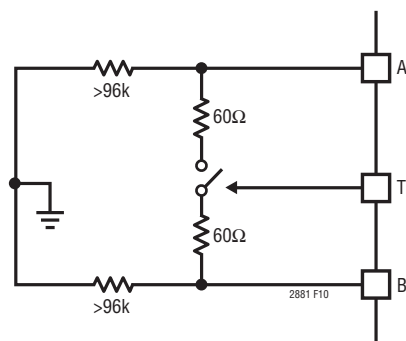


Figure 10. Equivalent Input Resistance into A and B

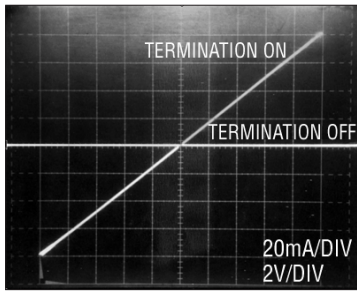
## APPLICATIONS INFORMATION

### Switchable Termination

Proper cable termination is very important for signal fidelity. If the cable is not terminated with its characteristic impedance, reflections will distort the signal waveforms.

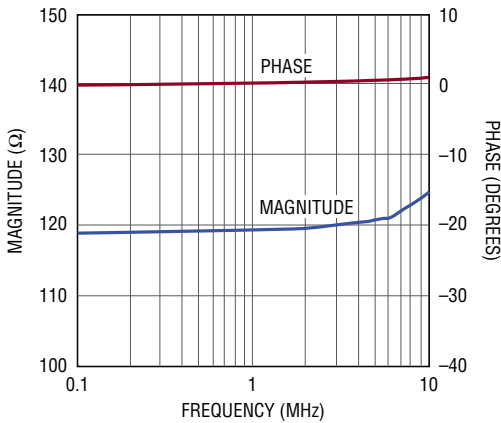
The integrated switchable termination resistor provides logic control of the line termination for optimal performance when configuring transceiver networks.

When the TE pin is high, the termination resistor is enabled and the differential resistance from A to B is 120Ω. Figure 11 shows the I/V characteristics between pins A and B with the termination resistor enabled and disabled. The resistance is maintained over the entire RS485 common mode range of -7V to 12V as shown in Figure 12. The integrated termination resistor has a high frequency response which does not limit performance at the maximum specified data rate. Figure 13 shows the magnitude and



2881 F11

Figure 11. Curve Trace Between A and B with Termination Enabled and Disabled



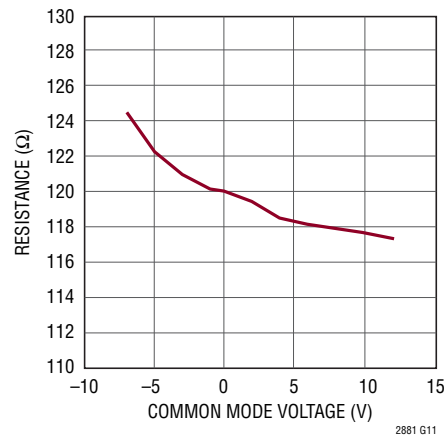
2881 F13

Figure 13. Termination Magnitude and Phase vs Frequency

phase of the termination impedance versus frequency. The termination resistor cannot be enabled by TE if the device is unpowered, ON is low or the LTM2881 is in thermal shutdown.

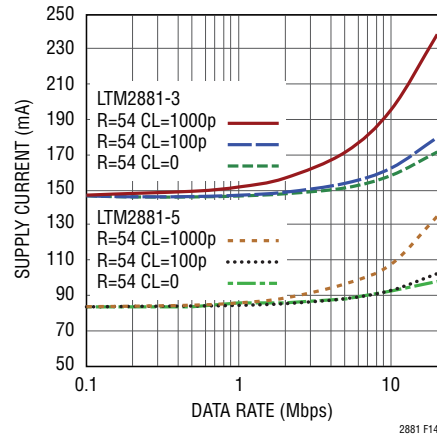
### Supply Current

The static supply current is dominated by power delivered to the termination resistance. Power supply current increases with data rate due to capacitive loading. Figure 14 shows supply current versus data rate for three different loads for the circuit configuration of Figure 4. Supply current increases with additional external applications drawing current from  $V_{CC2}$ .



2881 G11

Figure 12. Termination Resistance vs Common Mode Voltage



2881 F14

Figure 14. Supply Current vs Data Rate

## APPLICATIONS INFORMATION

### PCB Layout Considerations

The high integration of the LTM2881 makes PCB layout very simple. However, to optimize its electrical isolation characteristics, EMI, and thermal performance, some layout considerations are necessary.

- Under heavily loaded conditions  $V_{CC}$  and GND current can exceed 300mA. Sufficient copper must be used on the PCB to insure resistive losses do not cause the supply voltage to drop below the minimum allowed level. Similarly, the  $V_{CC2}$  and GND2 conductors must be sized to support any external load current. These heavy copper traces will also help to reduce thermal stress and improve the thermal conductivity.
- Input and Output decoupling is not required, since these components are integrated within the package. An additional bulk capacitor with a value of 6.8 $\mu$ F to 22 $\mu$ F is recommended. The high ESR of this capacitor reduces board resonances and minimizes voltage spikes caused by hot plugging of the supply voltage. For EMI sensitive applications, an additional low ESL ceramic capacitor of 1 $\mu$ F to 4.7 $\mu$ F, placed as close to the power and ground terminals as possible, is recommended. Alternatively, a number of smaller value parallel capacitors may be used to reduce ESL and achieve the same net capacitance.
- Do not place copper on the PCB between the inner columns of pads. This area must remain open to withstand the rated isolation voltage.
- The use of solid ground planes for GND and GND2 is recommended for non-EMI critical applications to optimize signal fidelity, thermal performance, and to minimize RF emissions due to uncoupled PCB trace conduction. The drawback of using ground planes, where EMI is of concern, is the creation of a dipole antenna structure which can radiate differential voltages formed between GND and GND2. If ground planes are used it is recommended to minimize their area, and use contiguous planes as any openings or splits can exacerbate RF emissions.
- For large ground planes a small capacitance ( $\leq 330$ pF) from GND to GND2, either discrete or embedded within the substrate, provides a low impedance current return path for the module parasitic capacitance, minimizing any high frequency differential voltages and substantially reducing radiated emissions. Discrete capacitance will not be as effective due to parasitic ESL. In addition, voltage rating, leakage, and clearance must be considered for component selection. Embedding the capacitance within the PCB substrate provides a near ideal capacitor and eliminates component selection issues; however, the PCB must be 4 layers. Care must be exercised in applying either technique to insure the voltage rating of the barrier is not compromised.

The PCB layout in Figures 15a to 15e show the low EMI demo board for the LTM2881. The demo board uses a combination of EMI mitigation techniques, including both embedded PCB bridge capacitance and discrete GND to GND2 capacitors. Two safety rated type Y2 capacitors are used in series, manufactured by Murata, part number GA342QR7GF471KW01L. The embedded capacitor effectively suppresses emissions above 400MHz, whereas the discrete capacitors are more effective below 400MHz.

EMI performance is shown in Figure 16, measured using a Gigahertz Transverse Electromagnetic (GTEM) cell and method detailed in IEC 61000-4-20, "Testing and Measurement Techniques – Emission and Immunity Testing in Transverse Electromagnetic Waveguides."

APPLICATIONS INFORMATION

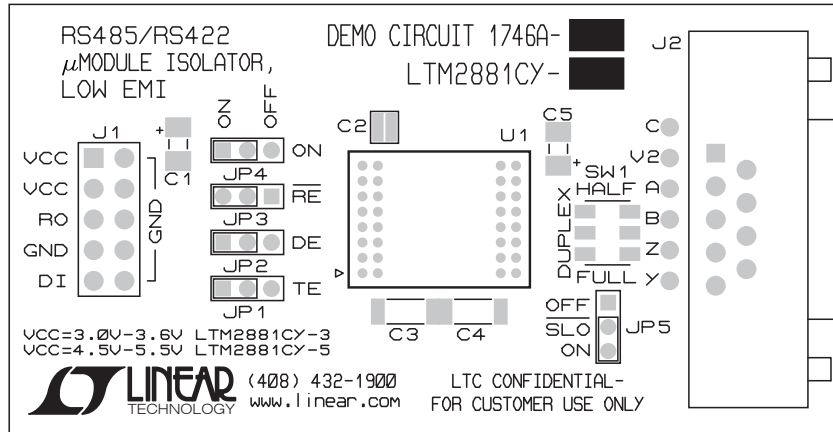


Figure 15a. Low EMI Demo Board Layout

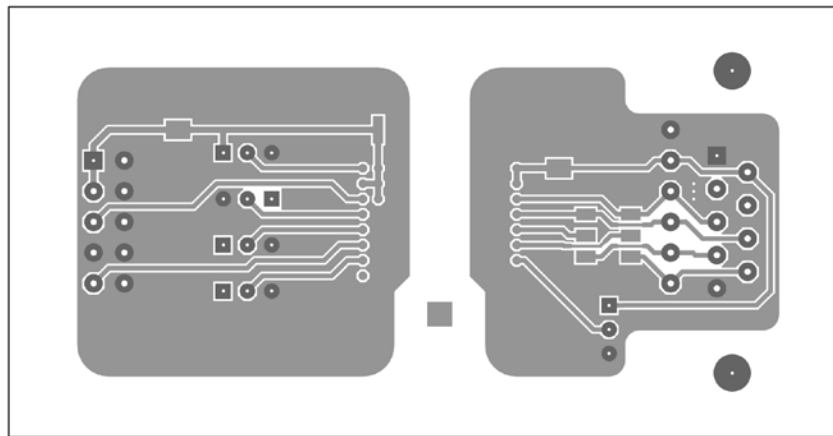


Figure 15b. Low EMI Demo Board Layout (DC1746A), Top Layer

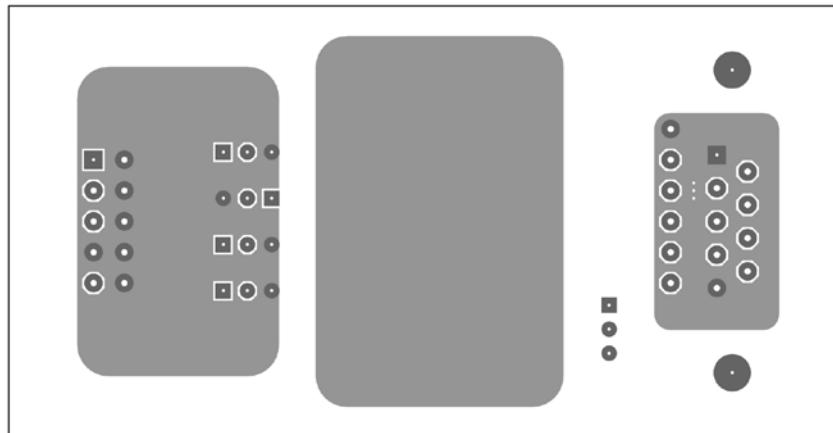


Figure 15c. Low EMI Demo Board Layout (DC1746A), Inner Layer 1



APPLICATIONS INFORMATION

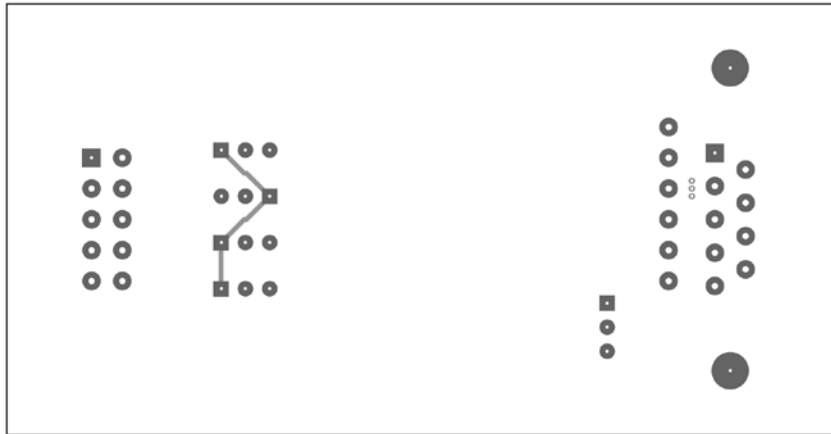


Figure 15d. Low EMI Demo Board Layout (DC1746A), Inner Layer 2

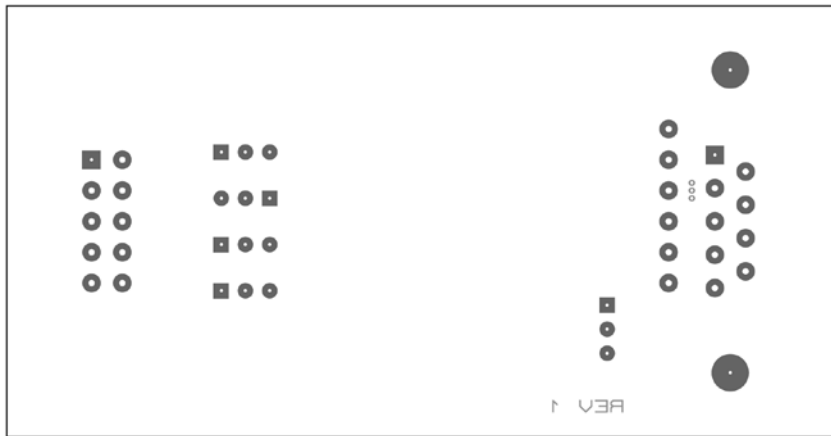


Figure 15e. Low EMI Demo Board Layout (DC1746A), Bottom Layer

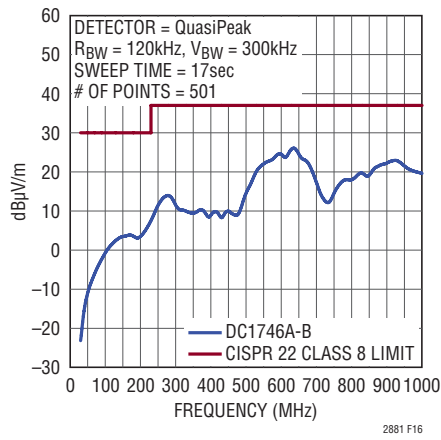


Figure 16. Low EMI Demo Board Emissions

## APPLICATIONS INFORMATION

### Cable Length versus Data Rate

For a given data rate, the maximum transmission distance is bounded by the cable properties. A typical curve of cable length versus data rate compliant with the RS485 standard is shown in Figure 16. Three regions of this curve reflect different performance limiting factors in data transmission. In the flat region of the curve, maximum distance is determined by resistive loss in the cable. The downward sloping region represents limits in distance and rate due to the AC losses in the cable. The solid vertical line represents the specified maximum data rate in the RS485 standard. The dashed line at 250kbps shows the maximum data rate when  $\overline{SLO}$  is low. The dashed line at 20Mbps shows the maximum data rate when  $\overline{SLO}$  is high.

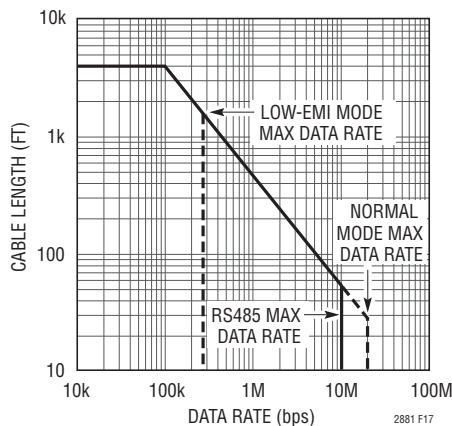


Figure 17. Cable Length vs Data Rate

### RF, Magnetic Field Immunity

The LTM2881 has been independently evaluated and has successfully passed the RF and magnetic field immunity testing requirements per European Standard EN 55024, in accordance with the following test standards:

EN 61000-4-3 Radiated, Radio-Frequency, Electromagnetic Field Immunity

EN 61000-4-8 Power Frequency Magnetic Field Immunity

EN 61000-4-9 Pulsed Magnetic Field Immunity

Tests were performed using an unshielded test card designed per the data sheet PCB layout recommendations. Specific limits per test are detailed in Table 1.

Table 1

TEST	FREQUENCY	FIELD STRENGTH
EN 61000-4-3, Annex D	80MHz to 1GHz	10V/m
	1.4MHz to 2GHz	3V/m
	2GHz to 2.7GHz	1V/m
EN 61000-4-8, Level 4	50Hz and 60Hz	30A/m
EN 61000-4-8, Level 5	60Hz	100A/m*
EN 61000-4-9, Level 5	Pulse	1000A/m

\*Non IEC Method

## TYPICAL APPLICATIONS

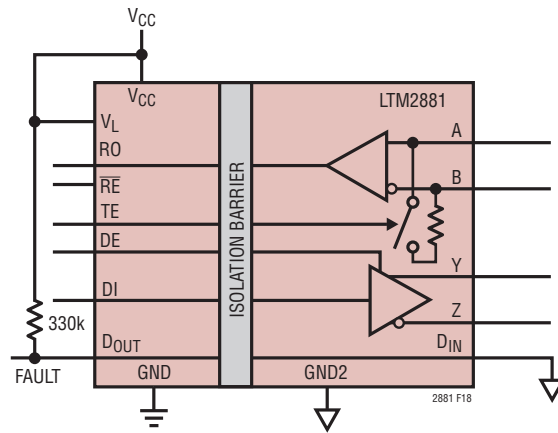


Figure 18. Isolated System Fault Detection

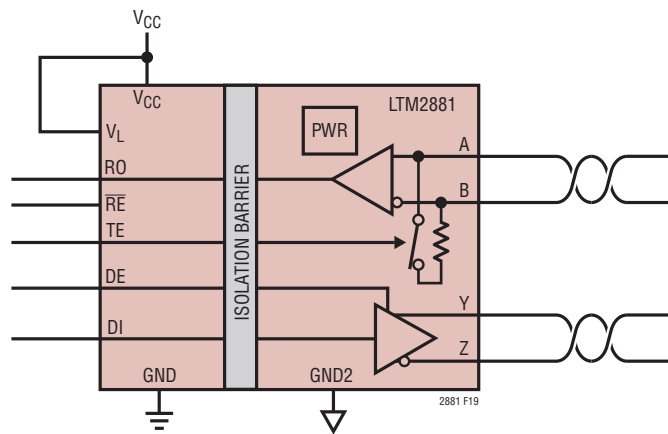


Figure 19. Full-Duplex RS485 Connection

TYPICAL APPLICATIONS

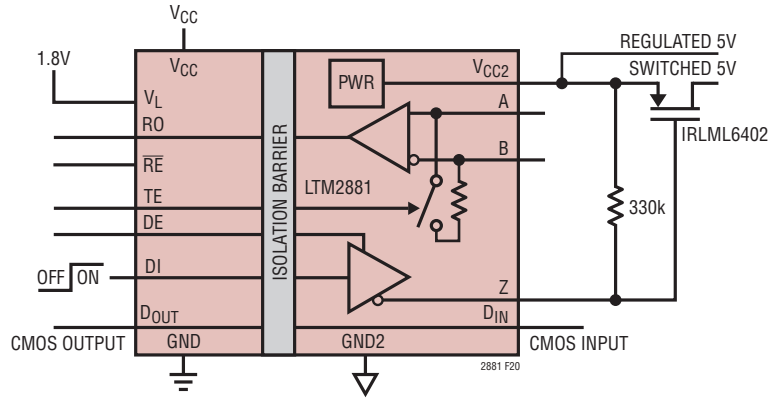


Figure 20. Switched 5V Power with Isolated CMOS Logic Connection with Low Voltage Interface

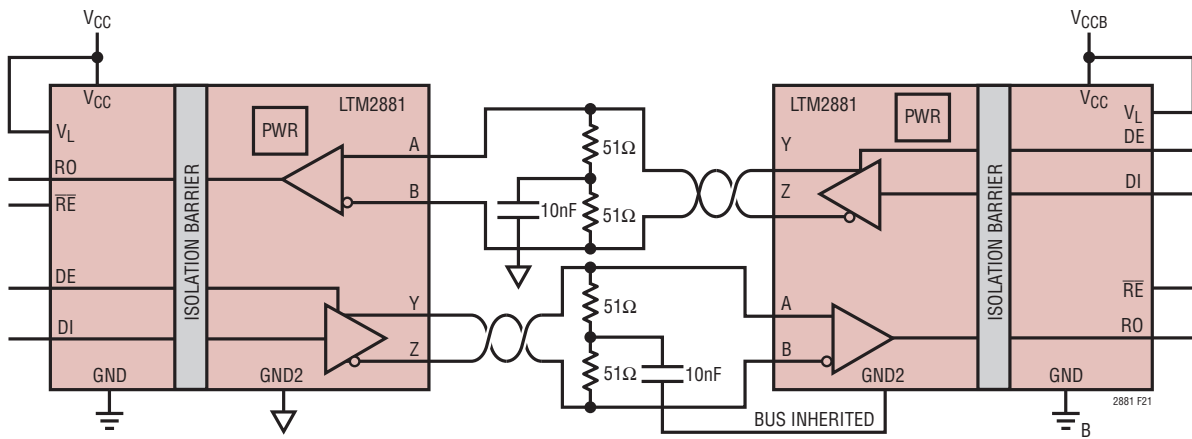
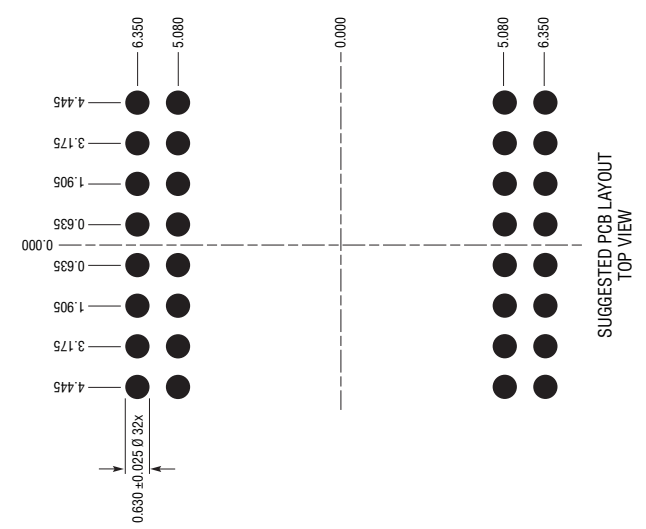
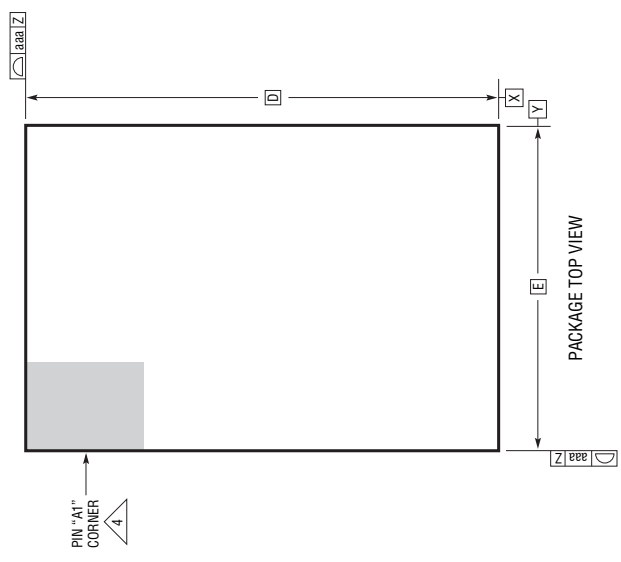
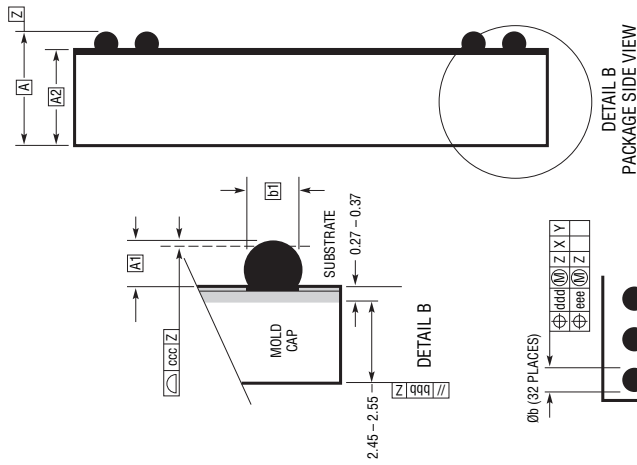
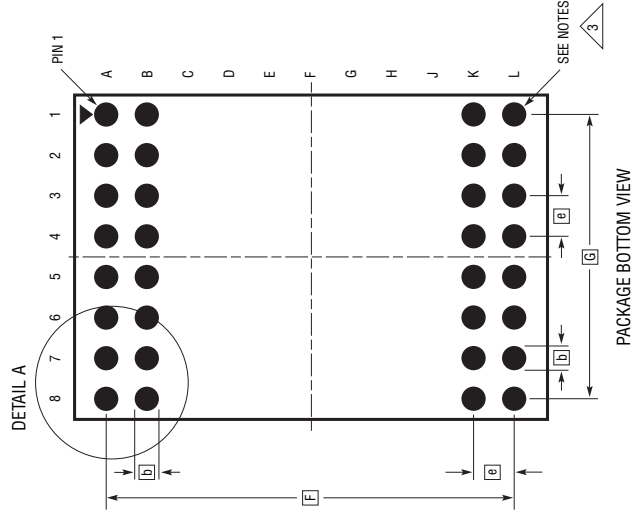


Figure 21. 4-Wire Full Duplex Self Biasing for Unshielded CAT5 Connection

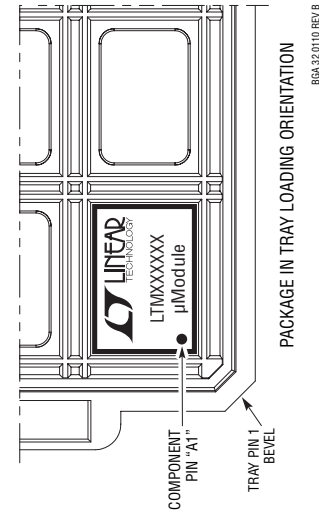
# PACKAGE DESCRIPTION

**BGA Package**  
**32-Lead (15mm × 11.25mm × 3.42mm)**  
 (Reference LTC DWG #05-08-1851 Rev B)



DIMENSIONS				
SYMBOL	MIN	NOM	MAX	NOTES
A	3.22	3.42	3.62	
A1	0.50	0.60	0.70	
A2	2.72	2.82	2.92	
b	0.73	0.78	0.83	
b1	0.60	0.63	0.66	
D	15.0			
E	11.25			
e	1.27			
F	12.70			
G	8.89			
aaa	0.15			
bbb	0.10			
ccc	0.20			
ddd	0.30			
eee	0.15			
TOTAL NUMBER OF BALLS: 32				

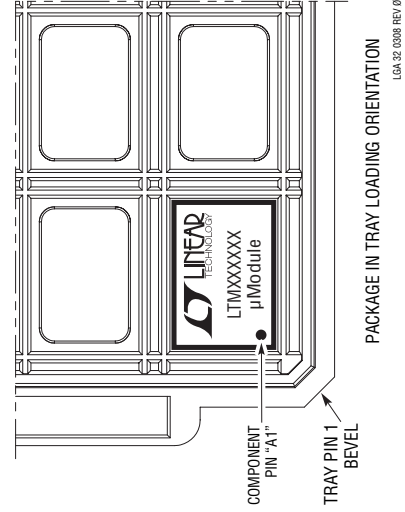
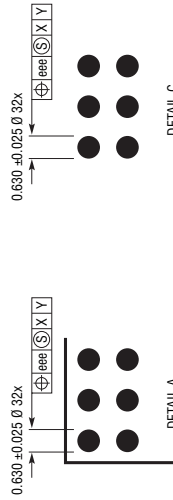
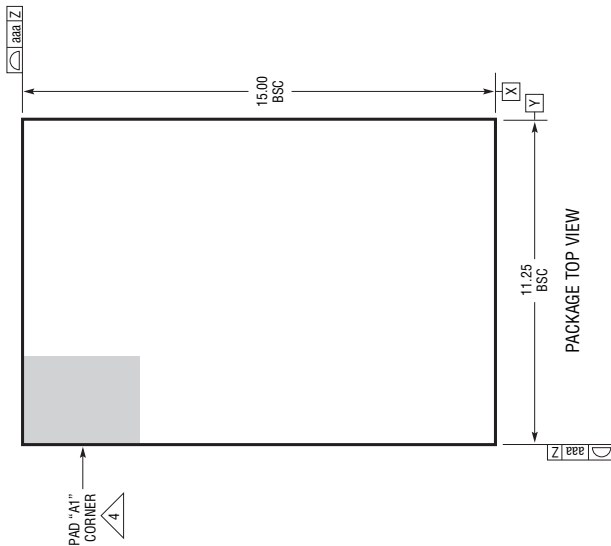
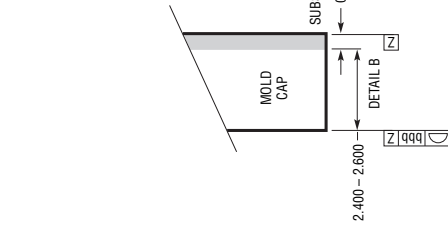
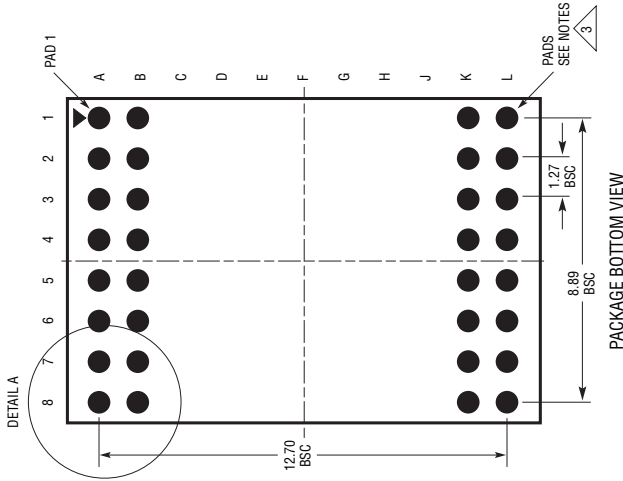
- NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M-1994
  2. ALL DIMENSIONS ARE IN MILLIMETERS
  3. BALL DESIGNATION PER JEDEC MS-028 AND JEP95
  4. DETAILS OF PIN #1 IDENTIFIER ARE OPTIONAL, BUT MUST BE LOCATED WITHIN THE ZONE INDICATED. THE PIN #1 IDENTIFIER MAY BE EITHER A MOLD OR MARKED FEATURE
  5. PRIMARY DATUM - Z - IS SEATING PLANE



BGA-320110 REV B

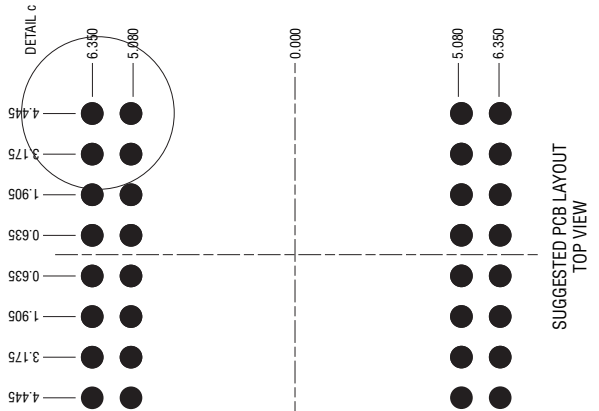
# PACKAGE DESCRIPTION

**LGA Package**  
**32-Lead (15mm × 11.25mm × 2.8mm)**  
 (Reference LTC DWG # 05-08-1773 Rev 0)



- NOTES:**
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M-1994
  2. ALL DIMENSIONS ARE IN MILLIMETERS
  3. LAND DESIGNATION PER JEDEC MO-222
  4. DETAILS OF PAD #1 IDENTIFIER ARE OPTIONAL, BUT MUST BE LOCATED WITHIN THE ZONE INDICATED. THE PAD #1 IDENTIFIER MAY BE EITHER A MOLD OR MARKED FEATURE
  5. PRIMARY DATUM -Z- IS SEATING PLANE
  6. THE TOTAL NUMBER OF PADS: 32

SYMBOL	TOLERANCE
aaa	0.10
bbb	0.10
eee	0.05



## REVISION HISTORY

REV	DATE	DESCRIPTION	PAGE NUMBER
A	3/10	Changes to Features, Description and Typical Application	1
		Add BGA Package to Pin Configuration, Order Information and Package Description Sections	2, 19
		Changes to LGA Package in Pin Configuration Section	2
		Changes to Electrical Characteristics Section	3
		Changes to Graphs G09, G13, G14	6, 7
		Update to Pin Functions	8
		Update to Applications Information	12
		Change to X-Axis on Figures 9a and 9b	13
		Update to Supply Current Section	14
		“PCB Layout Isolation Considerations” Section Replaced	15
		RF, Magnetic Field Immunity Section Added	16
		Changes to Related Parts	22
		B	8/10
C	5/11	HV-Grade parts removed. Reflected throughout the data sheet.	1-24
		Updated the PCB Layout section.	15, 16, 17
		Updated the Related Parts.	24

## TYPICAL APPLICATION

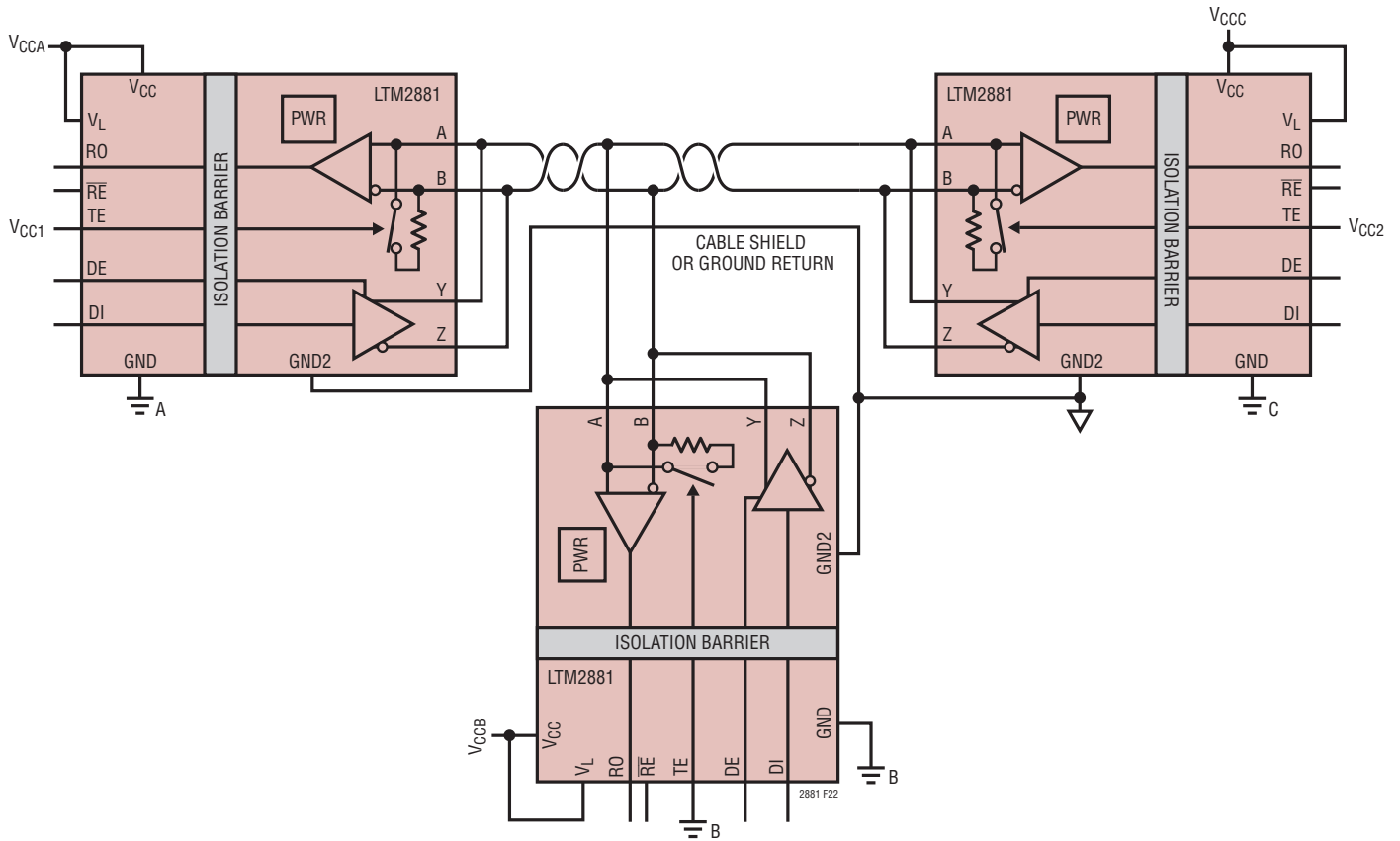


Figure 22. Multi-Node Network with End Termination and Single Ground Connection on Isolation Bus

## RELATED PARTS

PART NUMBER	DESCRIPTION	COMMENTS
LTM2882	Dual Isolated RS232 $\mu$ Module Transceiver + Power	1Mbps, $\pm 10\text{kV}$ HBM ESD, $2500V_{\text{RMS}}$
LTC1535	Isolated RS485 Transceiver	$2500V_{\text{RMS}}$ Isolation in Surface Mount Package
LT1785	$\pm 60\text{V}$ Fault-Protected Transceiver	Half Duplex
LT1791	$\pm 60\text{V}$ Fault-Protected Transceiver	Full Duplex
LTC2861	20Mbps RS485 Transceivers with Integrated Switchable Termination	Full Duplex $15\text{kV}$ ESD
LTM2883	SPI/Digital $\mu$ Module Isolator with Adjustable $\pm 12.5\text{V}$ and $5\text{V}$ Regulated Power	Up to $10\text{MHz}$ , $\pm 10\text{kV}$ HBM ESD, $2500V_{\text{RMS}}$ Isolation
LTC2870/ LTC2871	RS232/RS485 Multiprotocol Transceivers with Integrated Termination	20Mbps RS485 and 500kbps RS232, $\pm 26\text{kV}$ ESD, $3\text{V}$ to $5\text{V}$ Operation