# DPE8X16A

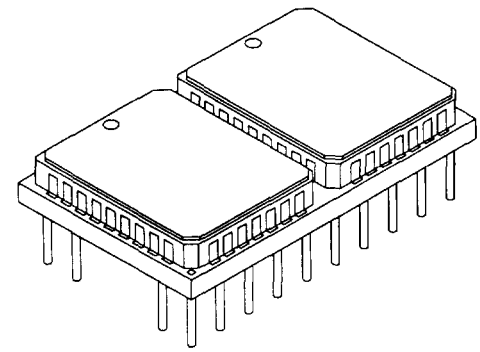
## 8K X 16 CMOS EEPROM HALF-PAC

### DESCRIPTION:

The DPE8X16A is a high-performance Electrically Erasable and Programmable Read Only Memory (EEPROM) module and may be organized as 8K X 16 or 16K X 8.

The module is built with two low-power CMOS 8K X 8 EEPROMs. The two chip enables are used for individual BW* selection. The DPE8X16A is ideally suited for those computer systems having 16-bit architectures.

The DPE8X16A contains a 32-BW page register to allow writing of up to 32 BWs simultaneously. During a write cycle, the address and 1 to 32 BWs of data are internally latched, freeing the address and data bus for other operations. Following the initiation of a write cycle, the module will automatically write the latched data using an internal control timer. The end of a write cycle can be detected by $\overline{DATA}$ Polling of the most significant data bit in each byte. Once the end of a write cycle has been detected, a new access for a read or write can begin.

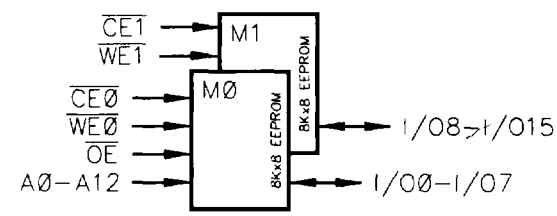


### FEATURES:

- Fast Access Times: 55, 70, 90, 120, 150, 200, 250ns
- Automatic Page Write Operation
  - Internal Address and Data Latches
  - Internal Control Timer
- Fast Write Cycle Times
  - Page Write Cycle Time: 10ms maximum
  - 1 to 32 BW* Page Write Operation
- $\overline{DATA}$ Polling for END of Write Detection
- High Reliability CMOS Technology
  - Endurance: $10^4$ Cycles
  - Data Retention: 10 years
- Single +5V Power Supply, ±10% Tolerance
- CMOS and TTL Compatible Inputs and Outputs
- Available with All Semiconductor Components Compliant to MIL-STD-883; Class B
- 40-Pin PGA (Grid Array) Package

* Byte or Word (BW)

### FUNCTIONAL BLOCK DIAGRAM

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| PIN NAMES | |
|---|---|
| A0 - A12 | Address Inputs |
| I/O0 - I/O15 | Data In/Out |
| $\overline{CE0}$, $\overline{CE1}$ | Chip Enables |
| $\overline{WE0}$, $\overline{WE1}$ | Write Enables |
| $\overline{OE}$ | Output Enable |
| $V_{DD}$ | Power (+5V) |
| $V_{SS}$ | Ground |
| N.C. | No Connect |

### PIN-OUT DIAGRAM

(TOP VIEW)

| | | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|
| $\overline{CE0}$ | 1 | I/O6 | 11 | 21 | I/O7 | 31 | VDD |
| A9 | 2 | I/O5 | 12 | 22 | I/O2 | 32 | AØ |
| A10 | 3 | I/O4 | 13 | 23 | I/O1 | 33 | A1 |
| A11 | 4 | I/O3 | 14 | 24 | I/OØ | 34 | A2 |
| A12 | 5 | $\overline{OE}$ | 15 | 25 | A3 | 35 | A4 |
| N.C. | 6 | $\overline{WE1}$ | 16 | 26 | $\overline{WE0}$ | 36 | A5 |
| N.C. | 7 | I/O14 | 17 | 27 | I/O15 | 37 | A6 |
| N.C. | 8 | I/O13 | 18 | 28 | I/O10 | 38 | A7 |
| N.C. | 9 | I/O12 | 29 | 29 | I/O9 | 39 | A8 |
| VSS | 10 | I/O11 | 20 | 30 | I/O8 | 40 | $\overline{CE1}$ |

| RECOMMENDED OPERATING RANGE[1] | | | | | |
|---|---|---|---|---|---|
| Symbol | Characteristic | Min. | Typ. | Max. | Unit |
| $V_{DD}$ | Supply Voltage | 4.5 | 5.0 | 5.5 | V |
| $V_{IH}$ | Input HIGH Voltage | 2.2 | | $V_{DD}$+0.3 | V |
| $V_{IL}$ | Input LOW Voltage | -0.1[2] | | 0.8 | V |

| ABSOLUTE MAXIMUM RATINGS[3] | | | |
|---|---|---|---|
| Symbol | Parameter | Value | Unit |
| $T_{STC}$ | Storage Temperature | -65 to + 150 | °C |
| $T_{BIAS}$ | Temperature Under Bias | -55 to + 125 | °C |
| $V_{DD}$ | Supply Voltage[1] | -0.3 to + 6.25 | V |
| $V_{I/O}$ | Input/Output Voltage[1] | -0.3[2] to +6.25 | V |

| AC TEST CONDITIONS | |
|---|---|
| Input Pulse Levels | 0V to 3.0V |
| Input Pulse Rise and Fall Times | 5ns* |
| Input and Output Timing Reference Levels | 1.5V |

* Transition between 0.8V and 2.2V.

| OUTPUT LOAD | | |
|---|---|---|
| Float | $C_L$ | Parameters Measured |
| 1 | 100 pF | except $t_{DF}$ |
| 2 | 5 pF | $t_{DF}$ |

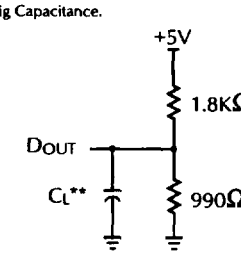
| TRUTH TABLE | | | | |
|---|---|---|---|---|
| Mode | $\overline{CE}$ | $\overline{OE}$ | $\overline{WE}$ | I/O PIN |
| Standby | H | X | X | HIGH-Z |
| Read | L | L | H | $D_{OUT}$ |
| Write | L | H | L | $D_{IN}$ |
| Write Inhibit | X | L | X | HIGH-Z |
| Write Inhibit | X | X | H | HIGH-Z |

L = LOW H = HIGH X = Don't Care

| CAPACITANCE[4]: $T_A$ = 25°C, F = 1.0MHz | | | | |
|---|---|---|---|---|
| Symbol | Parameter | Max. | Unit | Condition |
| $C_{CE}$ | Chip Enable | 15 | pF | $V_{IN}$ = 0V |
| $C_{ADR}$ | Address Input | 35 | | |
| $C_{WE}$ | Write Enable | 15 | | |
| $C_{OE}$ | Output Enable | 35 | | |
| $C_{I/O}$ | Data Input/Output | 25 | | |

**Figure 1.** Output Load

** Including Probe and Jig Capacitance.




| DC OPERATING CHARACTERISTICS: Over the operating ranges. | | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| Symbol | Characteristics | Test Conditions | X 16 | | X 8 | | Unit |
| | | | Min. | Max. | Min. | Max. | |
| $I_{CC}$ | Operating Supply Current | $\overline{CE}$ = $\overline{OE}$ = $V_{IL}$, all I/O = 0mA f = $t_{RC}$ Min. | | 160 | | 90 | mA |
| $I_{SB1}$ | $V_{DD}$ Current Standby (TTL) | $\overline{CE}$ = $V_{IH}$ | | 6 | | 6 | mA |
| $I_{SB2}$ | $V_{DD}$ Current Standby (CMOS) | $\overline{CE}$ = $V_{DD}$ -0.3Vdc | | 0.5 | | 0.5 | mA |
| $I_{IL}$ | Input Leakage Current | $V_{IN}$ = $V_{DD}$ Max. | -10 | 10 | -10 | 10 | µA |
| $I_{OL}$ | Output Leakage Current | $V_{OUT}$ = $V_{DD}$ Max. | -10 | 10 | -20 | 20 | µA |
| $V_{IL}$ | Input Voltage Low | | -0.1 | 0.8 | -0.1 | 0.8 | V |
| $V_{IH}$ | Input Voltage High | | 2.0 | $V_{DD}$+0.3 | 2.0 | $V_{DD}$+0.3 | V |
| $V_{OL}$ | Output Voltage Low | $I_{OUT}$ = 2.1mA | | 0.45 | | 0.45 | V |
| $V_{OH}$ | Output Voltage High | $I_{OUT}$ = -400µA | 2.4 | | 2.4 | | V |

| AC OPERATING CONDITIONS AND CHARACTERISTICS - READ CYCLE: Over operating ranges [6,7] | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|
| No. | Symbol | Parameter | -55 | | -70 | | -90 | | -120 | | Unit |
| | | | Min. | Max. | Min. | Max. | Min. | Max. | Min. | Max. | |
| 1 | $t_{ACC}$ | Address to Output Valid | | 55 | | 70 | | 90 | | 120 | ns |
| 2 | $t_{CE}$ | Chip Enable to Output Valid | | 55 | | 70 | | 90 | | 120 | ns |
| 3 | $t_{OE}$ | Output Enable to Output Valid | | 30 | | 35 | | 40 | | 50 | ns |
| 4 | $t_{DF}$ | Chip Enable or Output Enable to Output Float [4] | | 30 | | 35 | | 40 | | 50 | ns |
| 5 | $t_{OH}$ | Output Hold from Chip Enable, Output Enable, or Address, Whichever Occurs First | 0 | | 0 | | 0 | | 0 | | ns |

| AC OPERATING CONDITIONS AND CHARACTERISTICS - READ CYCLE: Over operating ranges [6,7] | | | | | | | | | Unit |
|---|---|---|---|---|---|---|---|---|---|
| No. | Symbol | Parameter | -150 | | -200 | | -250 | | |
| | | | Min. | Max. | Min. | Max. | Min. | Max. | |
| 1 | $t_{ACC}$ | Address to Output Valid | | 150 | | 200 | | 250 | ns |
| 2 | $t_{CE}$ | Chip Enable to Output Valid | | 150 | | 200 | | 250 | ns |
| 3 | $t_{OE}$ | Output Enable to Output Valid | | 70 | | 80 | | 100 | ns |
| 4 | $t_{DF}$ | Chip Enable or Output Enable to Output Float [4] | | 50 | | 60 | | 60 | ns |
| 5 | $t_{OH}$ | Output Hold from Chip Enable, Output Enable, or Address, Whichever Occurs First | 0 | | 0 | | 0 | | ns |

| AC OPERATING CONDITIONS AND CHARACTERISTICS - WRITE CYCLE: Over operating ranges [6,7] | | | | | |
|---|---|---|---|---|---|
| No. | Symbol | Parameter | MIN. | MAX. | Unit |
| 6 | $t_{WC}$ | Write Cycle Time | | 10 | ms |
| 7 | $t_{AS}$ | Address Set-up Time * | 0 | | ns |
| 8 | $t_{AH}$ | Address Hold Time | 50 | | ns |
| 9 | $t_{CS}$ | Chip Select Set-up Time | 0 | | ns |
| 10 | $t_{CH}$ | Chip Select Hold Time | 0 | | ns |
| 11 | $t_{WP}$ | Write Pulse Width ($\overline{CE}$ or $\overline{OE}$) | 100 | 1000 | ns |
| 12 | $t_{DS}$ | Data Set-up Time | 50 | | ns |
| 13 | $t_{DH}$ | Data Hold Time | 0 | | ns |
| 14 | $t_{DV}$ | Time to Data Valid | | 1 | µs |
| 15 | $t_{OES}$ | $\overline{OE}$ Setup Time | 0 | | ns |
| 16 | $t_{OEH}$ | $\overline{OE}$ Hold Time | 0 | | ns |
| 17 | $t_{WPH}$ | Write Pulse Width High | 50 | | ns |
| 18 | $t_{BLC}$ | Byte Load Cycle Time | 150 | | ns |
| 19 | $t_{PLW}$ | Page Load Width | | 150 | µs |

* Valid for both Read and Write Cycles.

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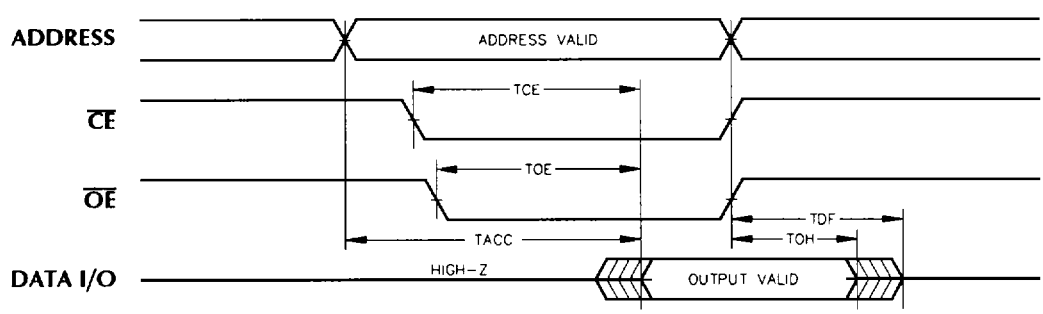
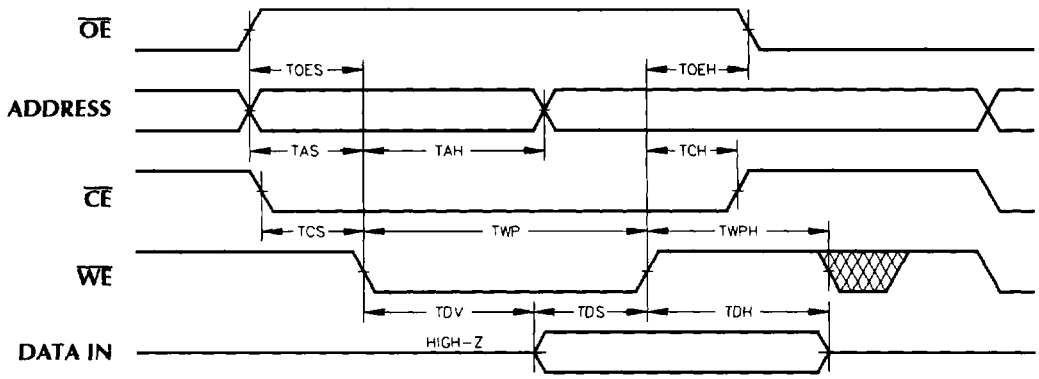
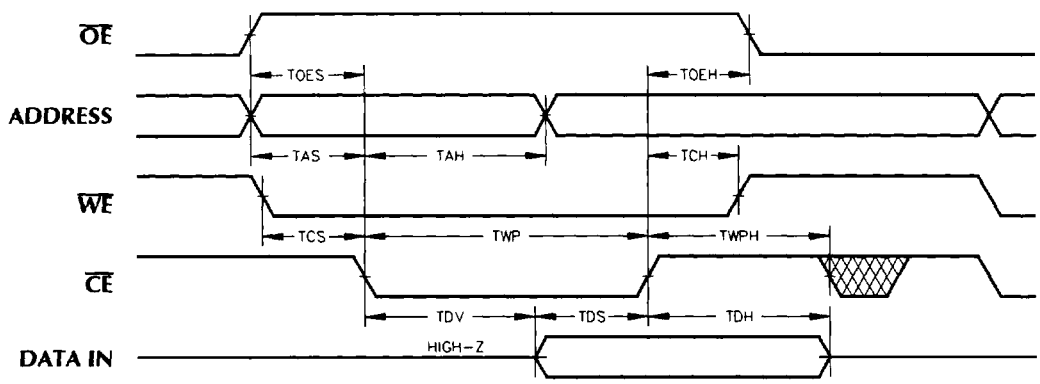
**READ CYCLE**



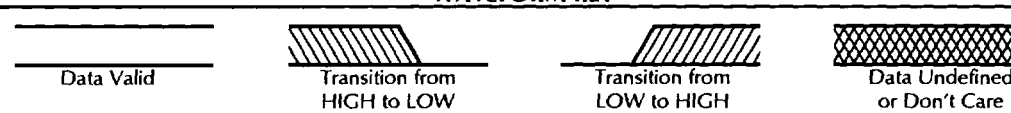
## WRITE CYCLE 1: $\overline{WE}$ Controlled.



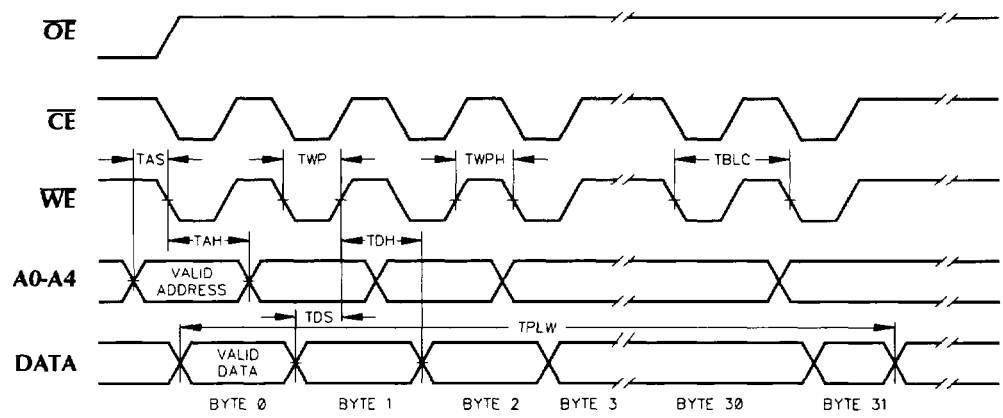

## WRITE CYCLE 2: $\overline{CE}$ Controlled.



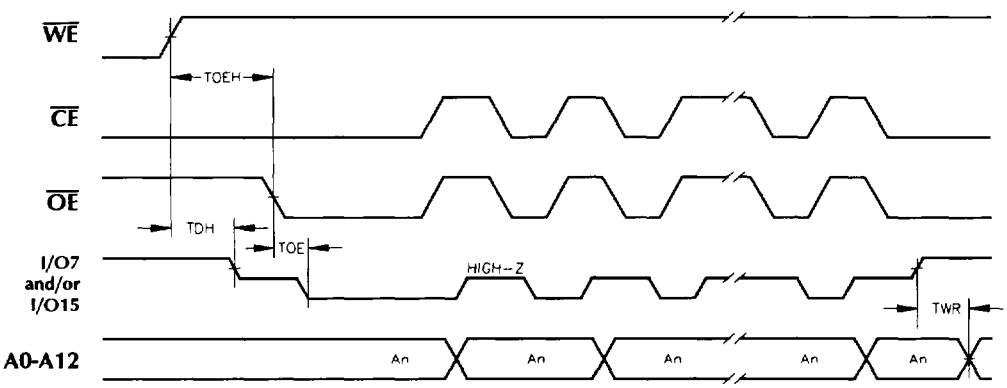

## WAVEFORM KEY



## PAGE MODE WRITE WAVEFORM




## DATA POLLING WAVEFORM

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## DEVICE OPERATION

**READ:** The DPE8X16A is accessed like a Static RAM. When $\overline{CE}$ and $\overline{OE}$ are low and $\overline{WE}$ is high, the data stored at the memory location determined by address pins is asserted on the outputs. The outputs are put in the high impedance state whenever $\overline{CE}$ or $\overline{OE}$ is high. This dual line control gives designers flexibility in preventing bus contention.

**WRITE:** A low pulse on the $\overline{WE}$ or $\overline{CE}$ input with $\overline{CE}$ or $\overline{WE}$ low *(respectively)* and $\overline{OE}$ high initiates a write cycle. The address is latched on the falling edge of $\overline{CE}$ or $\overline{WE}$, whichever occurs last. The data is latched by the first rising edge of $\overline{CE}$ or $\overline{WE}$. Once a BW* write has been started it will automatically time itself to completion.

**PAGE WRITE MODE:** The page write operation of the DPE8X16A allows 1 to 32 BWs of data to be loaded into the device and then simultaneously written during the internal programming period. After the first data BW has been loaded into the device, successive BWs may be loaded in the same manner. Each new BW to be written must have its high to low transition on $\overline{WE}$ (or $\overline{CE}$) within 150µs of the low to high transition of $\overline{WE}$ (or $\overline{CE}$) of the preceding BW. If a high to low transition is not detected within 150µs of the last low to high transition, the load period will end and the internal programming period will start. A5 to A12 specify the page address. The page address must be valid during each high to low transition of $\overline{WE}$ (or $\overline{CE}$). A0 to A4 are used to specify which BWs within the page are to be written. The BWs may be loaded in any order and may be changed within the same load period. Only BWs which are specified for writing will be written; unnecessary cycling of other BWs within the page does not occur.

**$\overline{DATA}$ POLLING:** The DPE8X16A features $\overline{DATA}$ Polling to indicate the end of a write cycle. During a byte or page write cycle an attempted read of the last byte written will result in the compliment of the written data on I/O7 and/or I/O15. Once the the write cycle has been completed, true data is valid on all outputs, and the next cycle may begin. $\overline{DATA}$ Polling may begin at any time during the write cycle.

* Byte or Word

## ORDERING INFORMATION

DP E8X16 A – XX X

PREFIX | DEVICE TYPE | PACKAGE | SPEED | GRADE

| | | |
|---|---|---|
| C | COMMERCIAL | 0°C to +70°C |
| I | INDUSTRIAL | -40°C to +85°C |
| M | MILITARY | -55°C to +125°C |
| B* | MIL-PROCESSED | -55°C to +125°C |

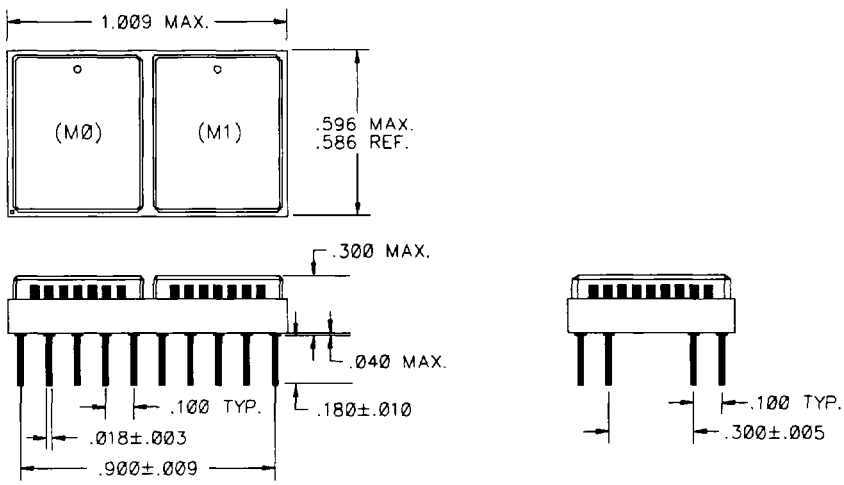
| | | |
|---|---|---|
| 55 | 55ns | (COMMERCIAL ONLY) |
| 70 | 70ns | |
| 90 | 90ns | |
| 12 | 120ns | |
| 15 | 150ns | |
| 20 | 200ns | |
| 25 | 250ns | |

A 40-PIN PGA MODULE

CMOS EEPROM 8Kx16 OR 16Kx8

* B grade modules are constructed with 883 devices.

## MECHANICAL DIAGRAMS




**NOTES:**

1. All voltages are with respect to $V_{SS}$.
2. *-1.0V min. for pulse width less than 20ns ($V_{IL}$ min. = -0.3V at DC level).*
3. Stresses greater than those under **ABSOLUTE MAXIMUM RATINGS** may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. *Exposure to absolute maximum rating conditions for extended periods may affect reliability.*
4. This parameter is guaranteed and not 100% tested.
5. Transition is measured at the point of ±500mV from steady state voltage.
6. When $\overline{OE}$ and $\overline{CE}$ are LOW and $\overline{WE}$ is HIGH, I/O pins are in the output state; and input signals of opposite phase to the outputs must not be applied.
7. The outputs are in a high impedance state when $\overline{WE}$ is LOW.

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