

FEATURES

Dual Serial Input, Voltage Output DACs
 Single +5 V Supply
 0.004% THD+N (typ)
 Low Power: 50 mW (typ)
 108 dB Channel Separation (min)
 Operates at 8× Oversampling
 16-Pin Plastic DIP or SOIC Package

APPLICATIONS

Portable Compact Disc Players
 Portable DAT Players and Recorders
 Automotive Compact Disc Players
 Automotive DAT Players
 Multimedia Workstations

PRODUCT DESCRIPTION

The AD1868 is a complete dual 18-bit DAC offering excellent performance while requiring a single +5 V power supply. It is fabricated on Analog Devices' ABCMOS wafer fabrication process. The monolithic chip includes CMOS logic elements, bipolar and MOS linear elements, and laser-trimmed thin-film resistor elements. Careful design and layout techniques have resulted in low distortion, low noise, high channel separation, and low power dissipation.

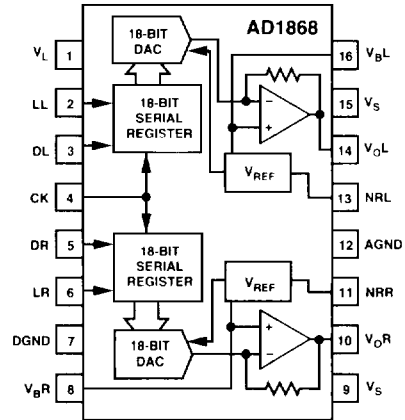
The DACs on the AD1868 chip employ a partially segmented architecture. The first three MSBs of each DAC are segmented into seven elements. The 15 LSBs are produced using standard R-2R techniques. The segments and R-2R resistors are laser trimmed to provide extremely low total harmonic distortion. The AD1868 requires no deglitcher or trimming circuitry. Low noise is achieved through the use of two noise-reduction capacitors.

Each DAC is equipped with a high performance output amplifier. These amplifiers achieve fast settling and high slew rate, producing ± 1 V signals at load currents up to ± 1 mA. The buffered output signal range is 1.5 V to 3.5 V. Reference voltages of 2.5 V are provided, eliminating the need for "False Ground" networks.

A versatile digital interface allows the AD1868 to be directly connected to all digital filter chips. Fast CMOS logic elements allow for an input clock rate of up to 13.5 MHz. This allows for operation at 2×, 4×, 8×, or 16× the sampling frequency for each channel. The digital input pins of the AD1868 are TTL and +5 V CMOS compatible.

*Protected by U.S. Patent Numbers: 3,961,326; 4,141,004; 4,349,811; 4,857,862; and patents pending.

FUNCTIONAL BLOCK DIAGRAM



The AD1868 operates on +5 V power supplies. The digital supply, V_L , can be separated from the analog supply, V_S , for reduced digital feedthrough. Separate analog and digital ground pins are also provided. In systems employing a single +5 volt power supply, V_L and V_S should be connected together. In battery operated systems, operation will continue even with reduced supply voltage. Typically, the AD1868 dissipates 50 mW.

The AD1868 is packaged in either a 16-pin plastic DIP or a 16-pin plastic SOIC package. Operation is guaranteed over the temperature range of -35°C to $+85^\circ\text{C}$ and over the voltage supply range of 4.75 V to 5.25 V.

PRODUCT HIGHLIGHTS

1. Single-supply operation ($v +5$ V).
2. 50 mW power dissipation (typical).
3. THD+N is 0.004% (typical).
4. Signal-to-Noise Ratio is 97.5 dB (typical).
5. 108 dB channel separation (minimum).
6. Compatible with all digital filter chips.
7. 16-pin DIP and 16-pin SOIC packages.
8. No deglitcher required.
9. No external adjustments required.

AD1868—SPECIFICATIONS (typical at $T_A = +25^\circ\text{C}$ and $+5\text{ V}$ supplies unless otherwise noted)

	Min	Typ	Max	Units
RESOLUTION		18		Bit
DIGITAL INPUTS	V_{IH}			V
	V_{IL}		0.8	V
	$I_{IH}, V_{IH} = V_L$	1.0		μA
	$I_{IL}, V_{IL} = \text{DGND}$	1.0		μA
Maximum Clock Input Frequency	13.5			MHz
ACCURACY				
Gain Error		+1		% of FSR
Gain Matching		+1		% of FSR
Midscale Error		± 15		mV
Midscale Error Matching		± 10		mV
Gain Linearity Error		+3		dB
DRIFT (0°C to $+70^\circ\text{C}$)				
Gain Drift		± 100		ppm/ $^\circ\text{C}$
Midscale Drift		± 100		$\mu\text{V}/^\circ\text{C}$
TOTAL HARMONIC DISTORTION + NOISE				
0 dB, 990.5 Hz	AD1868N	0.004	0.008	%
	AD1868N-J	0.004	0.006	%
20 dB, 990.5 Hz	AD1868N	0.020	0.08	%
	AD1868N-J	0.020	0.08	%
60 dB, 990.5 Hz	AD1868N	2.0	5.0	%
	AD1868N-J	2.0	5.0	%
CHANNEL SEPARATION 1 kHz, 0 dB	108	NIL*		dB
SIGNAL-TO-NOISE RATIO (with A-Weight Filter)	95	97.5		dB
D-RANGE (with A-Weight Filter)	86	92		dB
OUTPUT				
Voltage Output Pins (V_{OL}, V_{OR})				
Output Range (+3%)		± 1		V
Output Impedance		0.1		Ω
Load Current		± 1		mA
Bias Voltage Pins (V_{BL}, V_{BR})				
Output Voltage		+2.5		V
Output Impedance		350		Ω
POWER SUPPLY				
Specification, V_1 and V_S	4.75	5	5.25	V
Operation, V_1 and V_S	3.5		5.25	V
$\pm I_1, V_1$ and $V_S = 5\text{ V}$		10	14	mA
POWER DISSIPATION		50	70	mW
TEMPERATURE RANGE				
Specification	0	25	70	$^\circ\text{C}$
Operation	-35		85	$^\circ\text{C}$
Storage	-60		100	$^\circ\text{C}$

*Above 115 dB.

Specifications subject to change without notice.

ORDERING GUIDE

Model	THD + N @ F_S	SNR	Package Option*
AD1868N	0.008%	95 dB	N-16
AD1868R	0.008%	95 dB	R-16
AD1868N-J	0.006%	95 dB	N-16
AD1868R-J	0.006%	95 dB	R-16

*N = Plastic DIP; R = SOIC. For outline information see Package Information section.