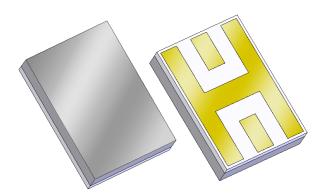
## Applications

- For GPS L1 Applications
- For high-selectivity applications





### Functional Block Diagram

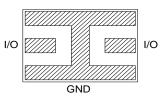
• Usable bandwidth 25 MHz

**Product Features** 

- Low loss
- High selectivity
- Single-ended operation
- Ceramic chip-scale Package (CSP)
- Small Size
- Hermetic **RoHS** compliant, **Pb**-free

### Pin Configuration

Pin # SE-Balanced	Description
I/O	Input/Output
GND	Ground



Overall width, length, and thickness are the only critical dimensions. All other dimensions are for reference only.

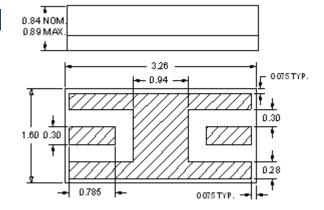
Dimensions shown are nominal in millimeters All tolerances are  $\pm 0.13$ mm except overall length and width  $\pm 0.25$ mm

#### Body: Sapphire Package: Alumina

Terminations: Au plating 0.5 - 2.5μm, over a 2.0 – 6.0 μm Ni plating

## **Ordering Information**

Part No.	Description
880094	packaged part
880094 Eval Board	evaluation board





## **Specifications**

# **Electrical Specifications**<sup>(1)</sup>

Specified Temperature Range: <sup>(2)</sup> -40 to +85 °C

Parameter <sup>(3)</sup>	Conditions	Min	Typical <sup>(4)</sup>	Max	Units
Center Frequency		-	1575.42	-	MHz
Maximum Insertion Loss	@ 1575.42 MHz	-	1.8	2.5	dB
3dB Bandwidth	Reference loss at 1575.42 MHz	30	35	-	MHz
20dB Lower Frequency Edge		1543.42	1548	-	MHz
20dB Upper Frequency Edge		-	1602	1607.42	MHz
VSWR	@ 1575.42 MHz	-	1.6	2.0	-
Source Impedance (single-ended)		-	50	-	Ω
Load Impedance (single-ended) <sup>(5)</sup>		-	50	-	Ω

Notes:

1. All specifications are based on the TriQuint schematic for the main reference design shown on page 3

2. In production, devices will be tested at room temperature to a guardbanded specification to ensure electrical compliance over temperature

3. Electrical margin has been built into the design to account for the variations due to temperature drift and manufacturing tolerances

4. Typical values are based on average measurements at room temperature

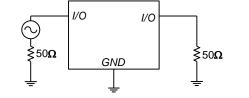
5. This is the optimum impedance in order to achieve the performance shown

## **Reference Design**



## Schematic

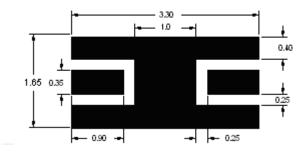




```
50 Ω
Single-ended
Input
```

## PC Board

## **Mounting Configuration**



Notes:

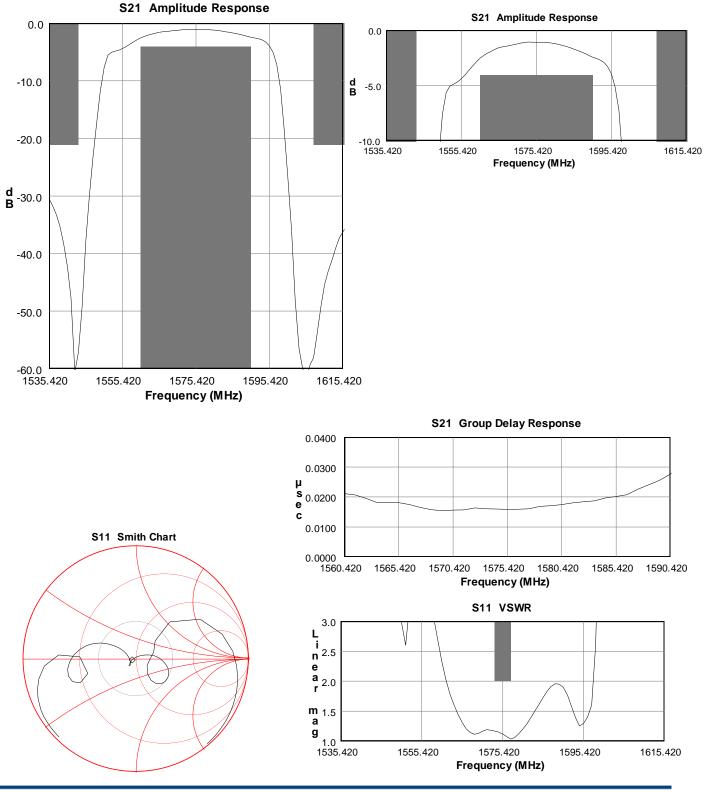
1. All dimensions are in millimeters.

2. This footprint represents a recommendation only.

#### Refer to **PCB Layout** for more information.



### Typical Performance (at room temperature)



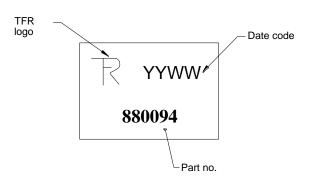
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Data Sheet: Rev B 12/2011 © 2011 TriQuint Semiconductor, Inc.



### Mechanical Information

## Marking



The date code consists of: YY = Iast digit of year, WW = 2 digit week

## **Tape and Reel Information**

Tape and Reel available upon request EIA-481

Tinning available per J-STD-001

### **Absolute Maximum Ratings**

Parameter	Rating
Operating Temperature	-40 to +85 °C
Storage Temperature	-55 to +100 °C
Maximum Input Power	+23 dBm

Operation of this device outside the parameter ranges given above may cause permanent damage.



**Product Compliance Information** 

### **ESD** Information



JEDEC Standard JESD22-A115

Value:	Passes $\geq$ 8000 V min.
Test:	Human Body Model (HBM)
Standard:	JEDEC Standard JESD22-A114
Value:	Passes $\geq 1600$ V min.
Test:	Machine Model (MM)

Refer to **ESD Sensitivity** for data

Standard:

### **Solderability**

Compatible with the latest version of J-STD-020, lead free solder, 260°C

Refer to Soldering Profile for recommended guidelines.

This part is compliant with EU 2002/95/EC RoHS directive (Restrictions on the Use of Certain Hazardous Substances in Electrical and Electronic Equipment).

This product also has the following attributes:

- Halogen Free (Chlorine, Bromine)
- Antimony Free
- TBBP-A ( $C_{15}H_{12}Br_4O_2$ ) Free
- PFOS Free
- SVHC Free

### **Contact Information**

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