

## OUTLINE

The R1151N Series are CMOS-based boost type voltage regulator ICs with high output voltage accuracy, low supply current, and high ripple rejection. Each of these voltage regulator controllers consists of a voltage reference unit, an error amplifier, comparators, resistors for output and reset voltage setting, a current limit protection circuit, and a chip enable circuit.

In addition to low consumption current by CMOS process, the chip enable function prolongs the battery life. Dynamic response and ripple rejection of the R1151N Series are excellent, further these are low noise type, plus maximum operating input voltage tolerance is up to 18.5V, thus these ICs are very suitable for the power supply for handheld equipment and other power management applications using AC adapter input voltage.

The output voltage of these ICs is internally fixed with high accuracy. Since the package for these ICs is SOT-23-6 (Mini-mold) package, high density mounting of the ICs on boards is possible.

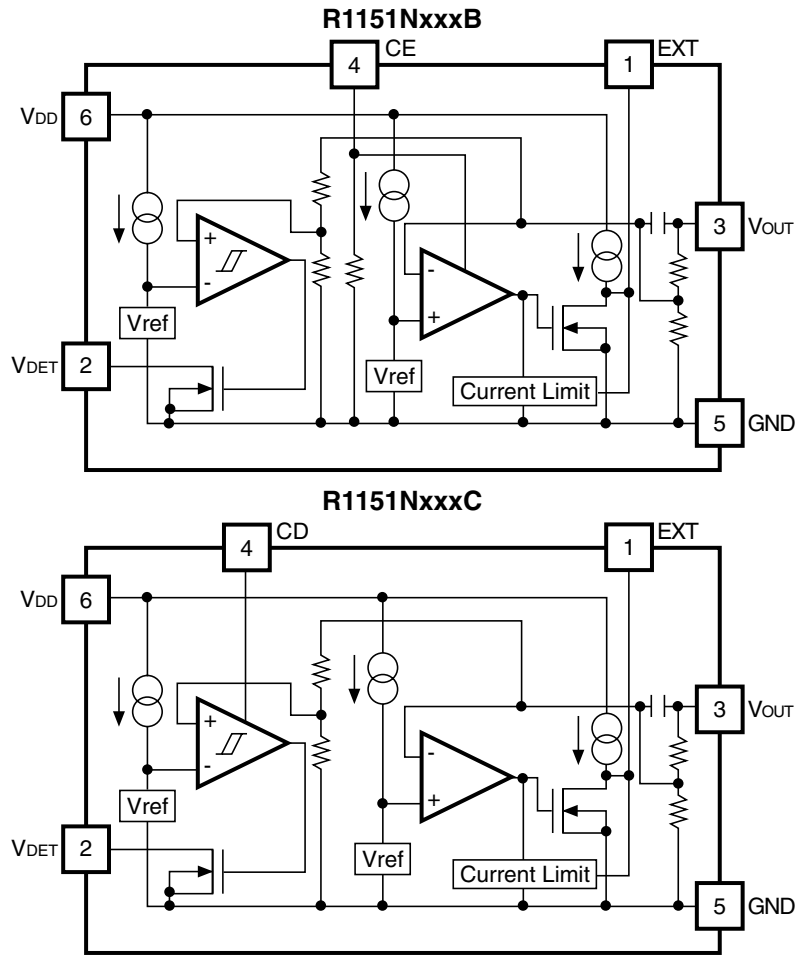
## FEATURES

- Ultra-Low Supply Current ..... Typ.  $70\mu\text{A}$  ( $I_{\text{OUT}}=0\text{mA}$ )
- Standby Mode ..... Typ.  $0.1\mu\text{A}$
- Low Dropout Voltage ..... Typ.  $0.1\text{V}$  ( $I_{\text{OUT}}=100\text{mA}$  \*Depends on External Transistor)
- High Ripple Rejection ..... Typ.  $60\text{dB}$  ( $f=1\text{kHz}$ )
- Low Temperature-Drift Coefficient of Output Voltage ..... Typ.  $\pm 100\text{ppm}/^\circ\text{C}$
- High Output Voltage Accuracy .....  $\pm 2.0\%$
- Excellent Dynamic Response
- Small Package ..... SOT-23-6 (Mini-mold)
- Output Voltage ..... Stepwise setting with a step of  $0.1\text{V}$  in the range of  $2.5\text{V}$  to  $9.0\text{V}$
- Built-in chip enable circuit (2 types; A: active low, B: active high)
- Output Capacitor ..... Tantalum type recommendation (or Ceramic+Series Resistor)
- Built-in output voltage detector ..... with delay (C version)
- Detector Threshold Tolerance .....  $\pm 2.5\%$
- Detector Threshold Voltage ..... Stepwise setting with a step of  $0.1\text{V}$  in the range of  $1.7\text{V}$  to  $8.0\text{V}$
- Operating Input Voltage ..... Max.  $18.5\text{V}$

## APPLICATIONS

- Power source for handheld equipment such as cameras and videos.
- Power source for home appliances.
- Power source for battery-powered equipment.

### BLOCK DIAGRAMS



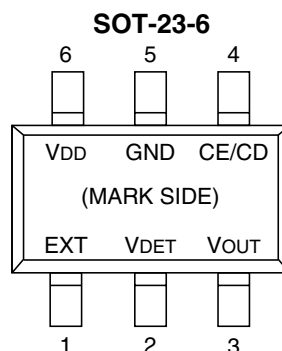
### SELECTION GUIDE

The output voltage, mask option code, and the taping type for the ICs can be selected at the user's request. The selection can be made with designating the part number as shown below;

R1151Nxxxx-xx ←Part Number  
 ↑ ↑ ↑  
 a b c

Code	Contents
a	Code Number for Voltage Setting
b	Setting <u>mask option</u> : A: with $\overline{CE}$ (active at "L" type) B: with CE (active at "H" type) C: with the pin for external capacitor to set the output delay of voltage detector
c	Designation of Taping Type : Ex. TR (Refer to Taping Specifications.)

## PIN CONFIGURATION



## PIN DESCRIPTIONS

Pin No.	Symbol	Description
1	EXT	External Transistor Drive Pin
2	V <sub>DET</sub>	Voltage Detector Output Pin
3	V <sub>OUT</sub>	Voltage Regulator Output pin
4	$\overline{\text{CE}}$ or CE	Chip Enable Pin (A/B version)
4	CD	Pin for External capacitor to set Output Delay of Voltage Detector (C version)
5	GND	Ground Pin
6	V <sub>DD</sub>	Input Pin

## ABSOLUTE MAXIMUM RATINGS

Symbol	Item	Rating	Unit
V <sub>IN</sub>	Input Voltage	20	V
V <sub>CE/CD</sub>	Input Voltage ( $\overline{\text{CE}}$ /CE/CD Pin)	-0.3 ~ V <sub>IN</sub> +0.3	V
V <sub>OUT</sub>	Output Voltage (V <sub>OUT</sub> Pin)	-0.3 ~ V <sub>IN</sub> +0.3	V
V <sub>EXT</sub>	Output Voltage (EXT Pin)	-0.3 ~ V <sub>IN</sub> +0.3	V
V <sub>DET</sub>	Output Voltage (V <sub>DET</sub> Pin)	-0.3 ~ V <sub>IN</sub> +0.3	V
I <sub>EXT</sub>	EXT Output Current	30	mA
P <sub>D</sub>	Power Dissipation	150	mW
T <sub>opt</sub>	Operating Temperature Range	-40 ~ 85	°C
T <sub>stg</sub>	Storage Temperature Range	-55 ~ 125	°C

## ELECTRICAL CHARACTERISTICS

## • R1151NxxxA/B

Topt=25°C

Symbol	Item	Conditions	Min.	Typ.	Max.	Unit
V <sub>OUT</sub>	Output Voltage	V <sub>IN</sub> = Set V <sub>OUT</sub> +1V I <sub>OUT</sub> = 50mA	V <sub>OUT</sub> ×0.98		V <sub>OUT</sub> ×1.02	V
I <sub>OUT</sub>	Output Current	V <sub>IN</sub> - V <sub>OUT</sub> = 1.0V		1 <sup>Note</sup>		A
ΔV <sub>OUT</sub> /ΔI <sub>OUT</sub>	Load Regulation	V <sub>IN</sub> = Set V <sub>OUT</sub> +1V 1mA ≤ I <sub>OUT</sub> ≤ 100mA	Refer to the Load Regulation Table			
V <sub>DIF</sub>	Dropout Voltage	I <sub>OUT</sub> = 100mA		0.1 <sup>Note</sup>	0.2	V
I <sub>SS</sub>	Supply Current	V <sub>IN</sub> = Set V <sub>OUT</sub> +1V, I <sub>OUT</sub> = 0mA		70	100	μA
I <sub>standby</sub>	Supply Current (Standby)	V <sub>IN</sub> = 18.5V		15		μA
I <sub>EXTleak</sub>	EXT Leakage Current				0.5	μA
ΔV <sub>OUT</sub> /ΔV <sub>IN</sub>	Line Regulation	Set V <sub>OUT</sub> +0.5V ≤ V <sub>IN</sub> ≤ 18.5V I <sub>OUT</sub> = 50mA	0.00	0.02	0.10	%/V
RR	Ripple Rejection	f = 1kHz, Ripple 0.5Vp-p V <sub>IN</sub> = Set V <sub>OUT</sub> +1V		60		dB
V <sub>IN</sub>	Input Voltage				18.5	V
ΔV <sub>OUT</sub> /ΔT	Output Voltage Temperature Coefficient	I <sub>OUT</sub> = 10mA -40°C ≤ Topt ≤ 85°C		±100		ppm /°C
I <sub>lim</sub>	Current Limit	Base Current I <sub>B</sub> of PNP Tr. V <sub>IN</sub> - V <sub>OUT</sub> = 1.0V	8		27	mA
I <sub>RPT</sub>	Short Current Limit	Base Current I <sub>B</sub> of PNP Tr. V <sub>OUT</sub> = 0V		0.7		mA
R <sub>UD</sub>	$\overline{\text{CE}}$ /CE Pull-up/down Resistance			2		MΩ
V <sub>CEH</sub>	$\overline{\text{CE}}$ /CE Input Voltage "H"		1.5		V <sub>IN</sub>	V
V <sub>CEL</sub>	$\overline{\text{CE}}$ /CE Input Voltage "L"		0.00		0.25	V
-V <sub>DET</sub>	Detector Threshold		-V <sub>DET</sub> ×0.975		-V <sub>DET</sub> ×1.025	V
V <sub>HYS</sub>	Detector Threshold Hysteresis Range		-V <sub>DET</sub> ×0.03	-V <sub>DET</sub> ×0.05	-V <sub>DET</sub> ×0.07	V
I <sub>OUT2</sub>	Output Current 2	V <sub>DD</sub> = 1.5V, V <sub>DS</sub> = 0.5V	2.0	5.0	10.0	mA
ΔV <sub>DET</sub> /ΔT	Detector Threshold Temperature Coefficient	-40°C ≤ Topt ≤ 85°C		±100		ppm /°C
t <sub>PLH</sub>	Output Delay Time				0.1	ms
V <sub>DDL</sub>	Minimum Operating Voltage			0.9	1.1	V

Note: This item depends on the capability of external PNP transistor. Use low saturation type transistor with hFE value range of 100 to 300.

## • R1151NxxxC

T<sub>opt</sub> = 25°C

Symbol	Item	Conditions	Min.	Typ.	Max.	Unit
V <sub>OUT</sub>	Output Voltage	V <sub>IN</sub> = Set V <sub>OUT</sub> +1V I <sub>OUT</sub> = 50mA	V <sub>OUT</sub> ×0.98		V <sub>OUT</sub> ×1.02	V
I <sub>OUT</sub>	Output Current	V <sub>IN</sub> - V <sub>OUT</sub> = 1.0V		1* <sup>Note1</sup>		A
ΔV <sub>OUT</sub> /ΔI <sub>OUT</sub>	Load Regulation	V <sub>IN</sub> = Set V <sub>OUT</sub> +1V 1mA ≤ I <sub>OUT</sub> ≤ 100mA	Refer to the Load Regulation Table			
V <sub>DIF</sub>	Dropout Voltage	I <sub>OUT</sub> = 100mA		0.1* <sup>Note1</sup>		V
I <sub>SS</sub>	Supply Current	V <sub>IN</sub> = Set V <sub>OUT</sub> +1V, I <sub>OUT</sub> = 0mA		70	100	μA
I <sub>EXTleak</sub>	EXT Leakage Current				0.5	μA
ΔV <sub>OUT</sub> /ΔV <sub>IN</sub>	Line Regulation	Set V <sub>OUT</sub> +0.5V ≤ V <sub>IN</sub> ≤ 18.5V I <sub>OUT</sub> = 50mA	0.00	0.02	0.10	%/V
RR	Ripple Rejection	f = 1kHz, Ripple 0.5Vp-p V <sub>IN</sub> = Set V <sub>OUT</sub> +1V		60		dB
V <sub>IN</sub>	Input Voltage				18.5	V
ΔV <sub>OUT</sub> /ΔT	Output Voltage Temperature Coefficient	I <sub>OUT</sub> = 10mA -40°C ≤ T <sub>opt</sub> ≤ 85°C		±100		ppm /°C
I <sub>lim</sub>	Current Limit	Base Current I <sub>B</sub> of PNP Tr. V <sub>IN</sub> - V <sub>OUT</sub> = 1.0V	8		27	mA
I <sub>RPT</sub>	Short Current Limit	Base Current I <sub>B</sub> of PNP Tr. V <sub>OUT</sub> = 0V		0.7		mA
-V <sub>DET</sub>	Detector Threshold		-V <sub>DET</sub> ×0.975		-V <sub>DET</sub> ×1.025	V
V <sub>HYS</sub>	Detector Threshold Hysteresis Range		-V <sub>DET</sub> ×0.03	-V <sub>DET</sub> ×0.05	-V <sub>DET</sub> ×0.07	V
I <sub>OUT2</sub>	Output Current 2	V <sub>DD</sub> = 1.5V, V <sub>DS</sub> = 0.5V	2.0	5.0	10.0	mA
ΔV <sub>DET</sub> /ΔT	Detector Threshold Temperature Coefficient	-40°C ≤ T <sub>opt</sub> ≤ 85°C		±100		ppm /°C
t <sub>PLH</sub>	Output Delay Time	CD=220pF* <sup>Note2</sup>	0.9	1.6	2.7	ms
V <sub>DDL</sub>	Minimum Operating Voltage			0.9	1.1	V

Note1: This item depends on the capability of external PNP transistor. Use low saturation type transistor with hFE value range of 100 to 300.

Note2: V<sub>DET</sub> pin is pulled-up to V<sub>DD</sub> via 470kΩ resistance. The time is between the rising edge of V<sub>OUT</sub> level from 0.9V to (+V<sub>DET</sub>)+2.0V and the reaching point to ((+V<sub>DET</sub>)+2.0V)/2 of the V<sub>DET</sub> output voltage.

**• Load Regulation Table**

Output Voltage $V_{OUT}$ (V)	Load Regulation $\Delta V_{OUT}/\Delta I_{OUT}$ (mV)	
	Typ.	Max.
2.5 to 3.3	20	60
3.4 to 5.0	30	90
5.1 to 7.0	40	130
7.1 to 9.0	50	160

**OPERATION**

In these ICs, fluctuation of Output Voltage,  $V_{OUT}$  is detected by the feed-back registers, and the result is compared with a reference voltage with the error amplifier and control the base current of an external PNP transistor so that a constant voltage is output. The base current is monitored with the base current limit circuit. If the base current may be too large, the protection circuit works, further, output voltage is monitored with the built-in voltage detector. If the set detector threshold voltage is detected, reset signal will be output.

**TECHNICAL NOTES**

When using these ICs, consider the following points:

In these ICs, phase compensation is made for securing stable operation even if the load current is varied. For this purpose, be sure to use as much as  $10\mu\text{F}$  capacitor as CL with good frequency characteristics and ESR (Equivalent Series Resistance).

The best suitable equivalent series resistor value (ESR) is approximately  $1\Omega$ .

If the ESR of the output capacitor is too large, output may be unstable, therefore fully evaluation is necessary.

Make  $V_{DD}$  and GND lines sufficient. When their impedance of these is high, noise pickup or unstable operation may be the result. Connect a capacitor with a capacitance value of as much as  $10\mu\text{F}$  between  $V_{DD}$  and GND as close as possible to these pins.

Set external components, especially output capacitor, as close as possible to the ICs.

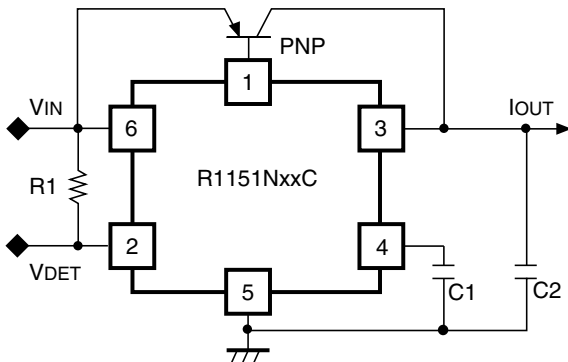
Refer to the next equation to calculate the output delay time of C version and decide the capacitance value for the delay time.

$$t_{PLH} = 1.83 \times C / (300 \times 10^{-9})$$

C: Capacitance value (F)

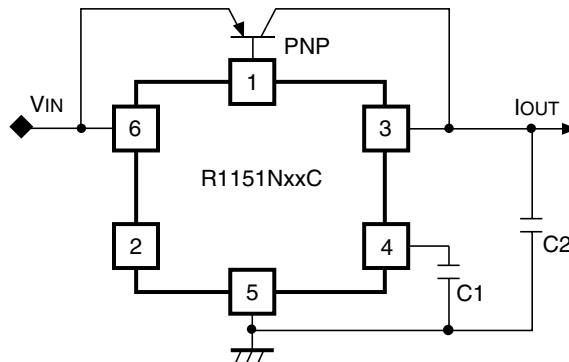
Recommended pull-up resistance ( $R1$ ) value is  $470\text{k}\Omega$ . If the value is too small, released voltage may shift, therefore, use  $10\text{k}\Omega$  or more value resistor.

## TEST CIRCUITS



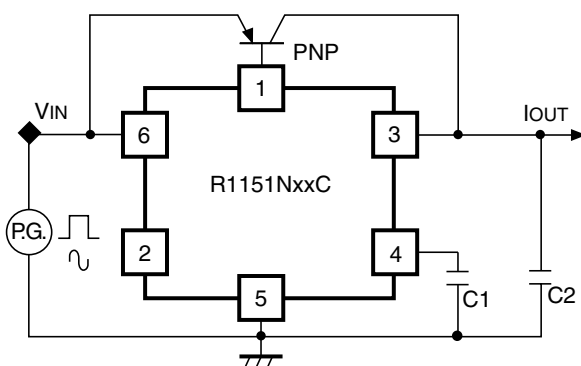
**Fig.1 Standard test Circuit**

**R1=470kΩ C1=220pF, C2=10μF**



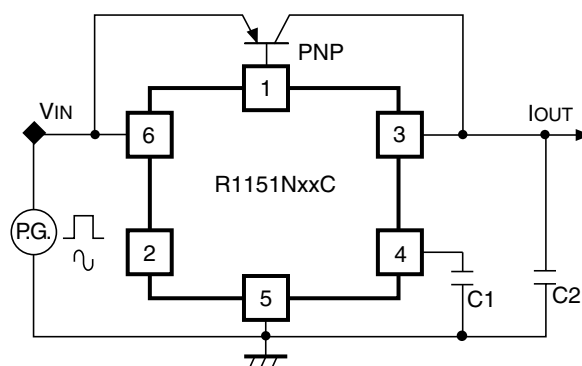
**Fig.2 Supply Current Test Circuit**

**C1=220pF, C2=10μF**



**Fig.3 Ripple Rejection, Line Transient Response Test Circuit**

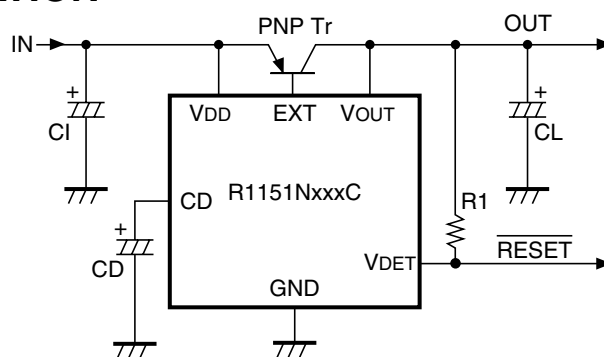
**C1=220pF, C2=10μF**



**Fig.4 Load Transient Response Test Circuit**

**C1=220pF, C2=10μF**

## TYPICAL APPLICATION



(External Components)

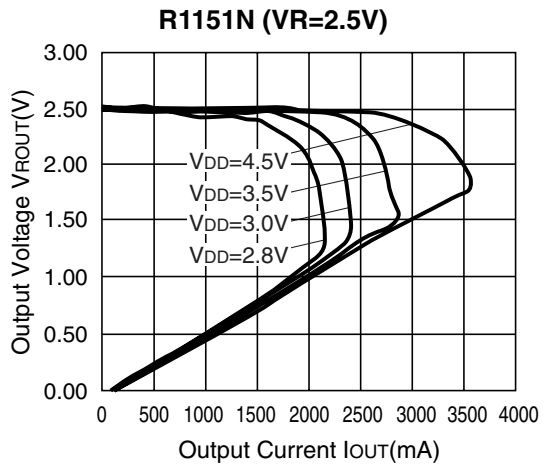
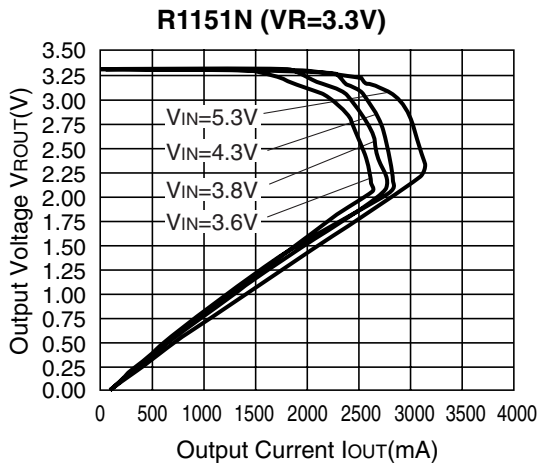
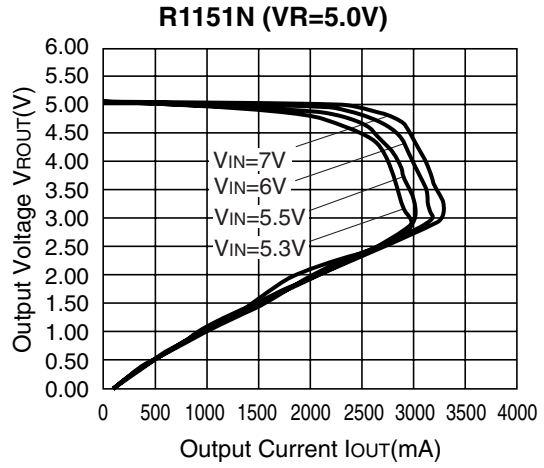
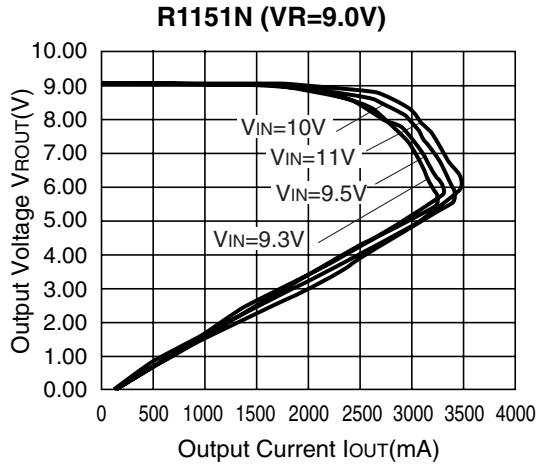
C1 10μF R1=470kΩ PNP Tr.: 2SA1441, 2SB940, 2SB703

CL 10μF

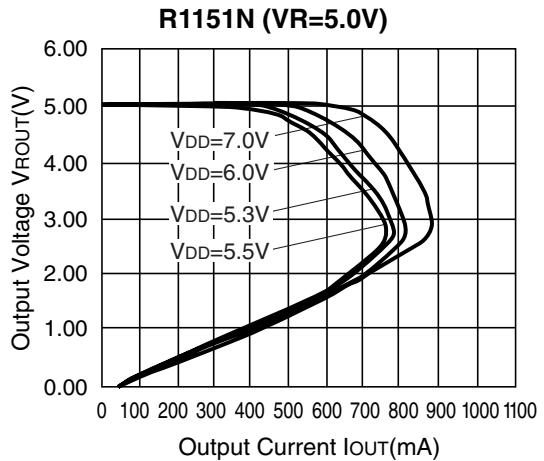
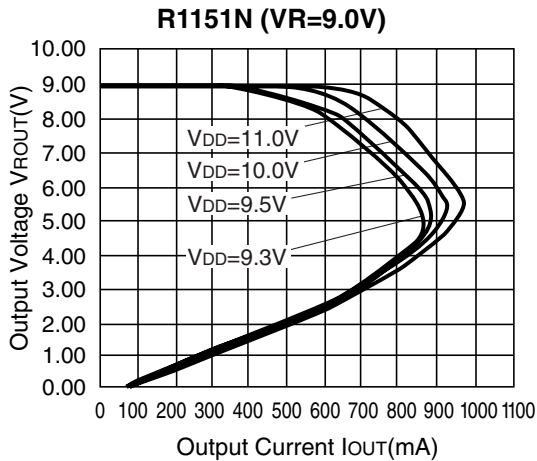
# TYPICAL CHARACTERISTICS

1) Output Voltage vs. Output Current (Topt=25°C)

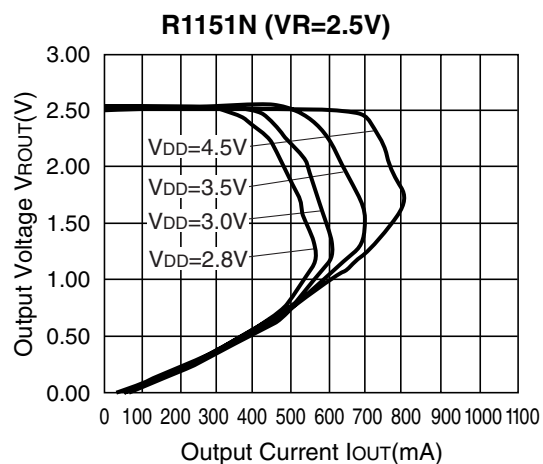
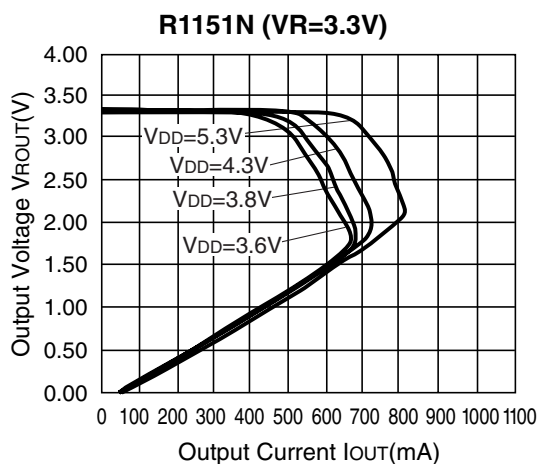
a. External Tr.: 2SA1441



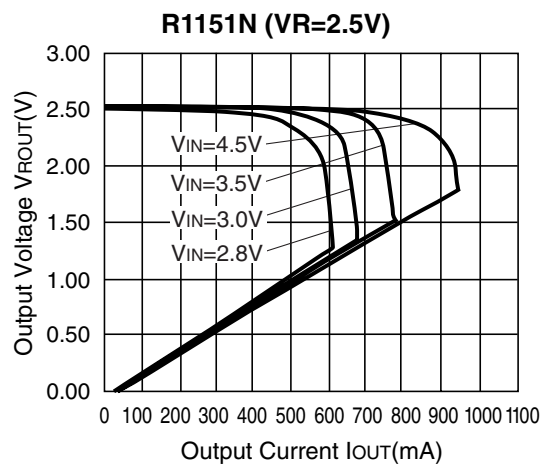
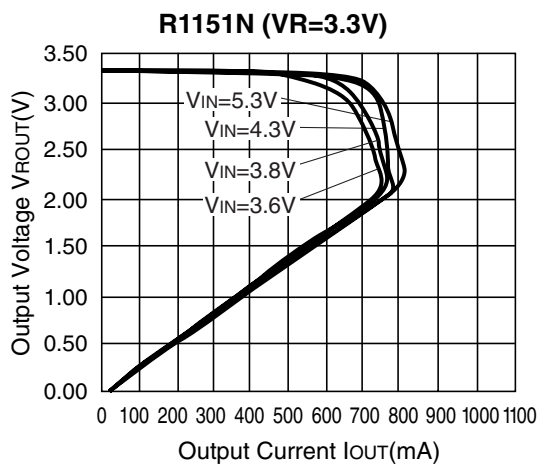
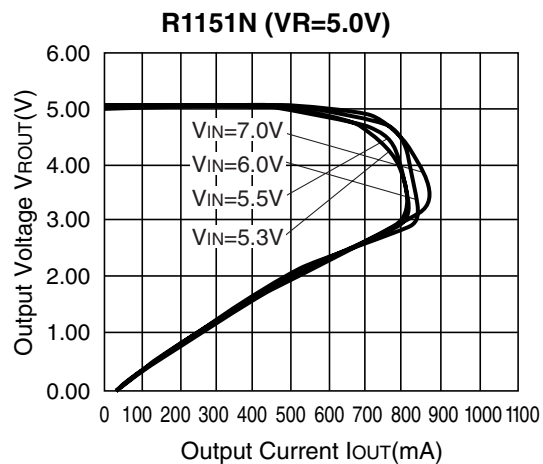
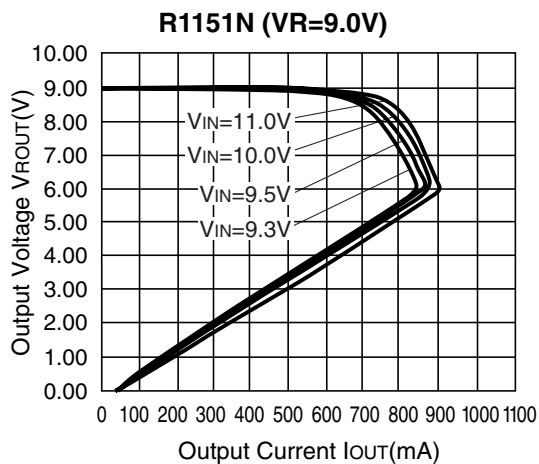
b. External Tr.: 2SB940



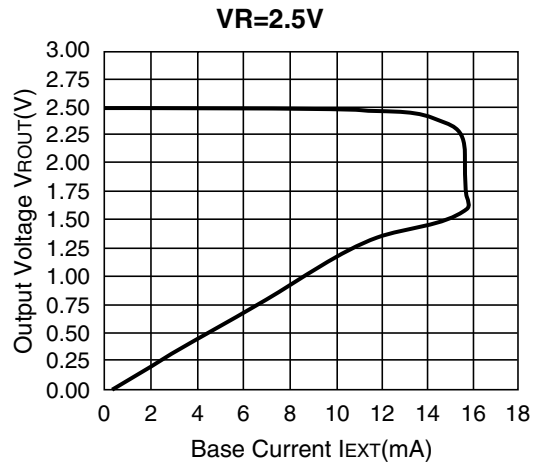
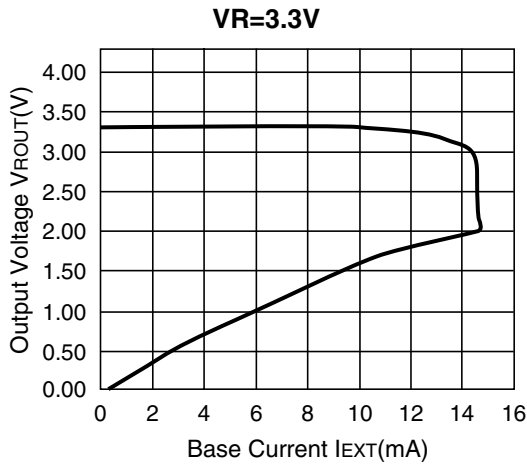
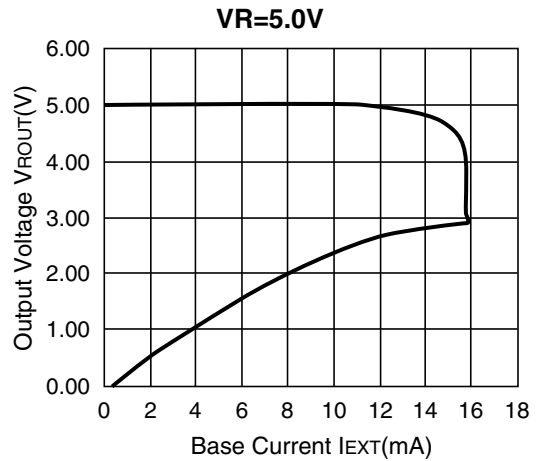
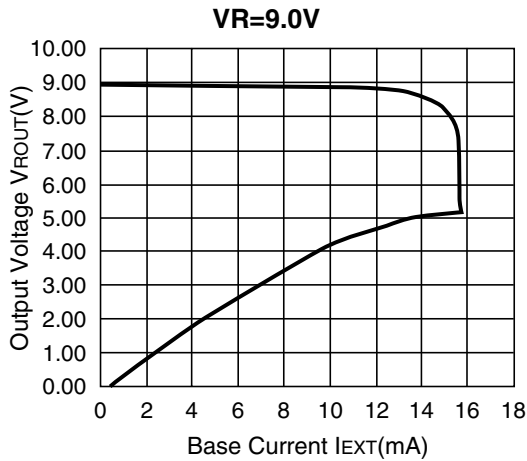




c. External Tr.:2SB703

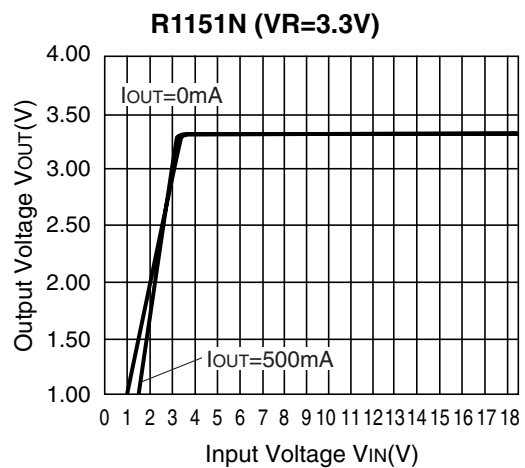
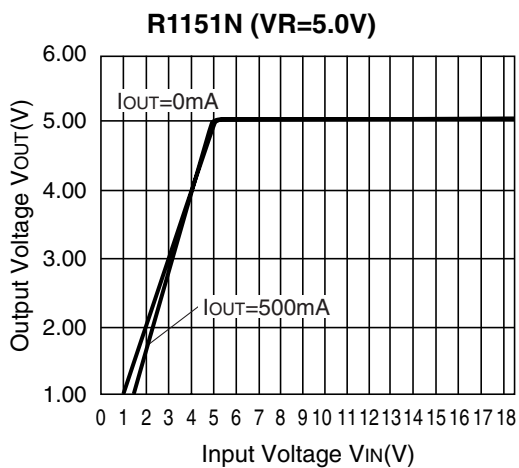


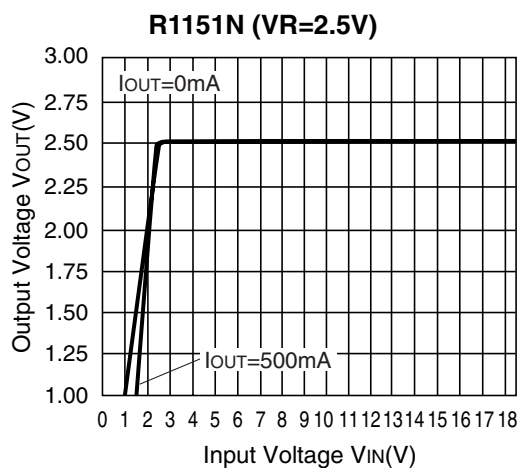
d. Output Voltage vs. Base Current ( $T_{opt}=25^{\circ}C$ )



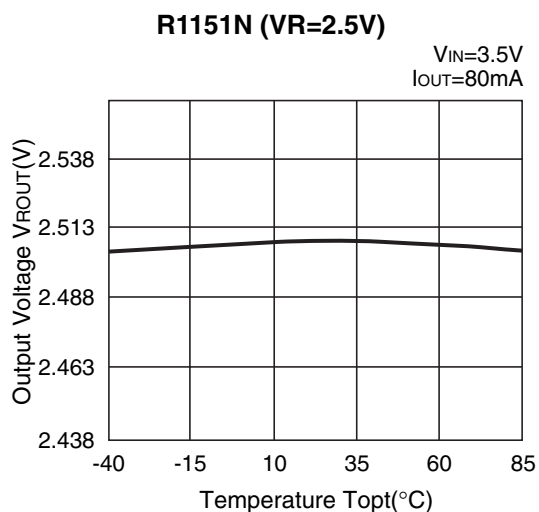
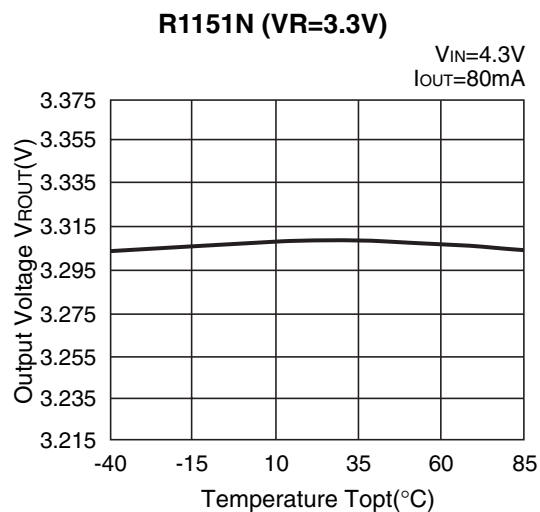
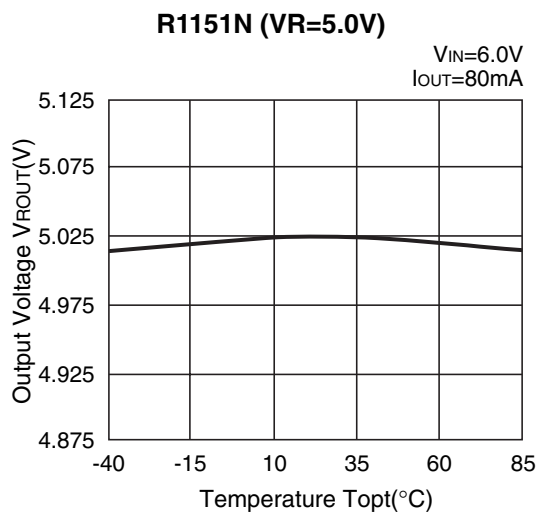
2) Output Voltage vs. Input Voltage ( $T_{opt}=25^{\circ}C$ )

External Transistor: 2SA1441



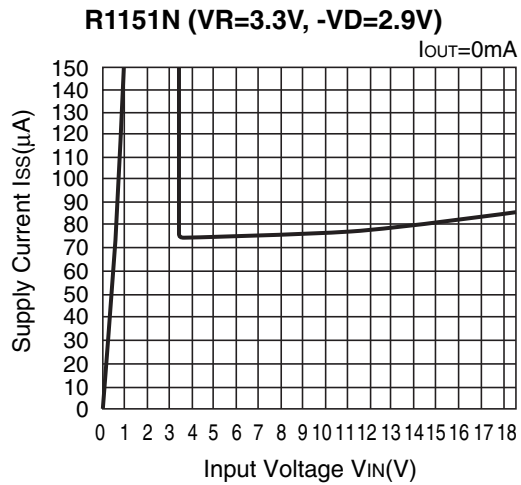
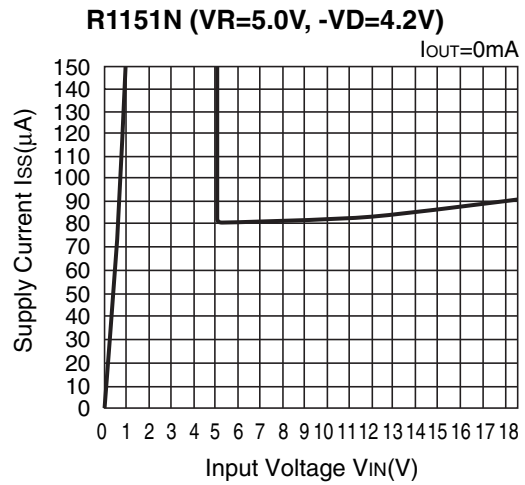
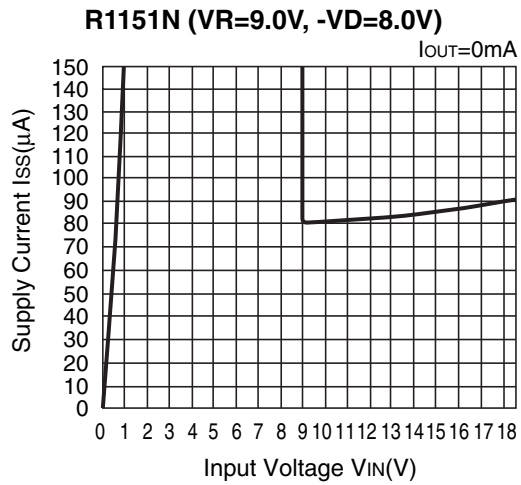


3) Output Voltage vs. Temperature



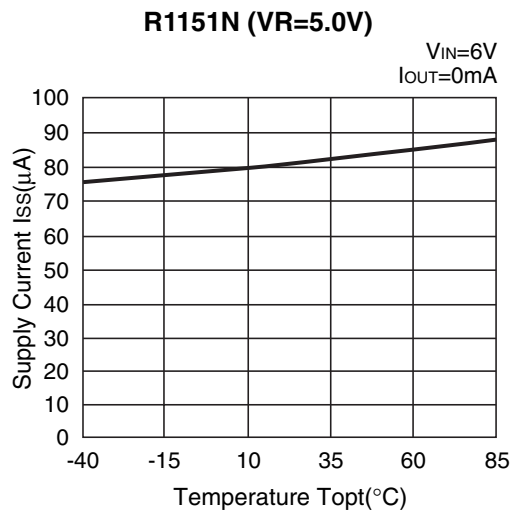
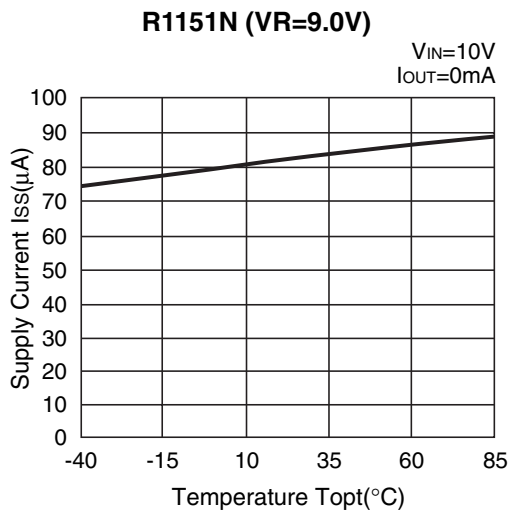
4) Supply Current vs. Input Voltage

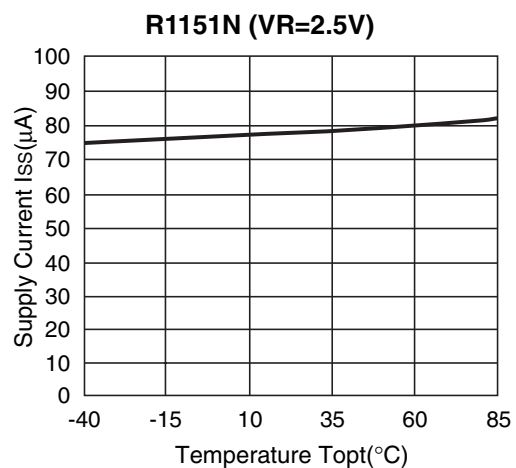
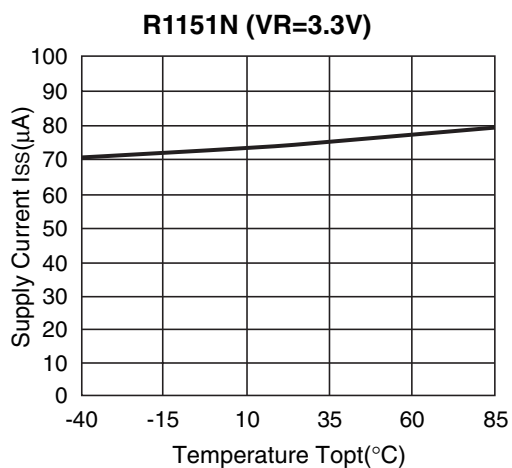
External Tr.:2SA1441



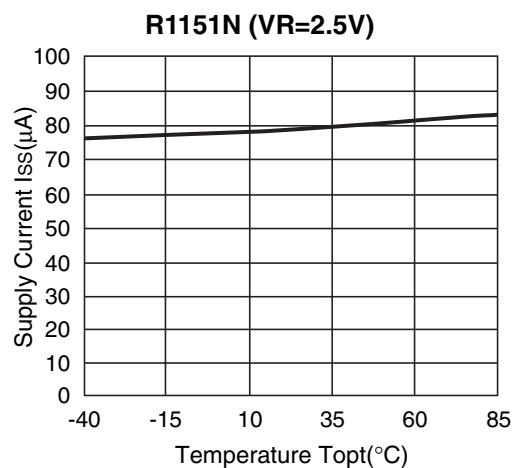
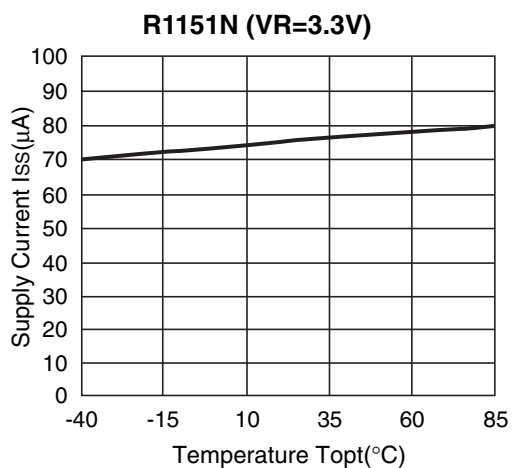
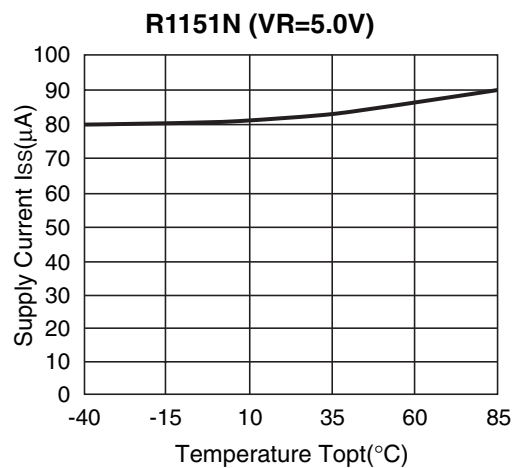
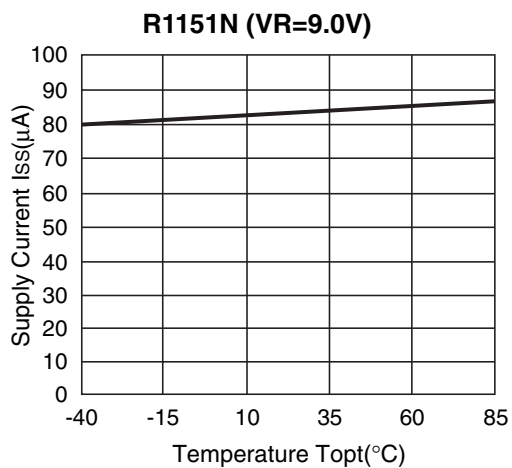
5) Supply Current vs. Temperature

a. External Tr.:2SA1441



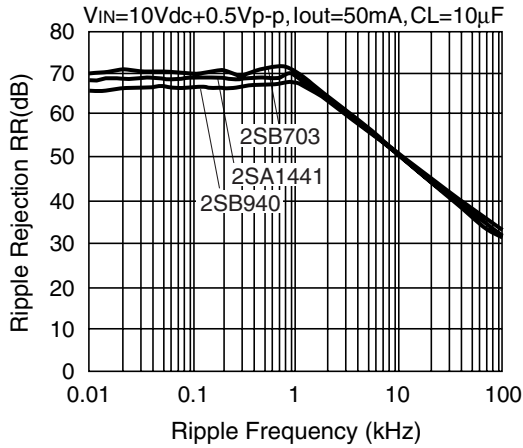


b. External Tr.:2SB703

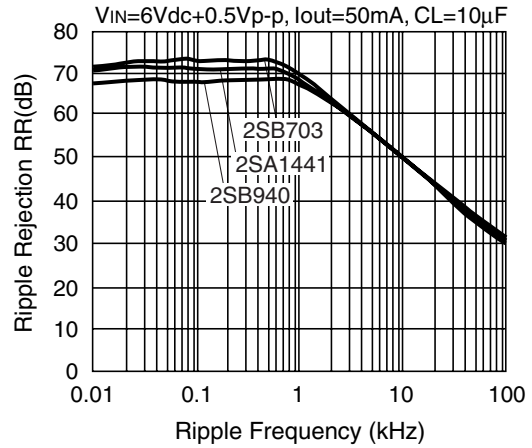


6) Ripple Rejection vs. Ripple Frequency (Topt=25°C)

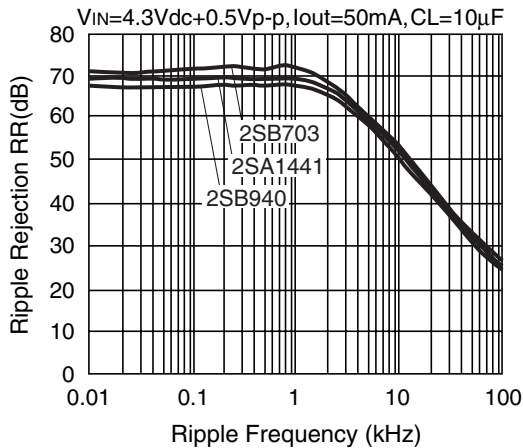
**R1151N (VR=9.0V)**



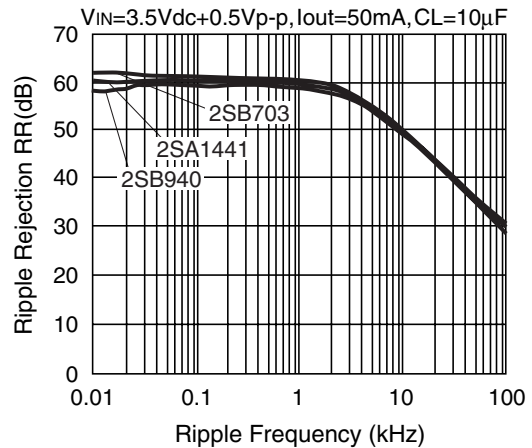
**R1151N (VR=5.0V)**



**R1151N (VR=3.3V)**

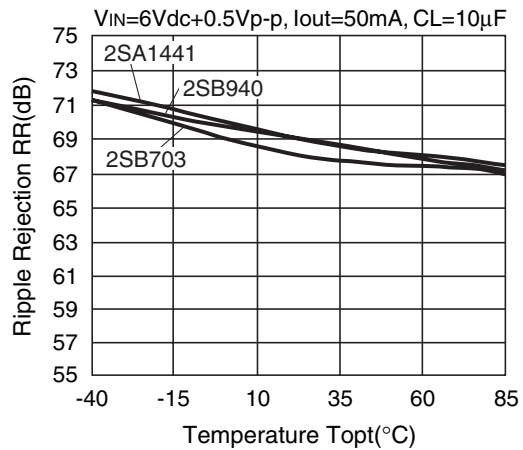


**R1151N (VR=2.5V)**

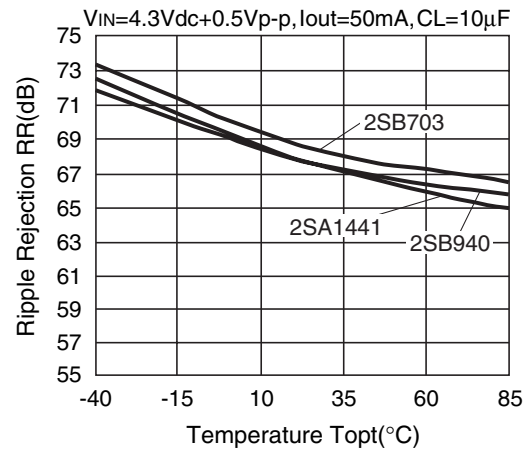


7) Ripple Rejection vs. Temperature

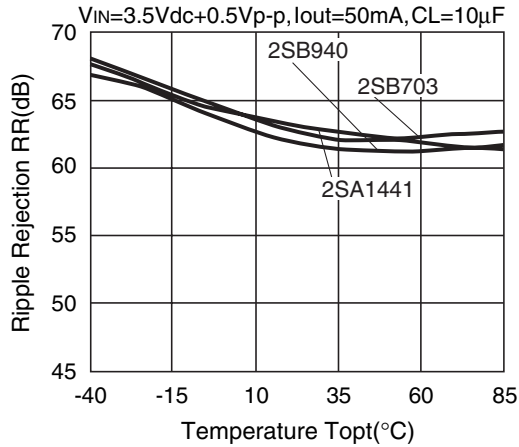
**R1151N (VR=5.0V)**



**R1151N (VR=3.3V)**



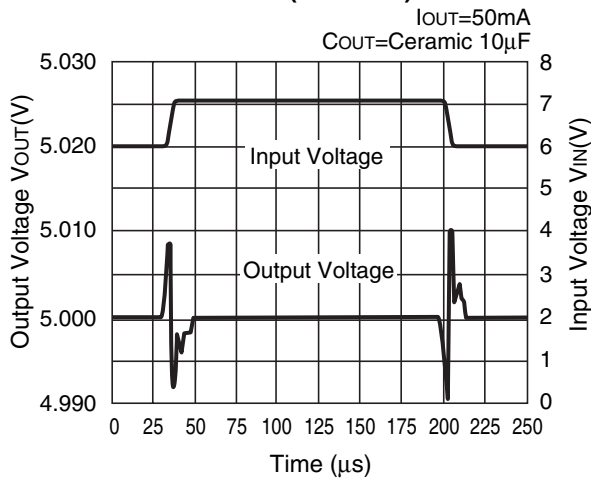
**R1151N (VR=2.5V)**



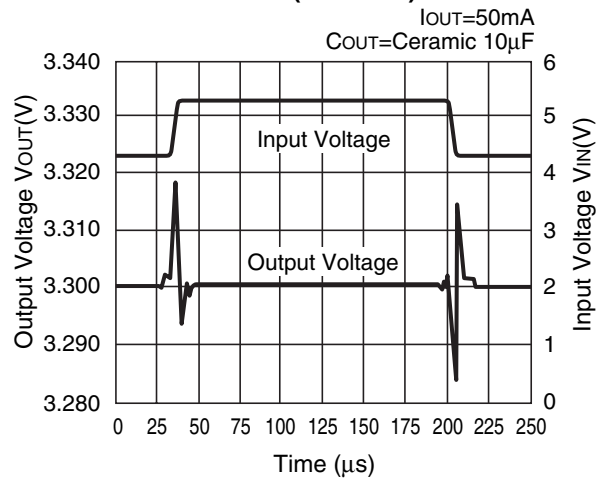
8) Input Transient Response ( $T_{opt}=25^{\circ}C$ )

a. External Tr.:2SA1441

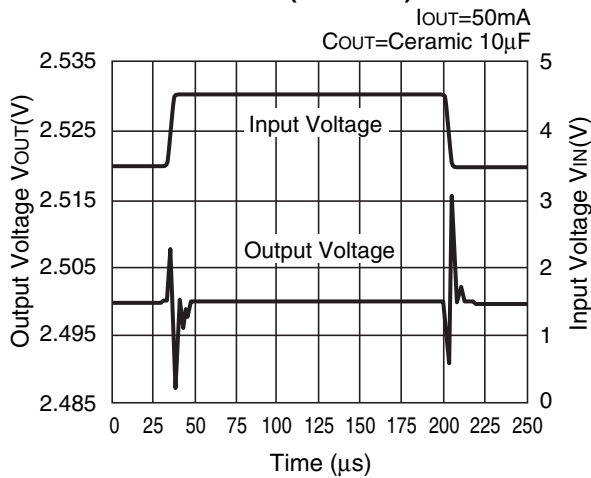
**R1151N (VR=5.0V)**



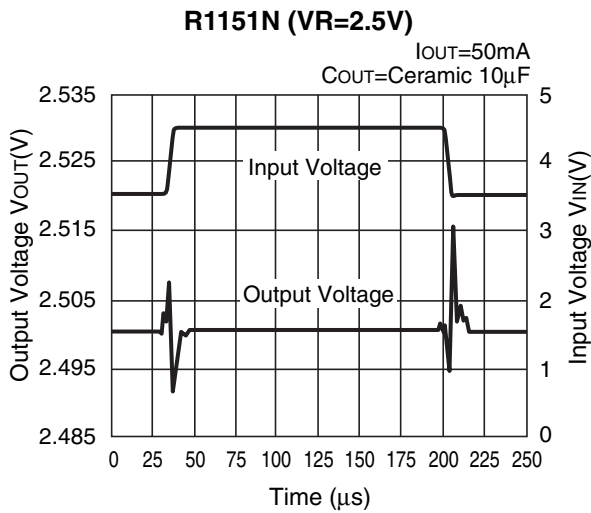
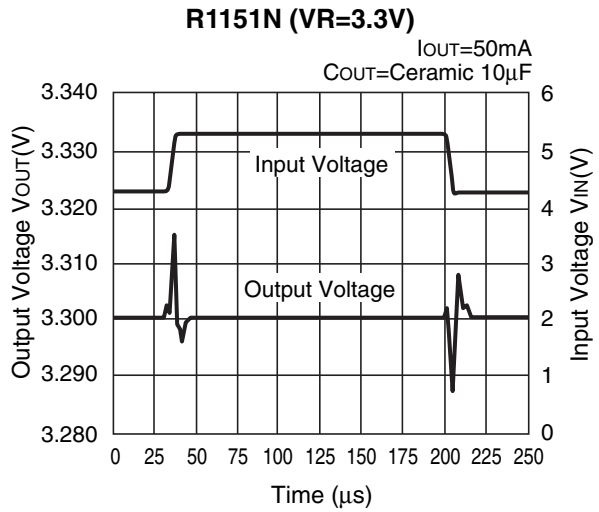
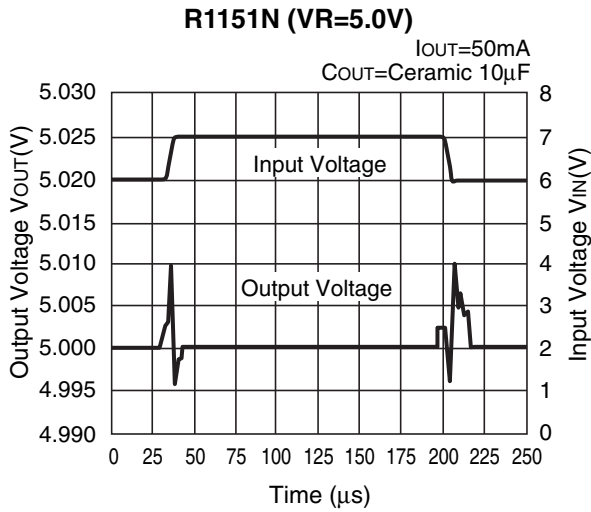
**R1151N (VR=3.3V)**



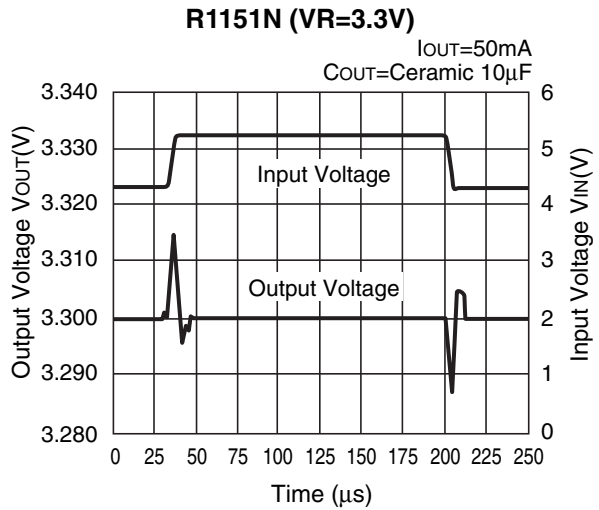
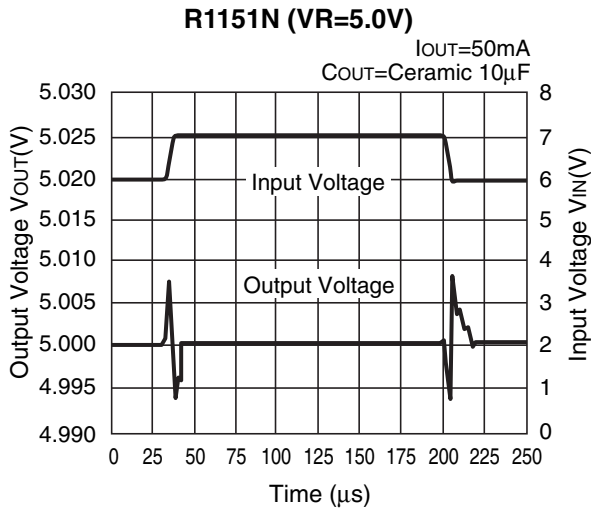
**R1151N (VR=2.5V)**



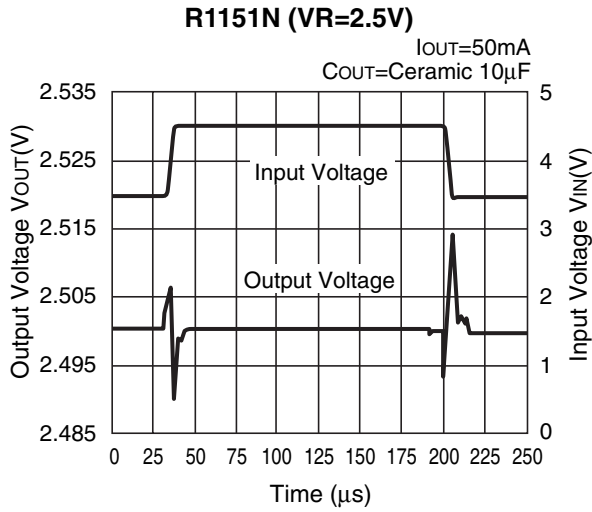
b. External Tr.: 2SB703



c. External Tr. : 2SB940

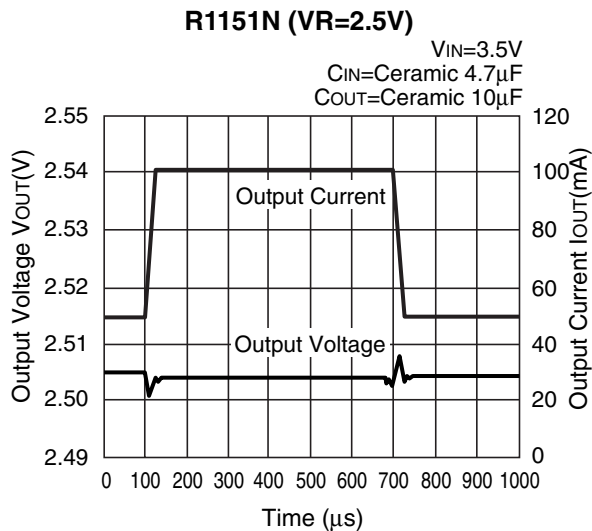
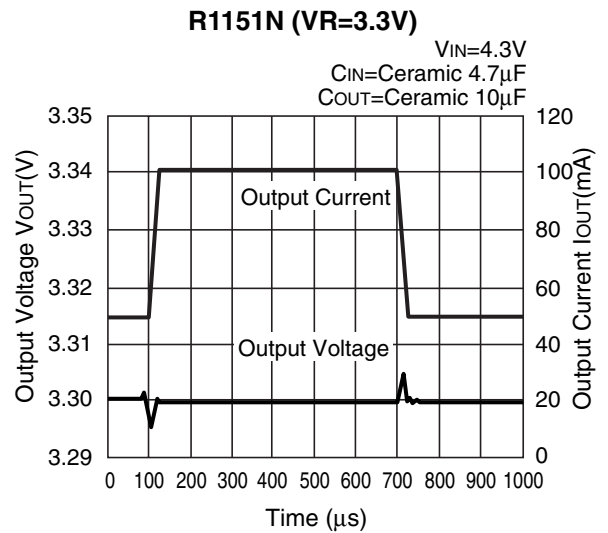
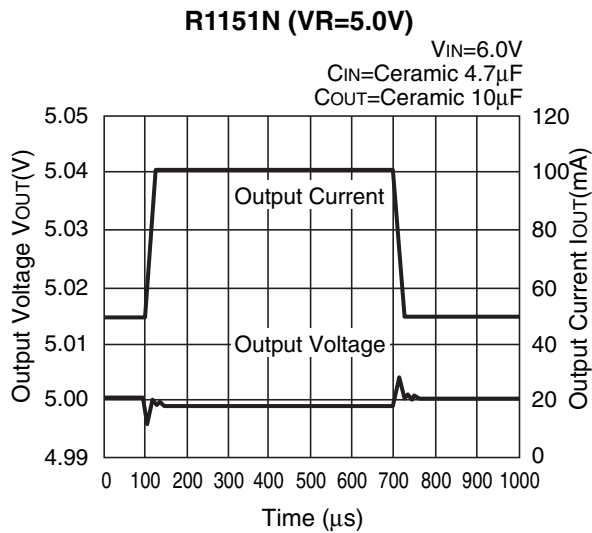






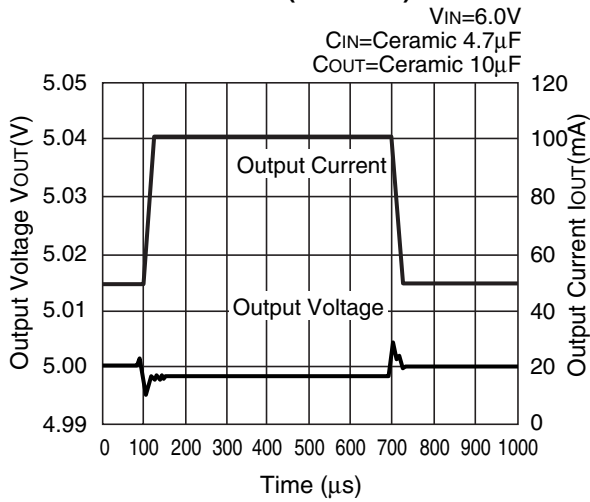
9) Load Transient Response ( $T_{opt}=25^{\circ}C$ )

a: External Tr.: 2SA1441

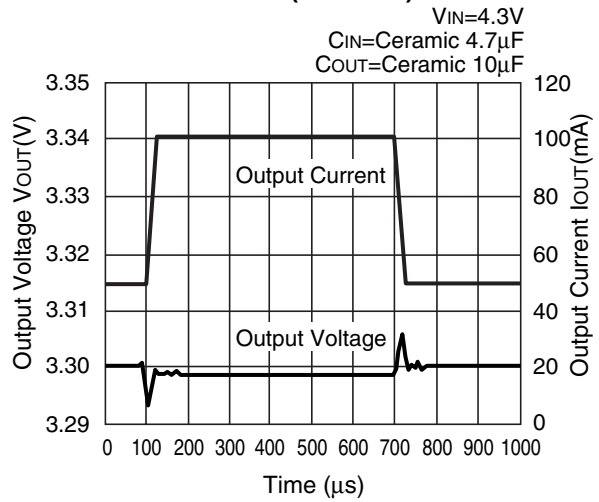


b. External Tr.: 2SB703

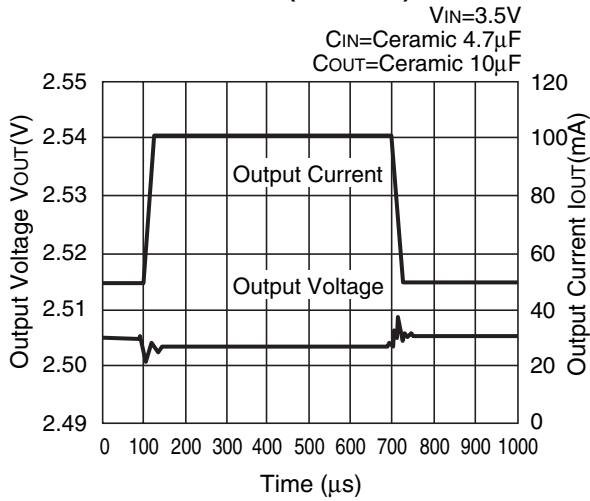
**R1151N (VR=5.0V)**



**R1151N (VR=3.3V)**

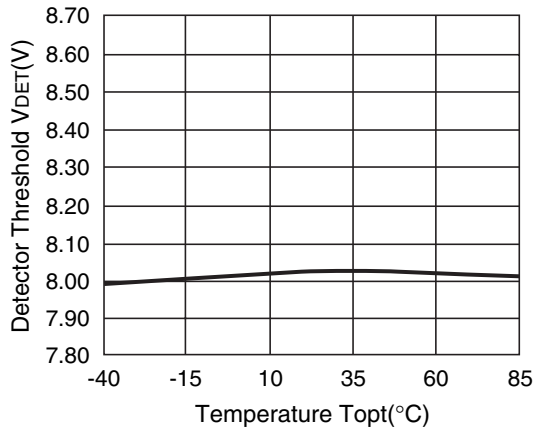


**R1151N (VR=2.5V)**

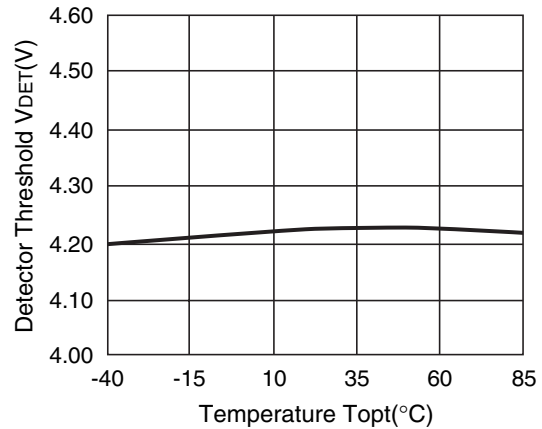


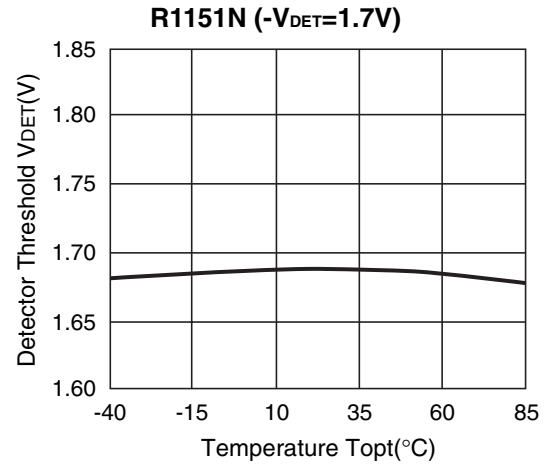
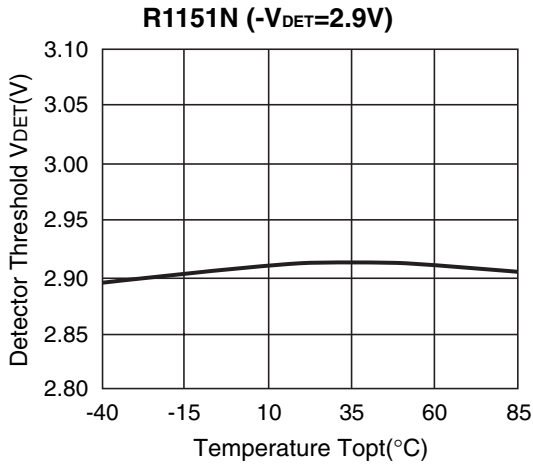
10) Detector Threshold vs. Temperature

**R1151N (-V<sub>DET</sub>=8.0V)**

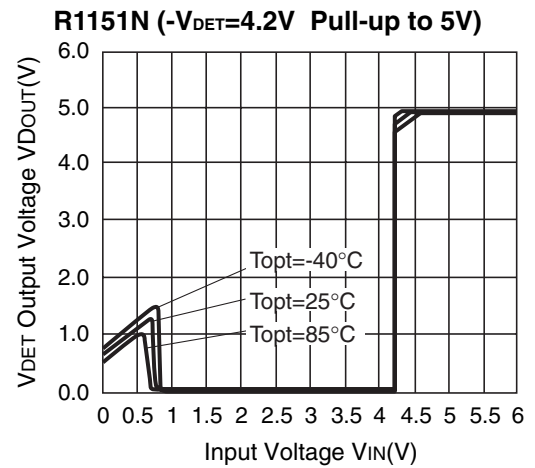
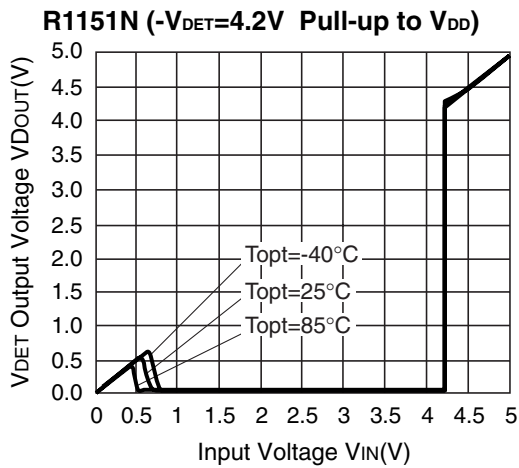
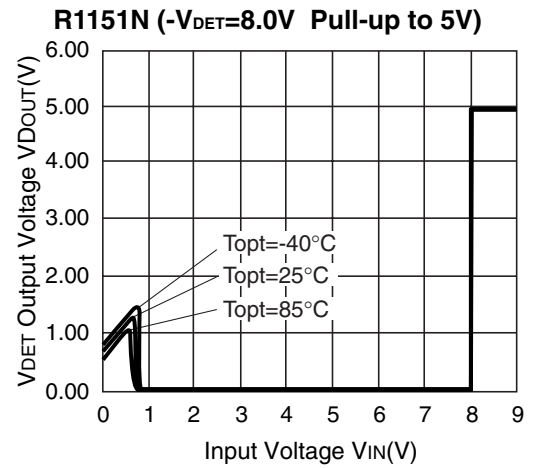
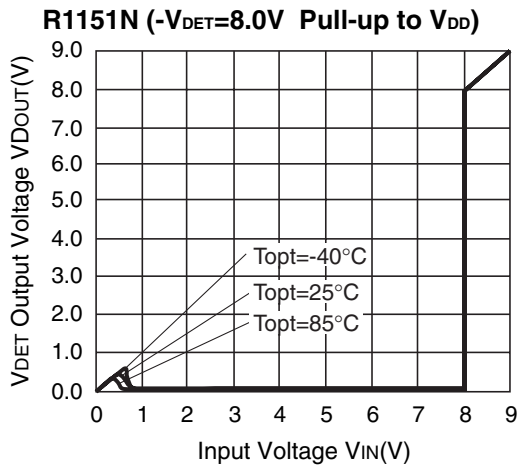


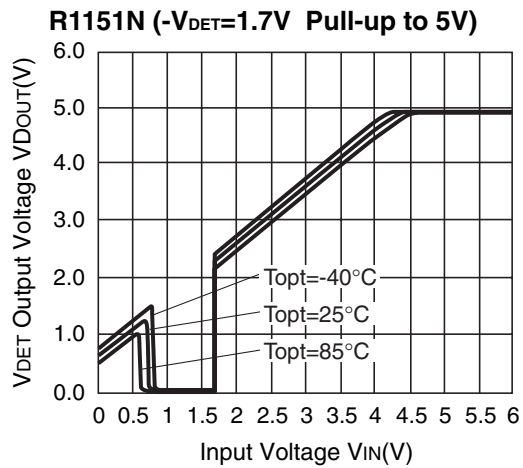
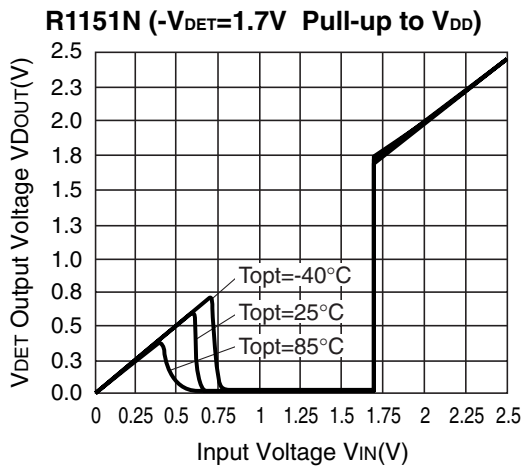
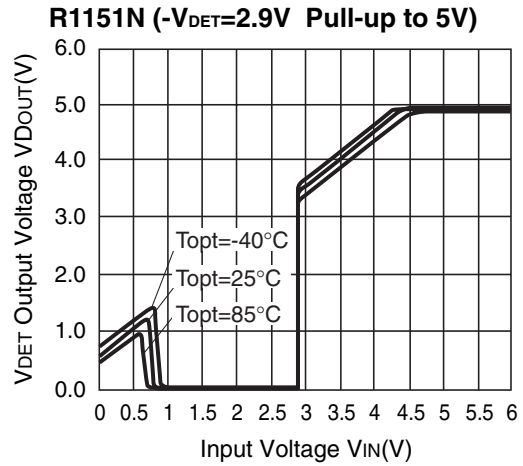
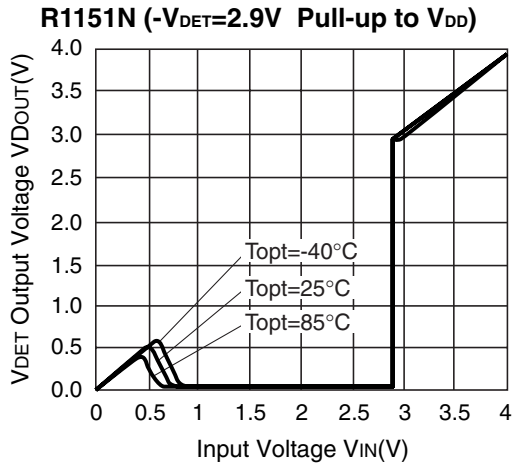
**R1151N (-V<sub>DET</sub>=4.2V)**



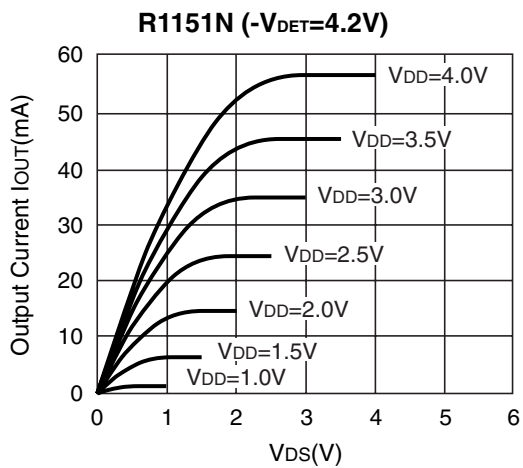
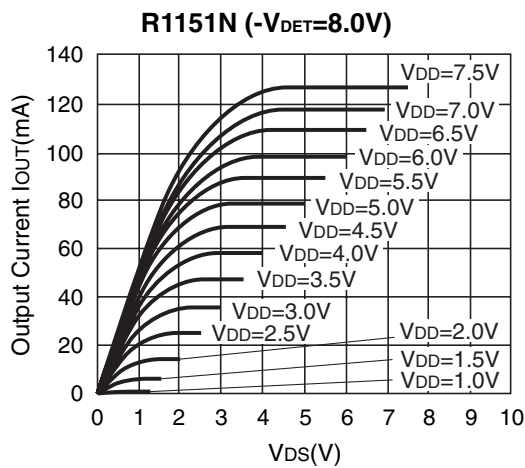


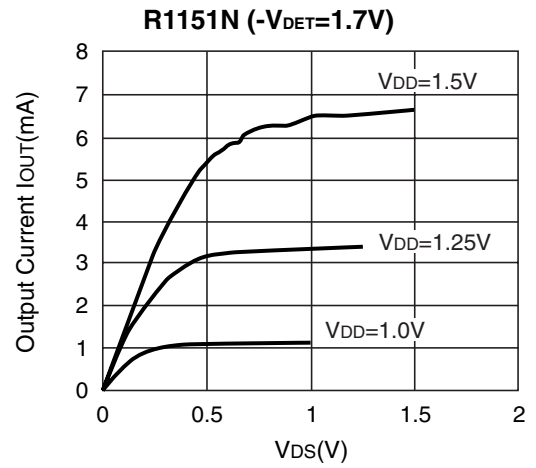
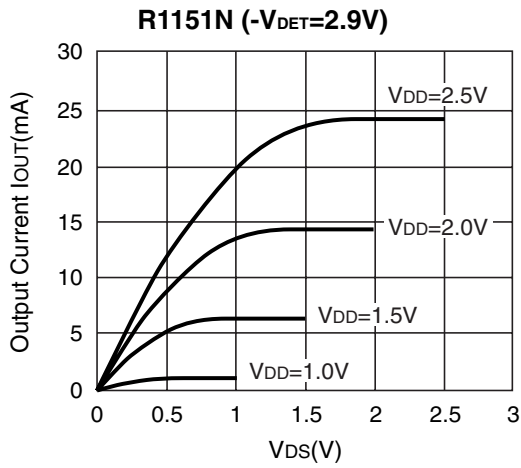
11) V<sub>DET</sub> Output Voltage vs. Input Voltage



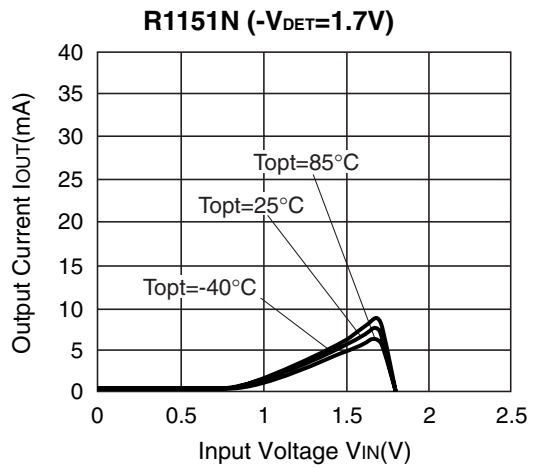
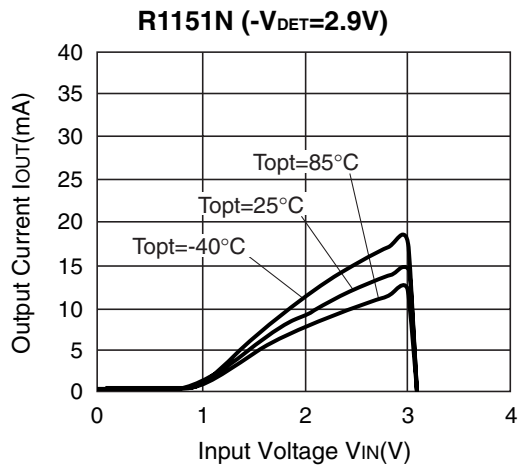
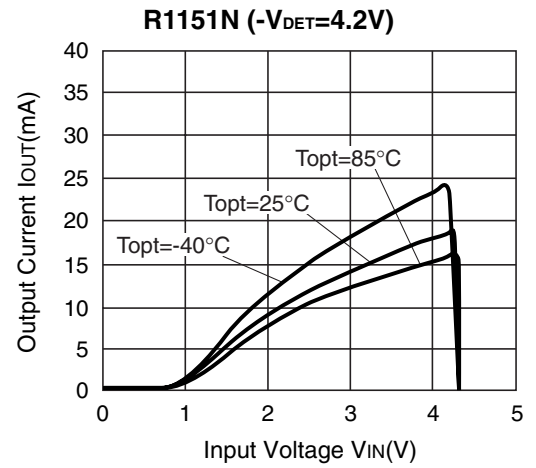
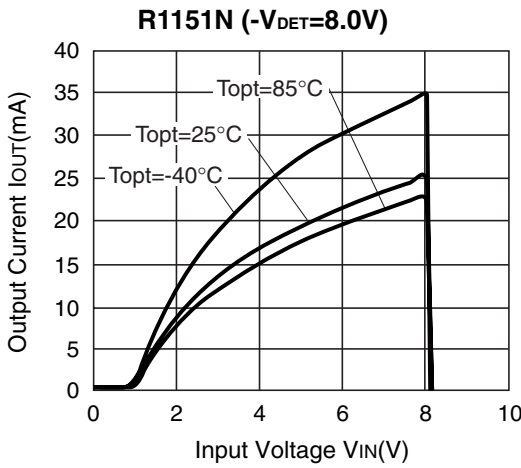


12) Nch Driver Output Current vs. V<sub>DS</sub> (T<sub>opt</sub>=25°C)

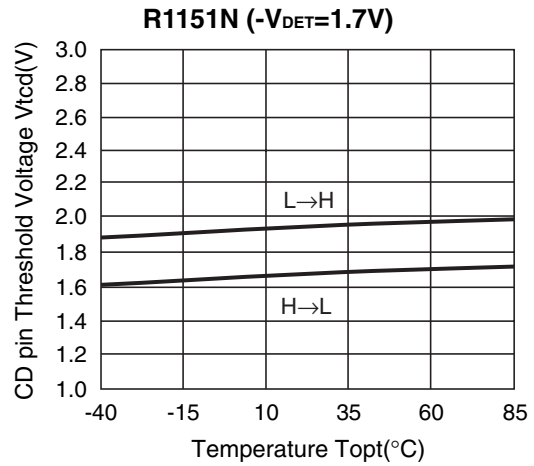
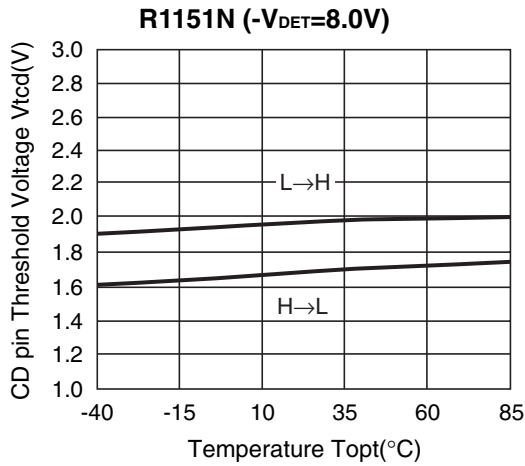




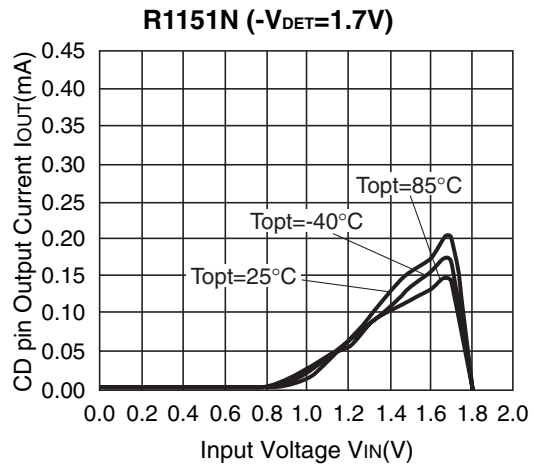
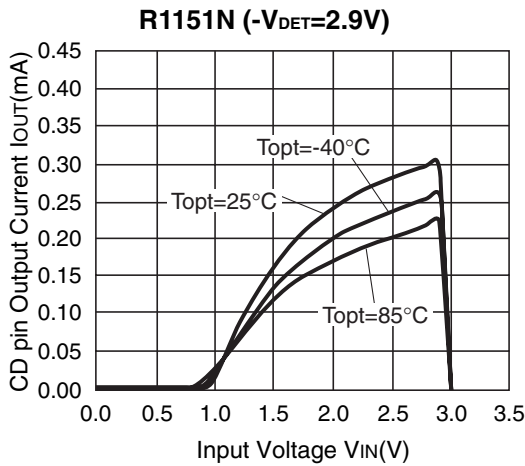
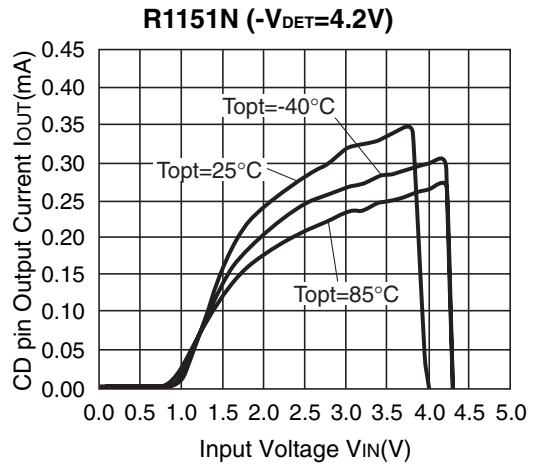
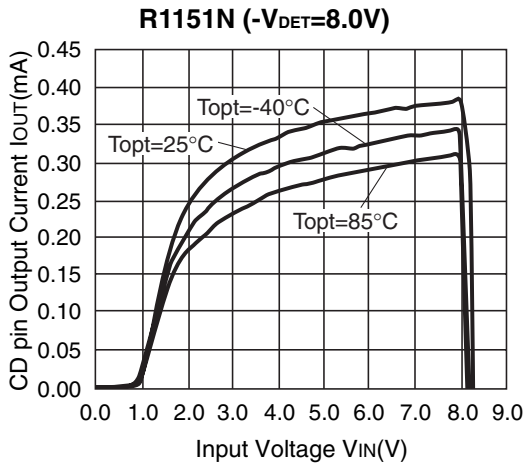
13) Nch Driver Output Current vs. Input Voltage



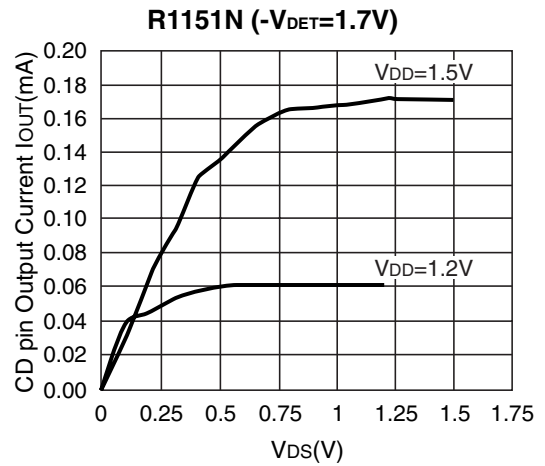
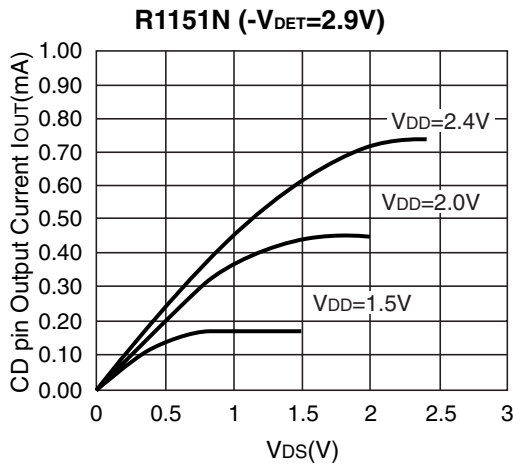
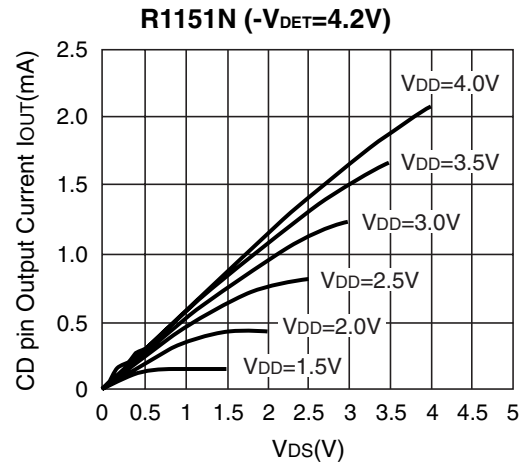
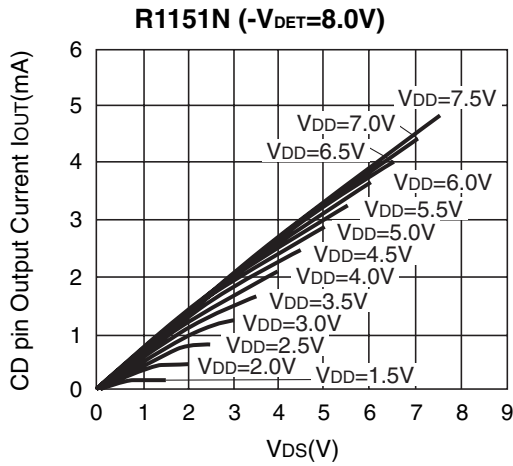
14) CD pin Threshold Voltage vs. Temperature



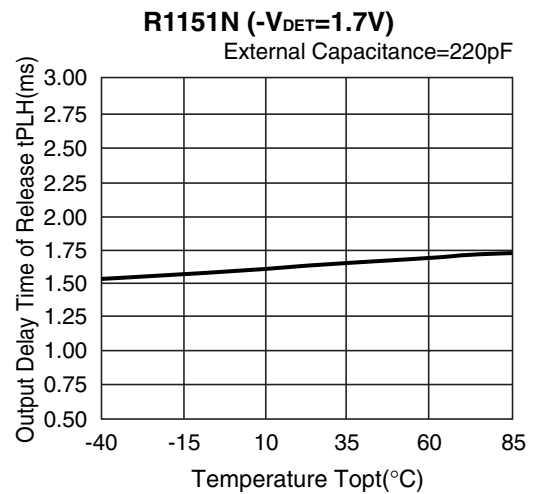
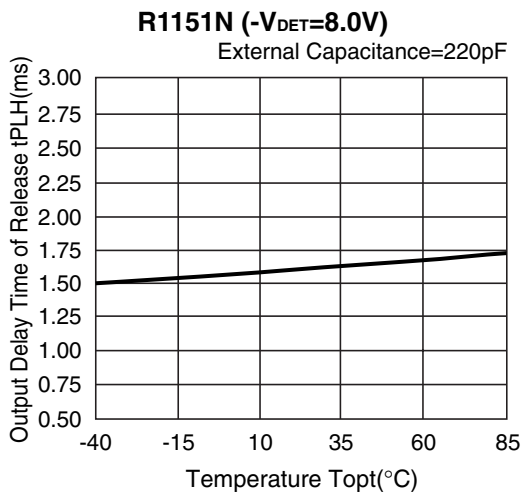
15) CD Pin Output Current vs. Input Voltage



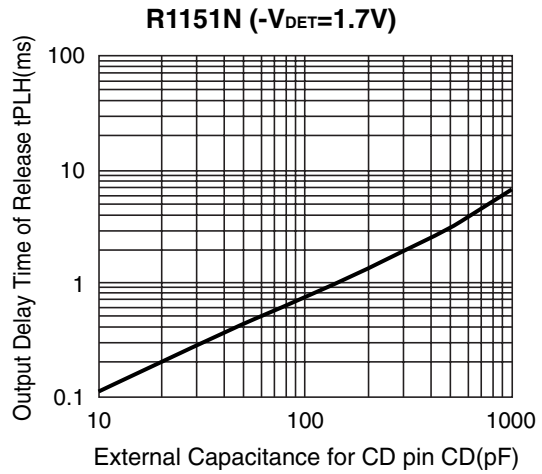
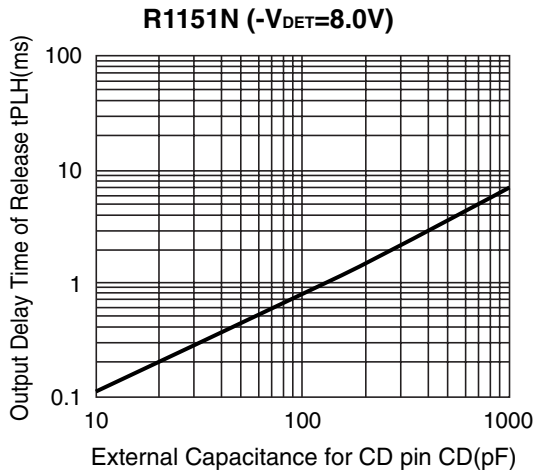
16) CD Pin Output Current vs.  $V_{DS}$  ( $T_{opt}=25^{\circ}C$ )



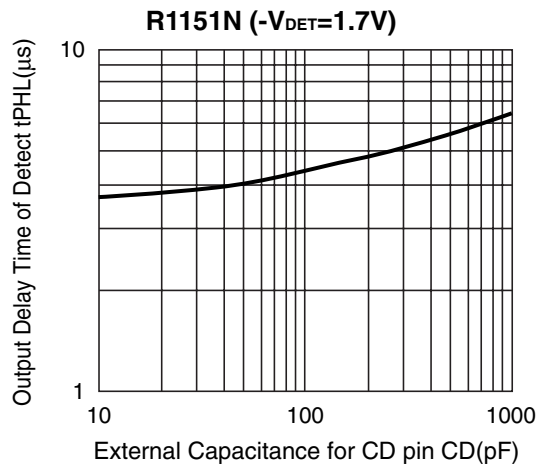
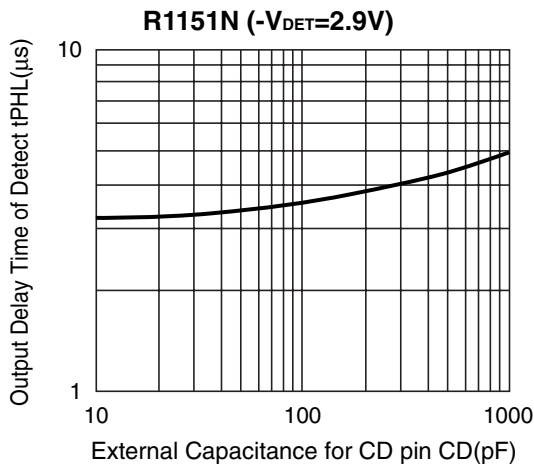
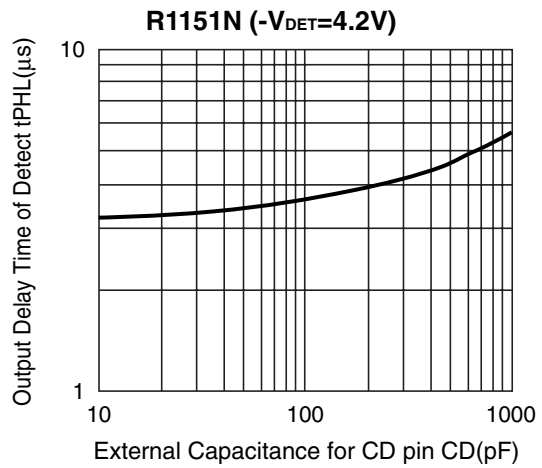
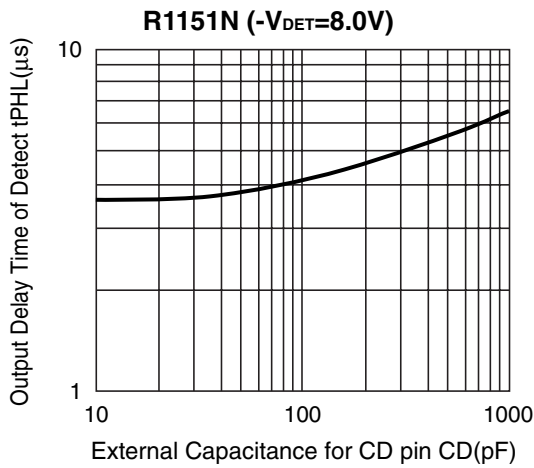
17) Output Delay Time of Release vs. Temperature



18) Output Delay Time of Release vs. External Capacitance for CD pin (T<sub>opt</sub>=25°C)



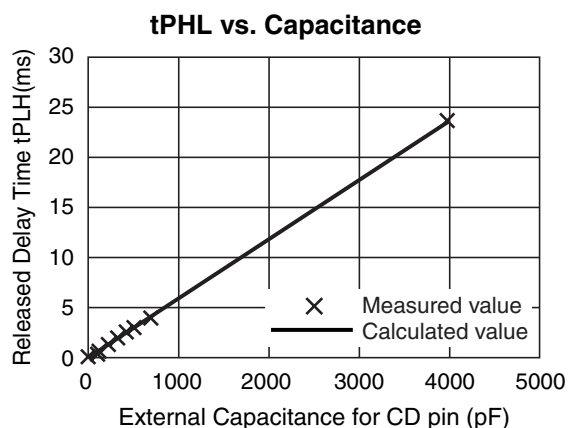
19) Output Delay Time of Detect vs. External Capacitance for CD pin (T<sub>opt</sub>=25°C)





## Calculation of Output Delay Time of Release

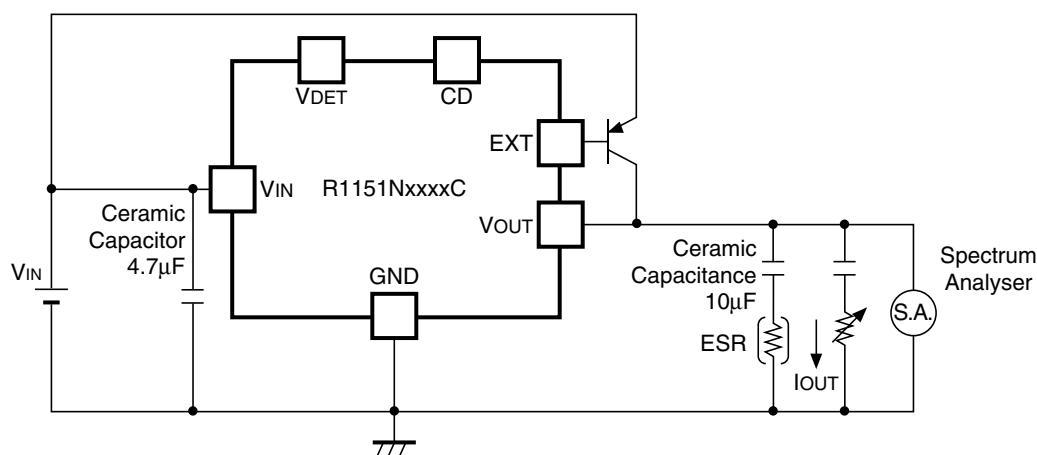
$$t_{PLH}(s) = 1.83 \times C / (300 \times 10^{-9})$$



## For Stable Operation

### Phase Compensation

In these ICs, phase compensation is externally made for securing stable operation even if the load current is varied. For this purpose, be sure to use a capacitor for the output pin with good frequency characteristics and ESR (Equivalent Series Resistance) of which is in the range described as follows:



**Measuring Circuit for white noise; R1151NxxxxC**

The relations between  $I_{OUT}$  (Output Current) and ESR of Output Capacitor are shown below. The conditions when the white noise level is under  $40\mu V$  (Avg.) are marked as the hatched area in the graph.

<Measurement conditions>

- (1)  $V_{IN} = V_{OUT} + 1V$
- (2) Frequency band: 10Hz to 1MHz
- (3) Temperature: 25°C
- (4)  $C_{OUT}$ : Ceramic 10 $\mu F$ ; ESR=0.075 $\Omega$  (10kHz)

