DRAM

2 MEG x 8 DRAM

5.0V, EDO PAGE MODE, OPTIONAL SELF REFRESH

FEATURES

* Industry-standard x8 pinout, timing, functions and packages
* High-performance CMOS silicon-gate process
* Single +5.0V ±10% power supply
* Low power, 1mW standby; 270mW active, typical
* All inputs, outputs and clocks are TTL-compatible
* Refresh modes: RAS#-ONLY, CAS#-BEFORE-RAS# (CBR), HIDDEN and Self Refresh
* 2,048-cycle refresh (11 row-, 10 column addresses)
* Extended Data-Out (EDO) PAGE access cycle

OPTIONS — MARKING

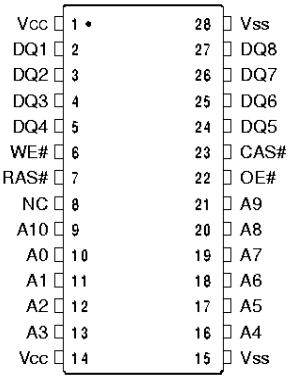
* Timing
  - 50ns access — -5
  - 60ns access — -6
  - 70ns access — -7
* Packages
  - Plastic SOJ (300 mil) — DJ
  - Plastic SOJ (400 mil) — DW
  - Plastic TSOP (300 mil) — TG
* Refresh Rate
  - Standard Refresh (32ms period) — None
  - Self Refresh (128ms period) — S
* Part Number Example: MT4C2M8E7DJ-6

KEY TIMING PARAMETERS

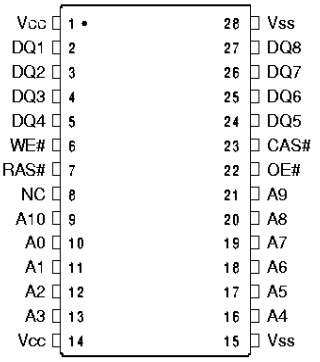
SPEED	t_{RC}	t_{RAC}	t_{PC}	t_{AA}	t_{CAC}	t_{CAS}
-5	90ns	50ns	25ns	25ns	15ns	10ns
-6	105ns	60ns	25ns	30ns	15ns	12ns
-7	125ns	70ns	30ns	35ns	20ns	12ns

PIN ASSIGNMENT (Top View)

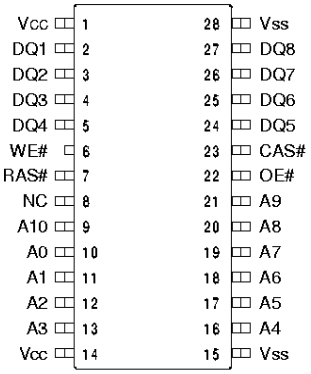
28-Pin SOJ (DA-3)



28-Pin SOJ (DA-4)



28-Pin TSOP (DB-3)



GENERAL DESCRIPTION

The MT4C2M8E7(S) is a randomly accessed solid-state memory containing 16,777,216 bits organized in a x8 configuration. The MT4C2M8E7(S) RAS# is used to latch the first 11 bits and CAS# the latter 10 bits (A10 is ignored during CAS# falling edge.) READ and WRITE cycles are selected with the WE# input. A logic HIGH on WE# dictates READ mode while a logic LOW on WE# dictates WRITE mode. During a WRITE cycle, data-in (D) is latched by the falling edge of WE# or CAS#, whichever occurs last. An EARLY WRITE occurs when WE# is taken LOW prior to CAS# falling. A LATE WRITE or READ-MODIFY-WRITE occurs when WE# falls after CAS# was taken LOW. During EARLY WRITE cycles, the data-outputs (Q) will remain High-Z regardless of the state of OE#. During LATE WRITE or READ-MODIFY-WRITE cycles, OE# must be taken HIGH to disable the data-outputs prior to applying input data. If a LATE WRITE or READ-MODIFY-WRITE is attempted while keeping OE# LOW, no write will occur, and the data-outputs will drive read data from the accessed location.

The eight data inputs and the eight data outputs are routed through eight pins using common I/O, and pin direction is controlled by WE# and OE#.

PAGE ACCESS

PAGE operations allow faster data operations (READ, WRITE or READ-MODIFY-WRITE) within a row-address-defined page boundary. The PAGE cycle is always initiated with a row-address strobed-in by RAS# followed by a column-address strobed-in by CAS#. CAS# may be toggled-in by holding RAS# LOW and strobing-in different column-addresses, thus executing faster memory cycles. Returning RAS# HIGH terminates the PAGE MODE of operation.

EDO PAGE MODE

The MT4C2M8E7(S) provides EDO PAGE MODE, which is an accelerated FAST PAGE MODE cycle. The primary advantage of EDO is the availability of data-out even after CAS# returns HIGH. EDO provides for CAS# precharge time (^{t}CP) to occur without the output data going invalid. This elimination of CAS# output control provides for pipeline READs.

FAST-PAGE-MODE DRAMs have traditionally turned the output buffers off (High-Z) with the rising edge of CAS#. EDO-PAGE-MODE DRAMs operate similar to FAST-PAGE-MODE DRAMs, except data will remain valid or become valid after CAS# goes HIGH during READs, provided RAS# and OE# are held LOW. If OE# is pulsed while RAS# and CAS# are LOW, data will toggle from valid data to High-Z and back to the same valid data. If OE# is toggled or pulsed after CAS# goes HIGH while RAS# remains LOW, data will transition to and remain High-Z (refer to Figure 1).

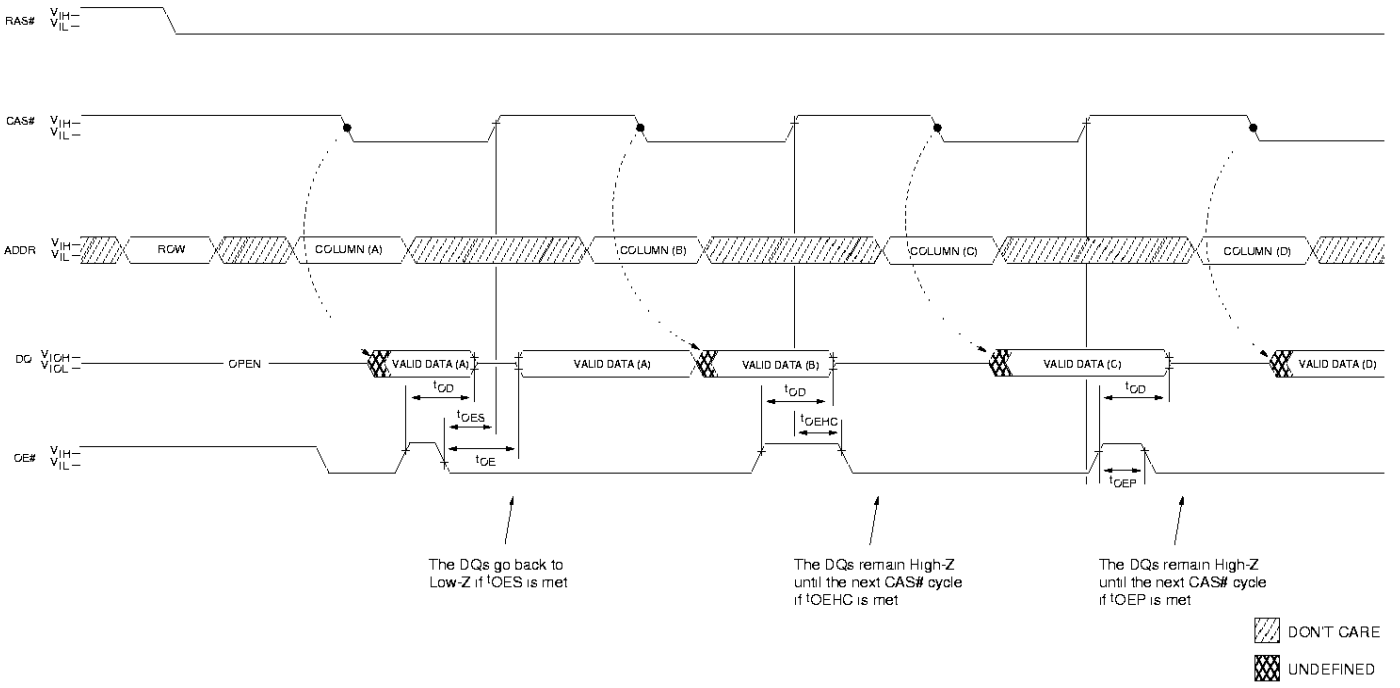


Figure 1
OE# CONTROL OF DQs

During an application, if the DQ outputs are wire OR'd, OE# must be used to disable idle banks of DRAMs. Alternatively, pulsing WE# to the idle banks during CAS# HIGH time will also High-Z the outputs. Independent of OE# control, the outputs will disable after ^{t}OFF, which is referenced from the rising edge of RAS# or CAS#, whichever occurs last (refer to Figure 2).

REFRESH

Preserve correct memory cell data by maintaining power and executing any RAS# cycle (READ, WRITE) or RAS# refresh cycle (RAS#-ONLY, CBR, or HIDDEN) so that all 2,048 combinations of RAS# addresses are executed within ^{t}REF max, regardless of sequence. The CBR and SELF REFRESH cycles will invoke the internal refresh counter for automatic RAS# addressing.

An optional SELF REFRESH mode is also available on the MT4C2M8E7 S. The "S" option allows the user the choice of a fully static low-power data retention mode, or a dynamic refresh mode at the extended refresh period of 128ms. The optional SELF REFRESH feature is initiated by performing a CBR REFRESH cycle, and holding RAS# LOW for the specified ^{t}RASS. Additionally, the "S" option allows for an extended refresh period of 128ms, or 62.5µs per row if using distributed CBR REFRESH. This refresh rate can be applied during normal operation, as well as during a standby or BATTERY BACKUP mode.

The SELF REFRESH mode is terminated by driving RAS# HIGH for a minimum time of ^{t}RPS. This delay allows for the completion of any internal refresh cycles that may be in process at the time of the RAS# LOW-to-HIGH transition. If the DRAM controller uses a distributed refresh sequence, a burst refresh is not required upon exiting SELF REFRESH. However, if the DRAM controller utilizes RAS#-ONLY or burst refresh sequence, all 2,048 rows must be refreshed within the average internal refresh rate, prior to the resumption of normal operation.

STANDBY

Returning RAS# and CAS# HIGH terminates a memory cycle and decreases chip current to a reduced standby level. The chip is preconditioned for the next cycle during the RAS# HIGH time.

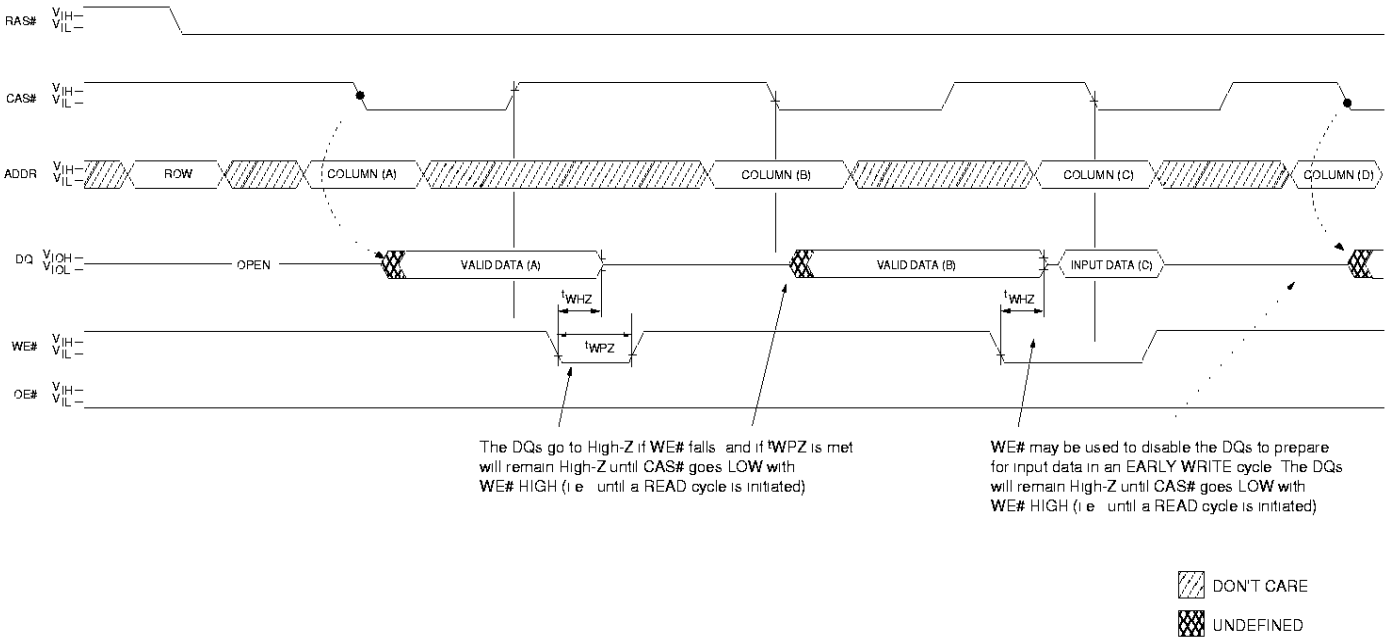
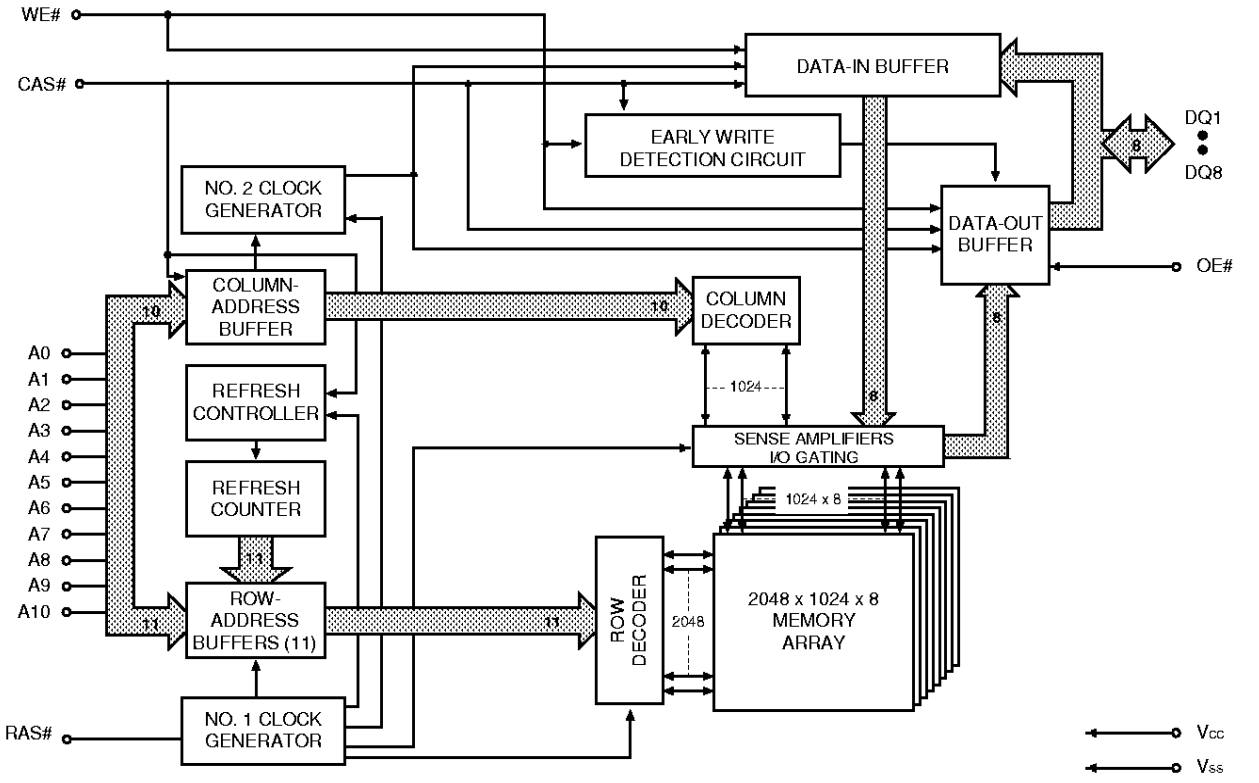


Figure 2
WE# CONTROL OF DQs

FUNCTIONAL BLOCK DIAGRAM



TRUTH TABLE

FUNCTION		RAS#	CAS#	WE#	OE#	ADDRESSES ^tR	ADDRESSES ^tC	DATA-IN/OUT DQ1-DQ4
Standby		H	H→X	X	X	X	X	High-Z
READ		L	L	H	L	ROW	COL	Data-Out
EARLY WRITE		L	L	L	X	ROW	COL	Data-In
READ WRITE		L	L	H→L	L→H	ROW	COL	Data-Out, Data-In
EDO-PAGE-MODE	1st Cycle	L	H→L	H	L	ROW	COL	Data-Out
READ	2nd Cycle	L	H→L	H	L	n/a	COL	Data-Out
EDO-PAGE-MODE	1st Cycle	L	H→L	L	X	ROW	COL	Data-In
EARLY-WRITE	2nd Cycle	L	H→L	L	X	n/a	COL	Data-In
EDO-PAGE-MODE	1st Cycle	L	H→L	H→L	L→H	ROW	COL	Data-Out, Data-In
READ-WRITE	2nd Cycle	L	H→L	H→L	L→H	n/a	COL	Data-Out, Data-In
RAS#-ONLY REFRESH		L	H	X	X	ROW	n/a	High-Z
HIDDEN	READ	L→H→L	L	H	L	ROW	COL	Data-Out
REFRESH	WRITE	L→H→L	L	L	X	ROW	COL	Data-In
CBR REFRESH		H→L	L	H	X	X	X	High-Z
SELF REFRESH		H→L	L	H	X	X	X	High-Z

ABSOLUTE MAXIMUM RATINGS*

Voltage on V_{CC} pin Relative to V_{SS} ..... -1V to +7.0V
Voltage on NC, Inputs or I/O pins
Relative to V_{SS} ..... -1V to +7.0V
Operating Temperature, T_A (ambient) ..... 0°C to +70°C
Storage Temperature (plastic) ..... -55°C to +150°C
Power Dissipation 1W
Short Circuit Output Current 50mA

*Stresses greater than those listed under " Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

ELECTRICAL CHARACTERISTICS AND RECOMMENDED DC OPERATING CONDITIONS

(Notes: 1, 6, 7) (V_{CC} = +5.0V ±10%)

PARAMETER/CONDITION	SYMBOL	MIN	MAX	UNITS	NOTES
Supply Voltage	V_{CC}	4.5	5.5	V	
Input High (Logic 1) Voltage, all inputs (including NC pins)	V_{IH}	2.4	V_{CC}+1	V	
Input Low (Logic 0) Voltage, all inputs (including NC pins)	V_{IL}	-1.0	0.8	V	
INPUT LEAKAGE CURRENT Any input 0V ≤ V_{IN} ≤ V_{CC}+1V (All other pins not under test = 0V)	I_I	-2	2	µA	
OUTPUT LEAKAGE CURRENT (Q is disabled; 0V ≤ V_{OUT} ≤ 5.5V)	I_{OZ}	-5	5	µA	
OUTPUT LEVELS Output High Voltage (I_{OUT} = -5mA)	V_{OH}	2.4		V	
Output Low Voltage (I_{OUT} = 4.2mA)	V_{OL}		0.4	V	

ELECTRICAL CHARACTERISTICS AND RECOMMENDED DC OPERATING CONDITIONS

(Notes: 1, 6, 7) (V_{CC} = +5.0V ±10%)

		MAX				
PARAMETER/CONDITION	SYM	-5	-6	-7	UNITS	NOTES
STANDBY CURRENT: (TTL) (RAS# = CAS# = V_{IH})	I_{CC1}	2	2	2	mA	
STANDBY CURRENT: (CMOS)	I_{CC2}	500	500	500	µA	
(RAS# = CAS# = other inputs = V_{CC} -0.2V)	I_{CC2}	150	150	150	µA	S only
OPERATING CURRENT: Random READ/WRITE Average power supply current (RAS#, CAS#, address cycling: ^{t}RC = ^{t}RC [MIN])	I_{CC3}	140	130	120	mA	3, 4, 12
OPERATING CURRENT: EDO PAGE MODE Average power supply current (RAS# = V_{IL}, CAS#, address cycling: ^{t}PC = ^{t}PC [MIN])	I_{CC4}	110	100	90	mA	3, 4, 12
REFRESH CURRENT: RAS# ONLY Average power supply current (RAS# cycling, CAS# = V_{IH}: ^{t}RC = ^{t}RC [MIN])	I_{CC5}	140	130	120	mA	3, 12
REFRESH CURRENT: CBR Average power supply current (RAS#, CAS#, address cycling: ^{t}RC = ^{t}RC [MIN])	I_{CC6}	140	130	120	mA	3, 5
REFRESH CURRENT: Extended (S version only) Average power supply current: CAS# = 0.2V or CBR cycling; RAS# = ^{t}RAS (MIN); WE#= V_{CC} -0.2V; A0-A10, OE# and D_{IN} = V_{CC} -0.2V or 0.2V (D_{IN} may be left open); ^{t}RC = 62.5µs (2,048 rows at 62.5µs = 128ms)	I_{CC7}	300	300	300	µA	3, 5
REFRESH CURRENT: Self (S version only) Average power supply current: CBR cycling with RAS# ≥ ^{t}RAS (MIN) and CAS# held low; WE#= V_{CC} -0.2V; A0-A10, OE# and D_{IN} = V_{CC} -0.2V or 0.2V (D_{IN} may be left open)	I_{CC7}	300	300	300	µA	5

CAPACITANCE

PARAMETER	SYMBOL	MAX	UNITS	NOTES
Input Capacitance: Address pins	C_{I1}	5	pF	8
Input Capacitance: RAS#, CAS#, WE#, OE#	C_{I2}	7	pF	8
Input/Output Capacitance: DQ	C_{IO}	7	pF	8

ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

(Notes: 2, 3, 6, 9, 10, 11, 12) (V_{CC} = +5.0V ±10%)

AC CHARACTERISTICS		-5		-6		-7			
PARAMETER	SYM	MIN	MAX	MIN	MAX	MIN	MAX	UNITS	NOTES
Access time from column-address	^tAA		25		30		35	ns	
Column-address set-up to CAS# precharge	^tACH	12		15		15		ns	
Column-address hold time (referenced to RAS#)	^tAR	38		45		50		ns	
Column-address setup time	^tASC	0		0		0		ns	
Row-address setup time	^tASR	0		0		0		ns	
Column-address to WE# delay time	^tAWD	48		55		60		ns	13
Access time from CAS#	^tCAC		15		15		20	ns	14
Column-address hold time	^tCAH	8		10		12		ns	
CAS# pulse width	^tCAS	10	10,000	12	10,000	12	10,000	ns	
CAS# LOW to don't care during SELF REFRSH	^tCHD	15		15		15		ns	
CAS# hold time (CBR REFRESH)	^tCHR	8		10		12		ns	7
CAS# to output in Low-Z	^tCLZ	0		0		0		ns	
Data output hold after next CAS# LOW	^tCOH	3		3		3		ns	
CAS# precharge time	^tCP	8		10		10		ns	15
Access time from CAS# precharge	^tCPA		30		35		40	ns	
CAS# to RAS# precharge time	^tCRP	5		5		5		ns	
CAS# hold time	^tCSH	40		45		50		ns	
CAS# setup time (CBR REFRESH)	^tCSR	5		5		5		ns	
CAS# to WE# delay time	^tCWD	28		35		40		ns	13
Write command to CAS# lead time	^tCWL	8		10		15		ns	
Data-in hold time	^tDH	8		10		12		ns	16
Data-in hold time (referenced to RAS#)	^tDHR	38		45		55		ns	
Data-in setup time	^tDS	0		0		0		ns	16
Output disable	^tOD	0	12	0	15	0	15	ns	
Output Enable	^tOE		12		15		20	ns	17
OE# hold time from WE# during READ-MODIFY-WRITE cycle	^tOEH	8		10		12		ns	18
OE# HIGH hold from CAS# HIGH	^tOEHC	5		10		10		ns	18
OE# HIGH pulse width	^tOEP	5		10		10		ns	
OE# LOW to CAS# HIGH setup time	^tOES	4		5		5		ns	

ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

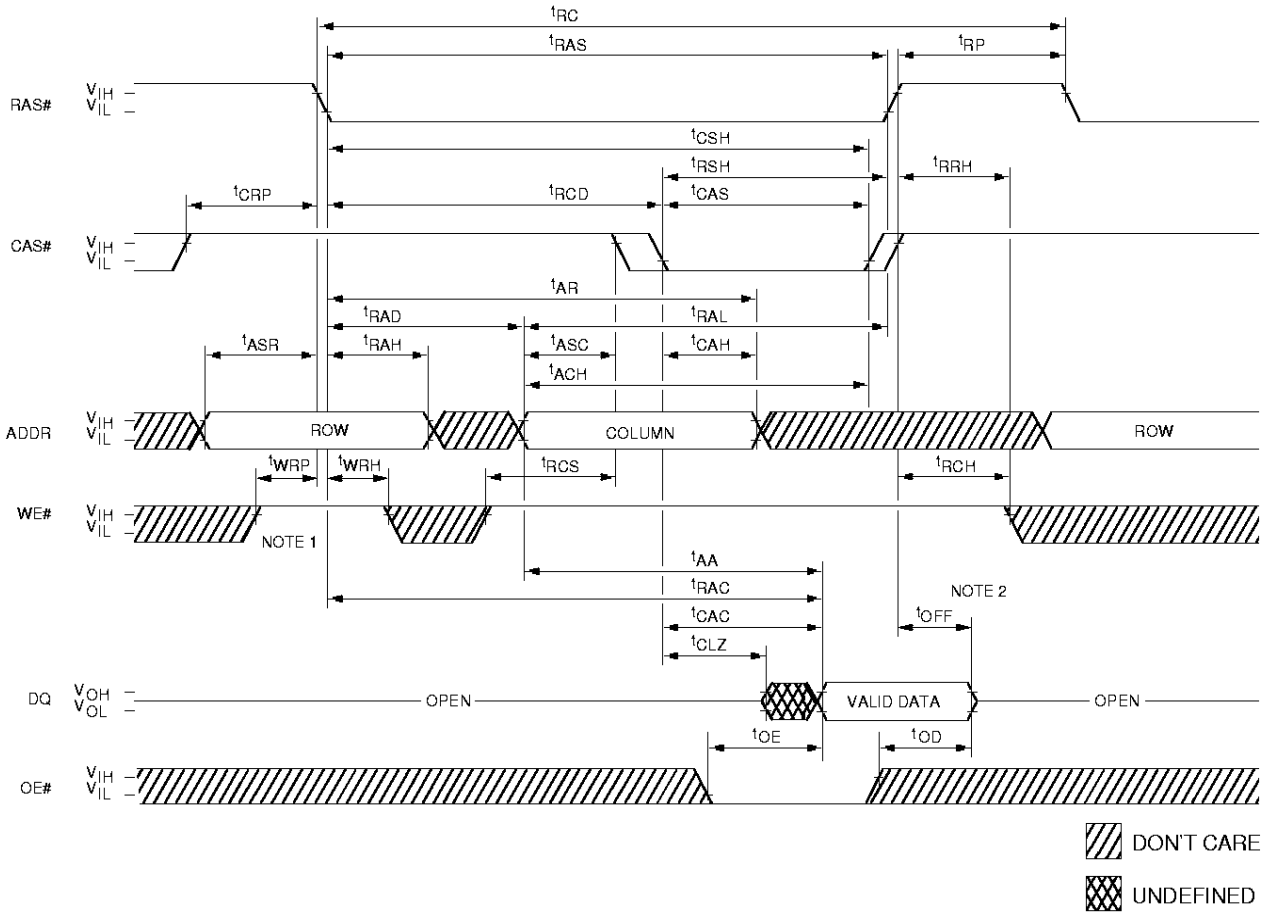
(Notes: 2, 3, 6, 9, 10, 11, 12, 20) (V_{CC} = +5.0V ±10%)

AC CHARACTERISTICS		-5		-6		-7			
PARAMETER	SYM	MIN	MAX	MIN	MAX	MIN	MAX	UNITS	NOTES
Output buffer turn-off delay	t_{OFF}	0	12	0	15	0	15	ns	20
OE# setup prior to RAS# during HIDDEN REFRESH cycle	t_{ORD}	0		0		0		ns	
EDO-PAGE-MODE READ or WRITE cycle time	t_{PC}	25		25		30		ns	
EDO-PAGE-MODE READ-WRITE cycle time	t_{PRWC}	52		66		75		ns	
Access time from RAS#	t_{RAC}		50		60		70	ns	19
RAS# to column-address delay time	t_{RAD}	9	25	12	30	12	35	ns	21
Row-address hold time	t_{RAH}	9		10		10		ns	
Column-address to RAS# lead time	t_{RAL}	25		30		35		ns	
RAS# pulse width	t_{RAS}	50	10,000	60	10,000	70	10,000	ns	
RAS# pulse width (EDO PAGE MODE)	t_{RASP}	50	125,000	60	125,000	70	125,000	ns	
RAS# pulse width during SELF REFRSH	t_{RASS}	100		100		100		µs	
Random READ or WRITE cycle time	t_{RC}	90		105		125		ns	
RAS# to CAS# delay time	t_{RCD}	11	35	14	45	14	50	ns	22
Read command hold time (referenced to CAS#)	t_{RCH}	0		0		0		ns	23
Read command setup time	t_{RCS}	0		0		0		ns	
Refresh period (2,048 cycles)	t_{REF}		32		32		32	ms	
Refresh period (2,048 cycles) S version	t_{REF}		128		128		128	ms	
RAS# precharge time	t_{RP}	30		40		50		ns	
RAS# to CAS# precharge time	t_{RPC}	5		5		5		ns	
RAS# precharge time exiting SELF REFRSH	t_{RPS}	90		105		125		ns	
Read command hold time (referenced to RAS#)	t_{RRH}	0		0		0		ns	23
RAS# hold time	t_{RSH}	13		15		15		ns	
READ WRITE cycle time	t_{RWC}	135		150		170		ns	
RAS# to WE# delay time	t_{RWD}	73		80		90		ns	13
Write command to RAS# lead time	t_{RWL}	13		15		15		ns	
Transition time (rise or fall)	t_{T}	2	50	2	50	2	50	ns	
Write command hold time	t_{WCH}	8		10		12		ns	
Write command hold time (referenced to RAS#)	t_{WCR}	38		45		55		ns	
WE# command setup time	t_{WCS}	0		0		0		ns	13
Output disable delay from WE#	t_{WHZ}	0	12	0	15	0	15	ns	
Write command pulse width	t_{WP}	7		10		12		ns	
WE# pulse to disable at CAS# HIGH	t_{WPZ}	7		10		12		ns	
WE# hold time (CBR REFRESH)	t_{WRH}	8		10		10		ns	
WE# setup time (CBR REFRESH)	t_{WRP}	8		10		10		ns	

NOTES

1. All voltages referenced to V_{SS}.
2. The minimum specifications are used only to indicate cycle time at which proper operation over the full temperature range (0 C ≤ T_A ≤ 70 C) is assured.
3. An initial pause of 100µs is required after power-up followed by eight RAS# refresh cycles (RAS#-ONLY or CBR with WE# HIGH) before proper device operation is assured. The eight RAS# cycle wake-ups should be repeated any time the ^tREF refresh requirement is exceeded.
4. NC pins are assumed to be left floating and are not tested for leakage.
5. I_{CC} is dependent on output loading and cycle rates. Specified values are obtained with minimum cycle time and the outputs open.
6. Column address changed once each cycle.
7. Enables on-chip refresh and address counters.
8. This parameter is sampled. V_{CC} = +4.5V; f = 1 MHz.
9. AC characteristics assume ^tT = 2.5ns.
10. V_{IH} (MIN) and V_{IL} (MAX) are reference levels for measuring timing of input signals. Transition times are measured between V_{IH} and V_{IL} (or between V_{IL} and V_{IH}).
11. In addition to meeting the transition rate specification, all input signals must transit between V_{IH} and V_{IL} (or between V_{IL} and V_{IH}) in a monotonic manner.
12. Measured with a load equivalent to two TTL gates, 100pF and V_{OL} = 0.8V and V_{OH} = 2.0V.
13. ^tWCS, ^tRWD, ^tAWD and ^tCWD are not restrictive operating parameters. ^tWCS applies to EARLY WRITE cycles. ^tRWD, ^tAWD and ^tCWD apply to READ-MODIFY-WRITE cycles. If ^tWCS ≥ ^tWCS (MIN), the cycle is an EARLY WRITE cycle and the data output will remain an open circuit throughout the entire cycle. If ^tWCS < ^tWCS (MIN) and ^tRWD ≥ ^tRWD (MIN), ^tAWD ≥ ^tAWD (MIN) and ^tCWD ≥ ^tCWD (MIN), the cycle is a READ-MODIFY-WRITE and the data output will contain data read from the selected cell. If neither of the above conditions is met, the state of data-out is indeterminate. OE# held HIGH and WE# taken LOW after CAS# goes LOW results in a LATE WRITE (OE#-controlled) cycle. ^tWCS, ^tRWD, ^tCWD and ^tAWD are not applicable in a LATE WRITE cycle.
14. Assumes that ^tRCD ≥ ^tRCD (MAX).
15. If CAS# is LOW at the falling edge of RAS#, Q will be maintained from the previous cycle. To initiate a new cycle and clear the data-out buffer, CAS# must be pulsed HIGH for ^tCP.
16. These parameters are referenced to CAS# leading edge in EARLY WRITE cycles and WE# leading edge in LATE WRITE or READ-MODIFY-WRITE cycles.
17. If OE# is tied permanently LOW, LATE WRITE or READ-MODIFY-WRITE operations are not permissible and should not be attempted. Additionally, WE# must be pulsed during CAS# HIGH time in order to place I/O buffers in High-Z.
18. LATE WRITE and READ-MODIFY-WRITE cycles must have both ^tOD and ^tOEH met (OE# HIGH during WRITE cycle) in order to ensure that the output buffers will be open during the WRITE cycle. The DQs will provide the previously read data if CAS# remains LOW and OE# is taken back LOW after ^tOEH is met. If CAS# goes HIGH prior to OE# going back LOW, the DQs will remain open.
19. Assumes that ^tRCD < ^tRCD (MAX). If ^tRCD is greater than the maximum recommended value shown in this table, ^tRAC will increase by the amount that ^tRCD exceeds the value shown.
20. ^tOFF (MAX) defines the time at which the output achieves the open circuit condition, and is not referenced to V_{OH} or V_{OL}. It is referenced from the rising edge of RAS# or CAS#, whichever occurs last.
21. Operation within the ^tRAD (MAX) limit ensures that ^tRAC (MIN) and ^tCAC (MIN) can be met. ^tRAD (MAX) is specified as a reference point only; if ^tRAD is greater than the specified ^tRAD (MAX) limit, then access time is controlled exclusively by ^tAA, provided ^tRCD is not exceeded.
22. Operation within the ^tRCD (MAX) limit ensures that ^tRAC (MAX) can be met. ^tRCD (MAX) is specified as a reference point only; if ^tRCD is greater than the specified ^tRCD (MAX) limit, then access time is controlled exclusively by ^tCAC, provided ^tRAD is not exceeded.
23. Either ^tRCH or ^tRRH must be satisfied for a READ cycle.
24. A HIDDEN REFRESH may also be performed after a WRITE cycle. In this case, WE# = LOW and OE# = HIGH.

READ CYCLE



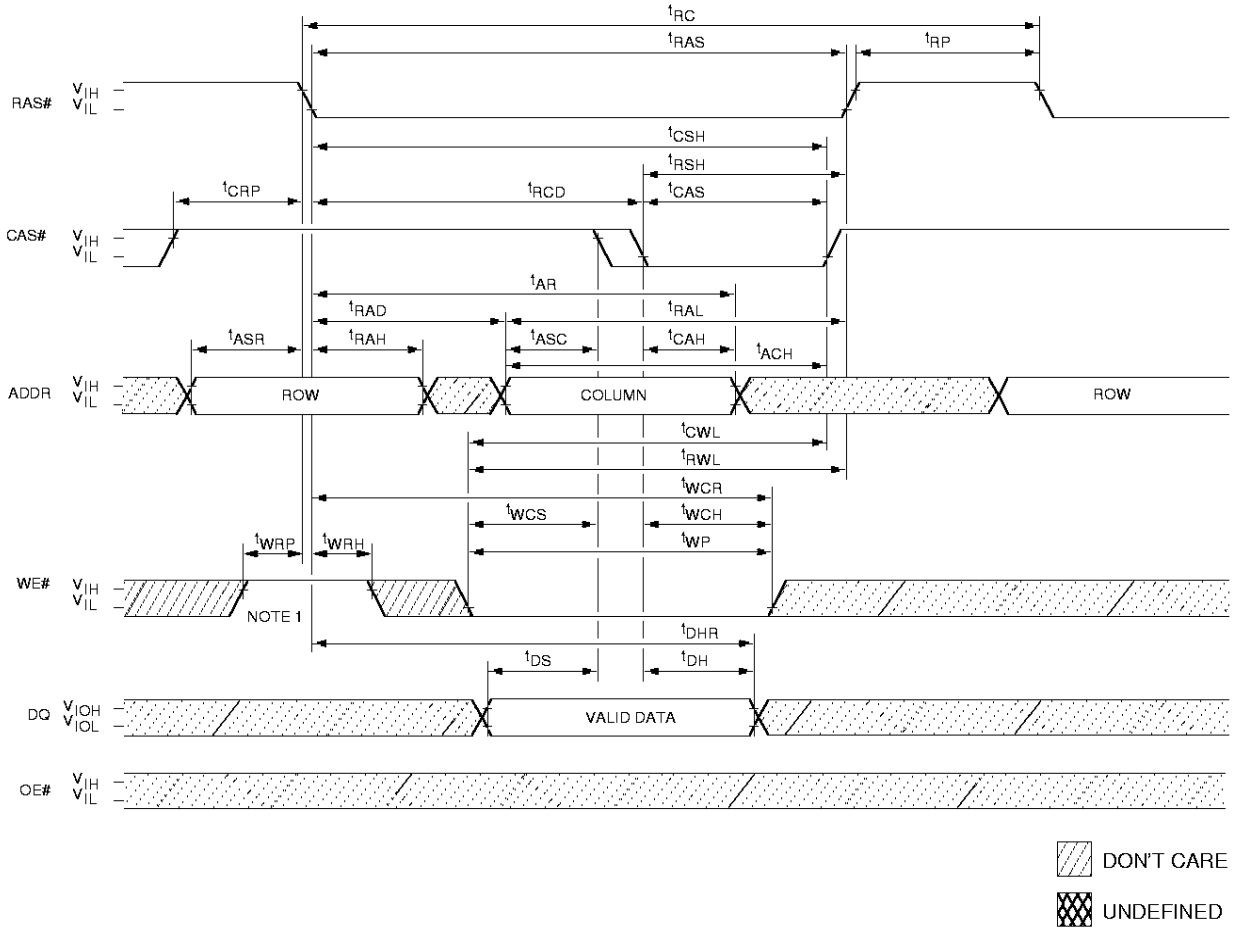
NOTE: 1. Although WE# is a "don't care" at RAS# time during an access cycle (READ or WRITE), the system designer should implement WE# HIGH for ^{t}WRP and ^{t}WRH. This design implementation will facilitate compatibility with future EDO DRAMs.
2. ^{t}OFF is referenced from rising edge of RAS# or CAS#, whichever occurs last.

TIMING PARAMETERS

	-5		-6		-7		
SYM	MIN	MAX	MIN	MAX	MIN	MAX	UNITS
^{t}AA		25		30		35	ns
^{t}ACH	12		15		15		
^{t}AR	38		45		50		ns
^{t}ASC	0		0		0		ns
^{t}ASR	0		0		0		ns
^{t}CAC		15		15		20	ns
^{t}CAH	8		10		12		ns
^{t}CAS	10	10,000	12	10,000	12	10,000	ns
^{t}CLZ	0		0		0		ns
^{t}CRP	5		5		5		ns
^{t}CSH	40		45		50		ns
^{t}OD	0	12	0	15	0	15	ns
^{t}OE		12		15		20	ns
^{t}OFF	0	12	0	15	0	15	ns

	-5		-6		-7		
SYM	MIN	MAX	MIN	MAX	MIN	MAX	UNITS
^{t}RAC		50		60		70	ns
^{t}RAD	9	25	12	30	12	35	ns
^{t}RAH	9		10		10		ns
^{t}RAL	25		30		35		ns
^{t}RAS	50	10,000	60	10,000	70	10,000	ns
^{t}RC	90		105		125		ns
^{t}RCD	11	35	14	45	14	50	ns
^{t}RCH	0		0		0		ns
^{t}RCS	0		0		0		ns
^{t}RP	30		40		50		ns
^{t}RRH	0		0		0		ns
^{t}RSH	13		15		15		ns
^{t}WRH	8		10		10		ns
^{t}WRP	8		10		10		ns

EARLY WRITE CYCLE



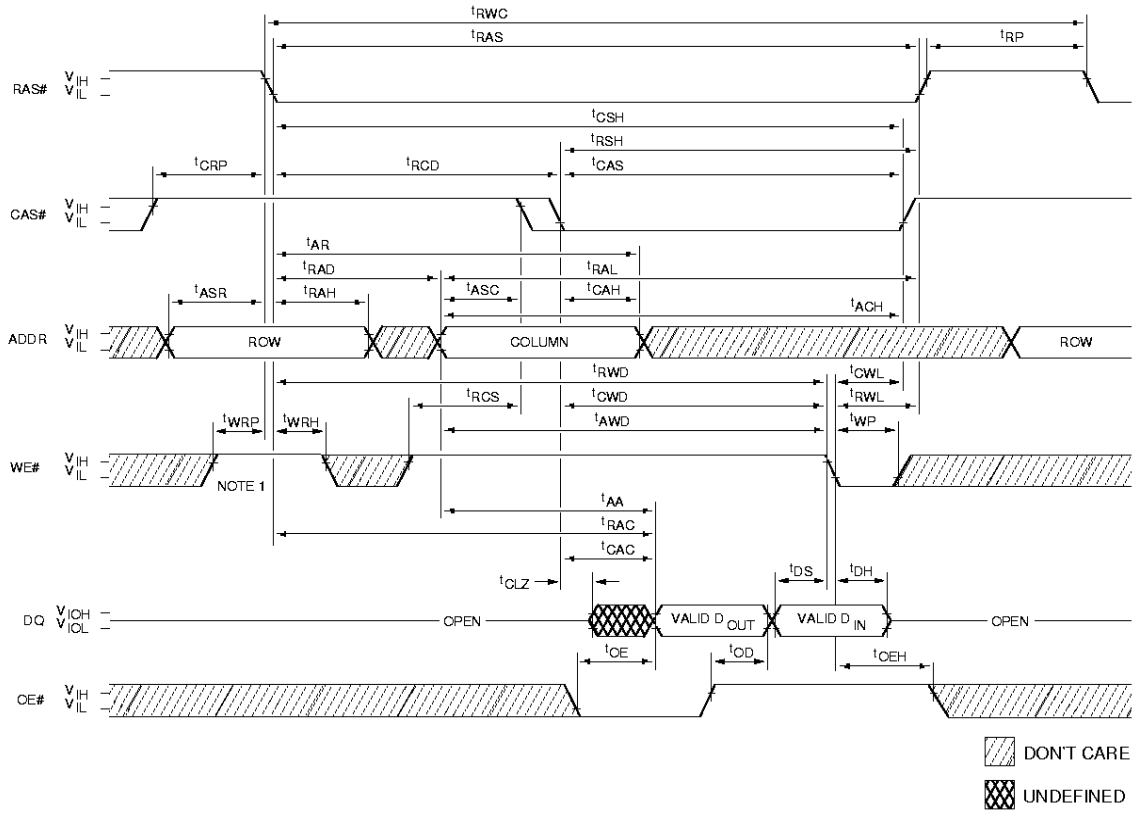
NOTE: 1. Although WE# is a "don't care" at RAS# time during an access cycle (READ or WRITE), the system designer should implement WE# HIGH for tWRP and tWRH. This design implementation will facilitate compatibility with future EDO DRAMs.

TIMING PARAMETERS

	-5		-6		-7		
SYM	MIN	MAX	MIN	MAX	MIN	MAX	UNITS
tACH	15		15		15		ns
tAR	38		45		50		ns
tASC	0		0		0		ns
tASR	0		0		0		ns
tCAH	8		10		12		ns
tCAS	10	10,000	12	10,000	12	10,000	ns
tCRP	5		5		5		ns
tCSH	40		45		50		ns
tCWL	8		10		15		ns
tDH	8		10		12		ns
tDHR	38		45		55		ns
tDS	0		0		0		ns
tRAD	9	25	12	30	12	35	ns
tRAH	9		10		10		ns

	-5		-6		-7		
SYM	MIN	MAX	MIN	MAX	MIN	MAX	UNITS
tRAL	25		30		35		ns
tRAS	50	10,000	60	10,000	70	10,000	ns
tRC	90		105		125		ns
tRCD	11	35	14	45	14	50	ns
tRP	30		40		50		ns
tRSH	13		15		15		ns
tRWL	13		15		15		ns
tWCH	8		10		12		ns
tWCR	38		45		55		ns
tWCS	0		0		0		ns
tWP	7		10		12		ns
tWRH	8		10		10		ns
tWRP	8		10		10		ns

READ WRITE CYCLE
(LATE WRITE and READ-MODIFY-WRITE cycles)



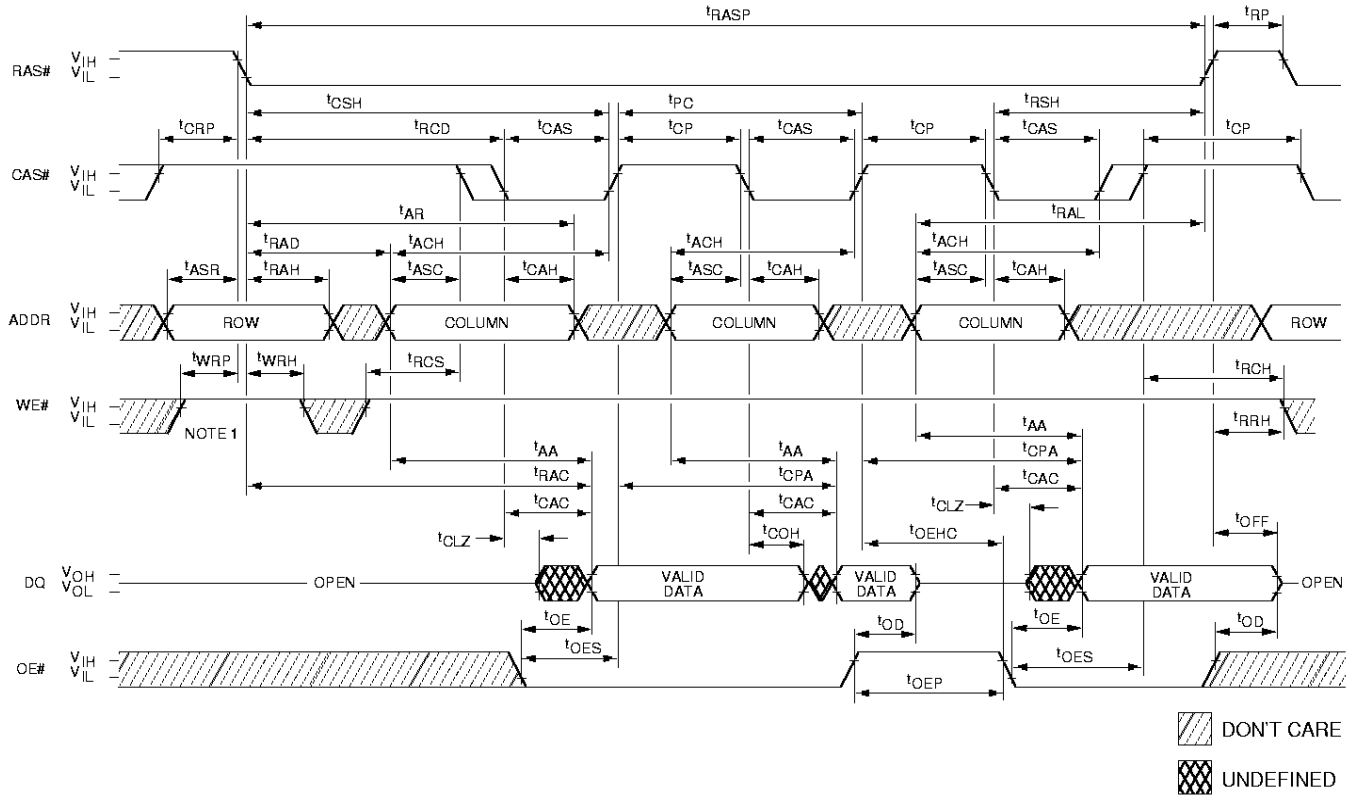
NOTE: 1. Although WE# is a "don't care" at RAS# time during an access cycle (READ or WRITE), the system designer should implement WE# HIGH for ^{t}WRP and ^{t}WRH. This design implementation will facilitate compatibility with future EDO DRAMs.

TIMING PARAMETERS

	-5		-6		-7		
SYM	MIN	MAX	MIN	MAX	MIN	MAX	UNITS
^{t}AA		25		30		35	ns
^{t}ACH	12		15		15		ns
^{t}AR	38		45		55		ns
^{t}ASC	0		0		0		ns
^{t}AWD	48		55		60		ns
^{t}ASR	0		0		0		ns
^{t}CAC		15		15		20	ns
^{t}CAH	8		10		12		ns
^{t}CAS	10	10,000	12	10,000	12	10,000	ns
^{t}CLZ	0		0		0		ns
^{t}CRP	5		5		5		ns
^{t}CSH	40		45		50		ns
^{t}CWD	28		35		40		ns
^{t}CWL	8		10		15		ns
^{t}DH	8		10		12		ns
^{t}DS	0		0		0		ns
^{t}OD	0	12	0	15	0	15	ns

	-5		-6		-7		
SYM	MIN	MAX	MIN	MAX	MIN	MAX	UNITS
^{t}OE		12		15		20	ns
^{t}OEH	8		10		12		ns
^{t}RAC		50		60		70	ns
^{t}RAD	9	25	12	30	12	35	ns
^{t}RAH	9		10		10		ns
^{t}RAL	25		30		35		ns
^{t}RAS	50	10,000	60	10,000	70	10,000	ns
^{t}RCD	11	35	14	45	14	50	ns
^{t}RCS	0		0		0		ns
^{t}RP	30		40		50		ns
^{t}RSH	13		15		15		ns
^{t}RWC	135		150		170		ns
^{t}RWD	73		80		90		ns
^{t}RWL	13		15		15		ns
^{t}WP	7		10		12		ns
^{t}WRH	8		10		10		ns
^{t}WRP	8		10		10		ns

EDO-PAGE-MODE READ CYCLE



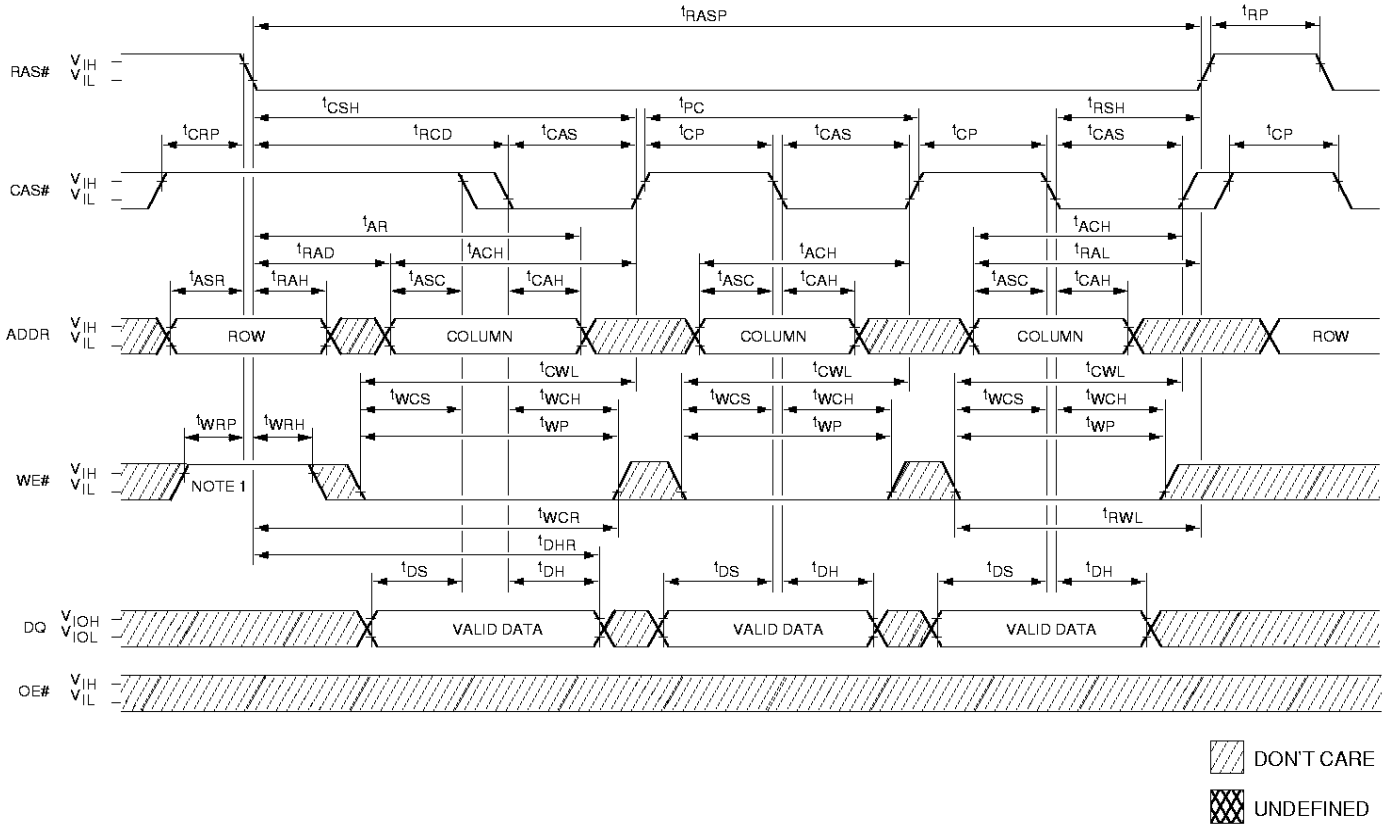
NOTE: 1. Although WE# is a "don't care" at RAS# time during an access cycle (READ or WRITE), the system designer should implement WE# HIGH for ^{t}WRP and ^{t}WRH. This design implementation will facilitate compatibility with future EDO DRAMs.

TIMING PARAMETERS

	-5		-6		-7		
SYM	MIN	MAX	MIN	MAX	MIN	MAX	UNITS
^{t}AA		25		30		35	ns
^{t}ACH	12		15		15		ns
^{t}AR	38		45		50		ns
^{t}ASC	0		0		0		ns
^{t}ASR	0		0		0		ns
^{t}CAC		15		15		20	ns
^{t}CAH	8		10		12		ns
^{t}CAS	10	10,000	12	10,000	12	10,000	ns
^{t}CLZ	0		0		0		ns
^{t}COH	3		3		3		ns
^{t}CP	8		10		10		ns
^{t}CPA		30		35		40	ns
^{t}CRP	5		5		5		ns
^{t}CSH	40		45		50		ns
^{t}OD	0	12	0	15	0	15	ns
^{t}OE		12		15		20	ns
^{t}OEHC	5		10		10		ns

	-5		-6		-7		
SYM	MIN	MAX	MIN	MAX	MIN	MAX	UNITS
^{t}OEP	5		10		10		ns
^{t}OES	4		5		5		ns
^{t}OFF	0	12	0	15	0	15	ns
^{t}PC	25		25		30		ns
^{t}RAC		50		60		70	ns
^{t}RAD	9	25	12	30	12	35	ns
^{t}RAH	9		10		10		ns
^{t}RAL	25		30		35		ns
^{t}RASP	50	125,000	60	125,000	70	125,000	ns
^{t}RCD	11	35	14	45	14	50	ns
^{t}RCH	0		0		0		ns
^{t}RCS	0		0		0		ns
^{t}RP	30		40		50		ns
^{t}RRH	0		0		0		ns
^{t}RSH	13		15		15		ns
^{t}WRH	8		10		10		ns
^{t}WRP	8		10		10		ns

EDO-PAGE-MODE EARLY-WRITE CYCLE



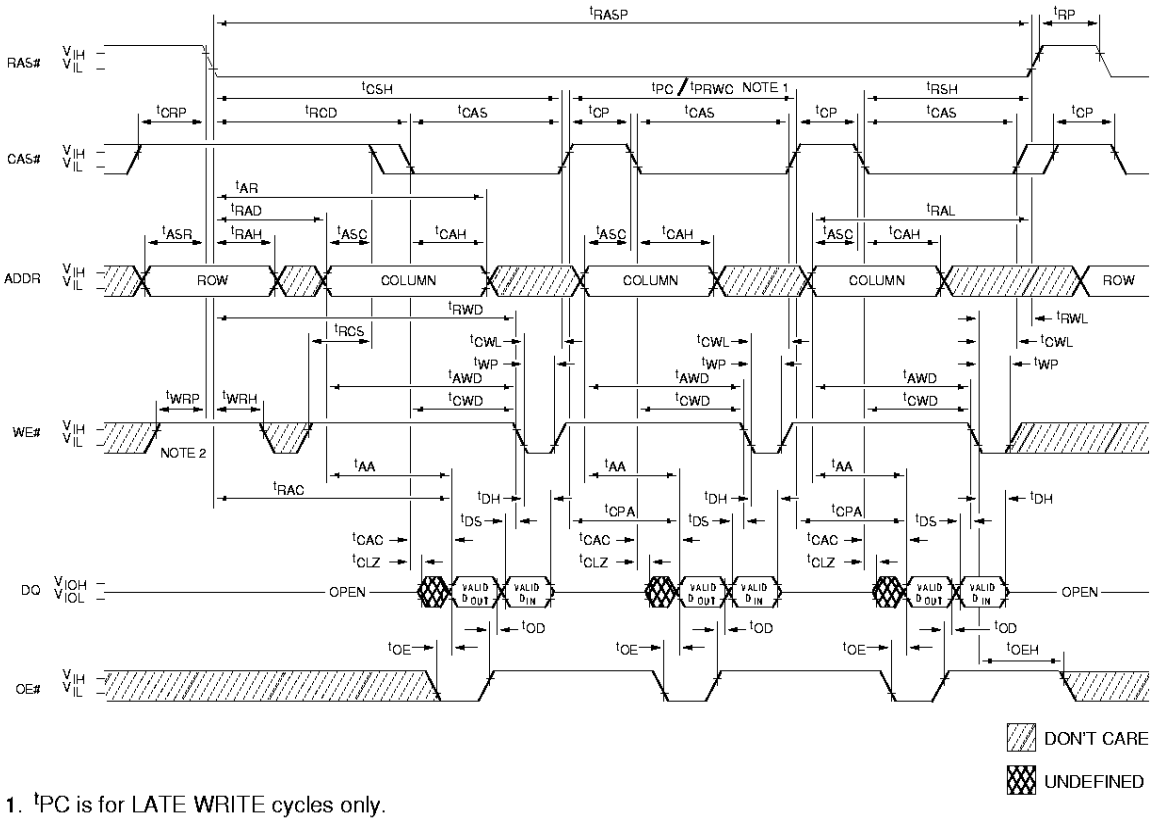
NOTE: 1. Although WE# is a "don't care" at RAS# time during an access cycle (READ or WRITE), the system designer should implement WE# HIGH for tWRP and tWRH. This design implementation will facilitate compatibility with future EDO DRAMs.

TIMING PARAMETERS

	-5		-6		-7		
SYM	MIN	MAX	MIN	MAX	MIN	MAX	UNITS
tACH	12		15		15		ns
tAR	38		45		50		ns
tASC	0		0		0		ns
tASR	0		0		0		ns
tCAH	8		10		12		ns
tCAS	10	10,000	12	10,000	12	10,000	ns
tCP	8		10		10		ns
tCRP	5		5		5		ns
tCSH	40		45		50		ns
tCWL	8		10		15		ns
tDH	8		10		12		ns
tDHR	38		45		55		ns
tDS	0		0		0		ns
tPC	25		25		30		ns

	-5		-6		-7		
SYM	MIN	MAX	MIN	MAX	MIN	MAX	UNITS
tRAD	9	25	12	30	12	35	ns
tRAH	9		10		10		ns
tRAL	25		30		35		ns
tRASP	50	125,000	60	125,000	70	125,000	ns
tRCD	11	35	14	45	14	50	ns
tRP	30		40		50		ns
tRSH	13		15		15		ns
tRWL	13		15		15		ns
tWCH	8		10		12		ns
tWCR	38		45		55		ns
tWCS	0		0		0		ns
tWP	7		10		12		ns
tWRH	8		10		10		ns
tWRP	8		10		10		ns

EDO-PAGE-MODE READ-WRITE CYCLE
(LATE WRITE and READ-MODIFY-WRITE cycles)



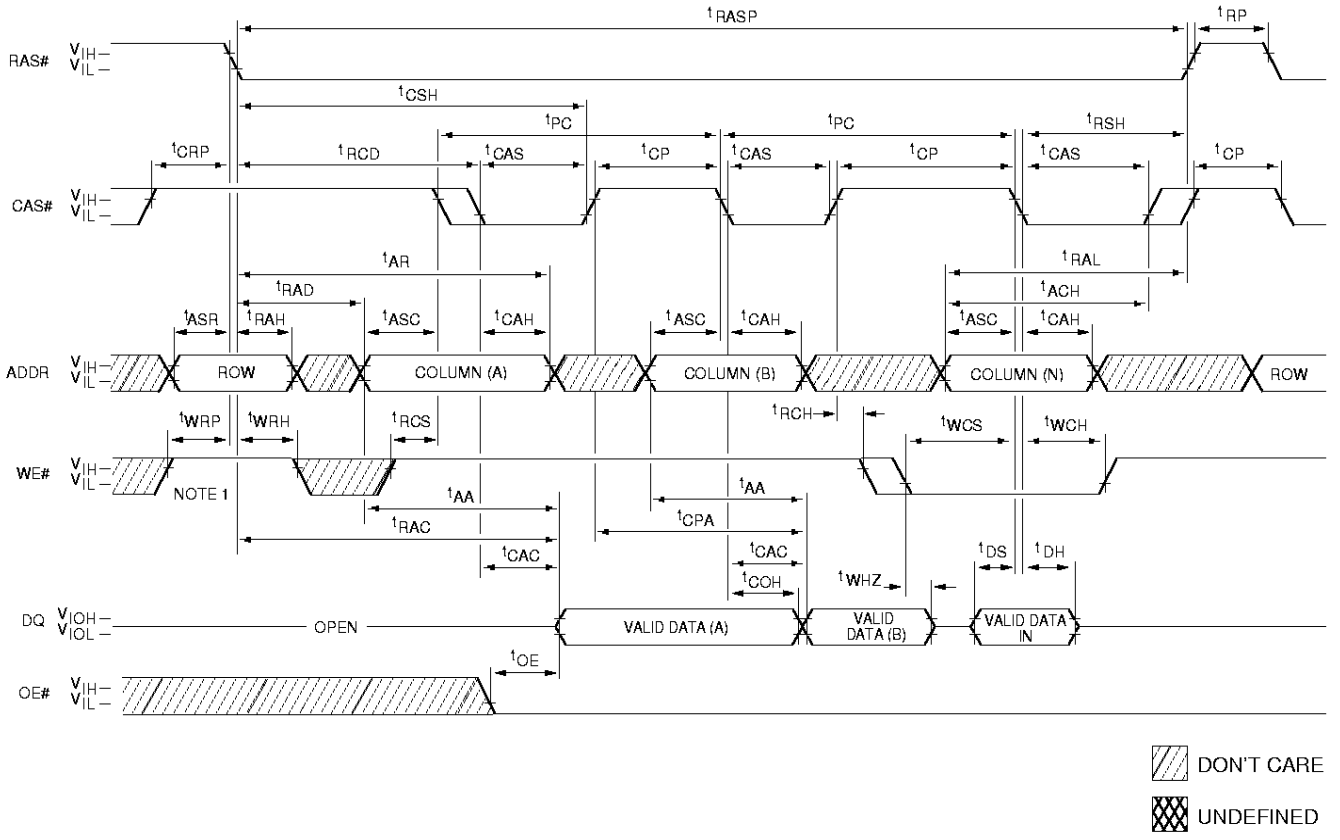
NOTE:
1. tPC is for LATE WRITE cycles only.
2. Although WE# is a "don't care" at RAS# time during an access cycle (READ or WRITE), the system designer should implement WE# HIGH for tWRP and tWRH. This design implementation will facilitate compatibility with future EDO DRAMs.

TIMING PARAMETERS

	-5		-6		-7		
SYM	MIN	MAX	MIN	MAX	MIN	MAX	UNITS
tAA		25		30		35	ns
tAR	38		45		50		ns
tASC	0		0		0		ns
tASR	0		0		0		ns
tAWD	48		55		60		ns
tCAC		15		15		20	ns
tCAH	8		10		12		ns
tCAS	10	10,000	12	10,000	12	10,000	ns
tCLZ	0		0		0		ns
tCP	8		10		10		ns
tCPA		30		35		40	ns
tCRP	5		5		5		ns
tCSH	40		45		50		ns
tCWD	28		35		40		ns
tCWL	8		10		15		ns
tDH	8		10		12		ns
tDS	0		0		0		ns
tOD	0	12	0	15	0	15	ns

	-5		-6		-7		
SYM	MIN	MAX	MIN	MAX	MIN	MAX	UNITS
tOE		12		15		20	ns
tOEH	8		12		12		ns
tPC	25		25		30		ns
tPRWC	52		66		75		ns
tRAC		50		60		70	ns
tRAD	9	25	12	30	12	35	ns
tRAH	9		10		10		ns
tRAL	25		30		35		ns
tRASP	50	125,000	60	125,000	70	125,000	ns
tRCD	11	35	14	45	14	50	ns
tRCS	0		0		0		ns
tRP	30		40		50		ns
tRSH	13		15		15		ns
tRWD	73		80		90		ns
tRWL	13		15		15		ns
tWP	7		10		12		ns
tWRH	8		10		10		ns
tWRP	8		10		10		ns

EDO-PAGE-MODE READ-EARLY-WRITE CYCLE
(Pseudo READ-MODIFY-WRITE)



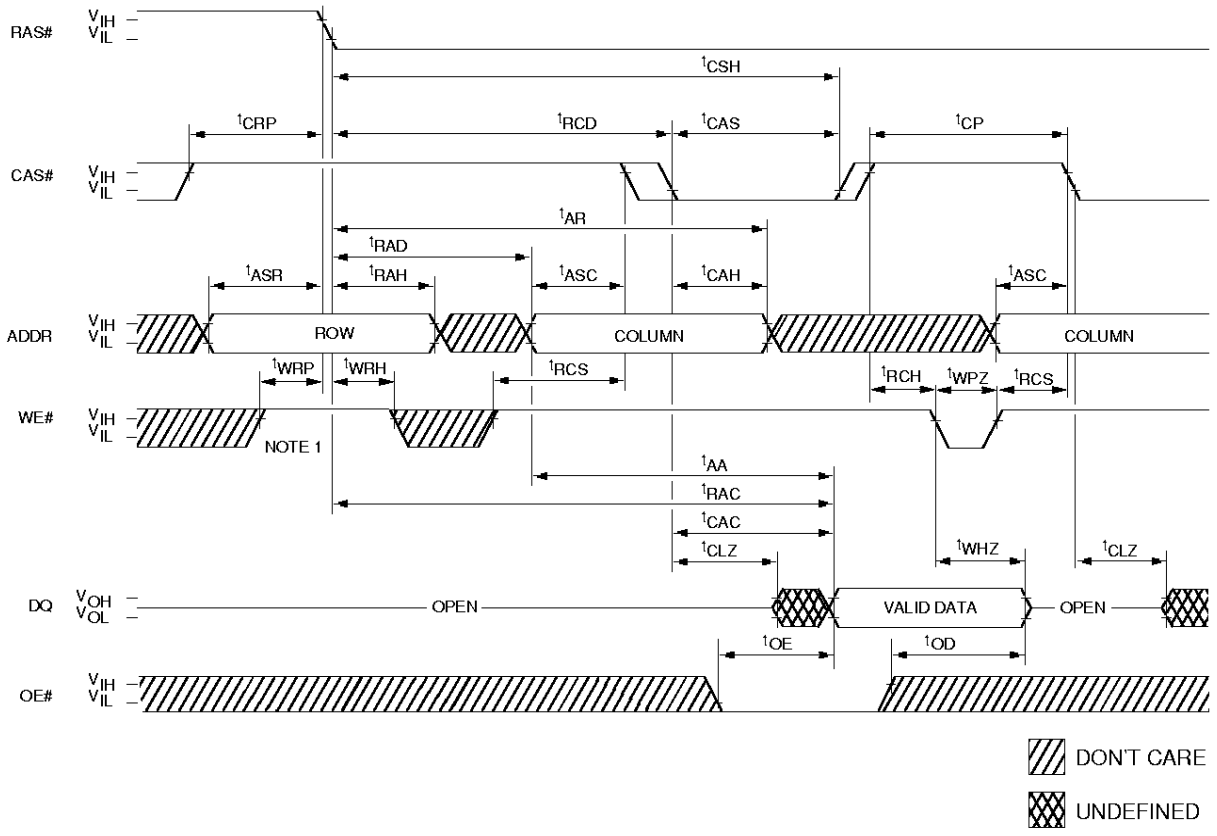
NOTE: 1. Although WE# is a "don't care" at RAS# time during an access cycle (READ or WRITE), the system designer should implement WE# HIGH for tWRP and tWRH. This design implementation will facilitate compatibility with future EDO DRAMs.

TIMING PARAMETERS

	-5		-6		-7		
SYM	MIN	MAX	MIN	MAX	MIN	MAX	UNITS
tAA		25		30		35	ns
tACH	12		15		15		ns
tAR	38		45		50		ns
tASC	0		0		0		ns
tASR	0		0		0		ns
tCAC		15		15		20	ns
tCAH	8		10		12		ns
tCAS	10	10,000	12	10,000	12	10,000	ns
tCOH	3		3		3		ns
tCP	8		10		10		ns
tCPA		30		35		40	ns
tCRP	5		5		5		ns
tCSH	40		45		50		ns
tDH	8		10		12		ns
tDS	0		0		0		ns
tOE		12		15		20	ns

	-5		-6		-7		
SYM	MIN	MAX	MIN	MAX	MIN	MAX	UNITS
tPC	25		25		30		ns
tRAC		50		60		70	ns
tRAD	9	25	12	30	12	35	ns
tRAH	9		10		10		ns
tRAL	25		30		35		ns
tRASP	50	125,000	60	125,000	70	125,000	ns
tRCD	11	35	14	45	14	50	ns
tRCH	0		0		0		ns
tRCS	0		0		0		ns
tRP	30		40		50		ns
tRSH	13		15		15		ns
tWCH	8		10		12		ns
tWCS	0		0		0		ns
tWHZ		12		15		15	ns
tWRH	8		10		10		ns
tWRP	8		10		10		ns

READ CYCLE
(with WE#-controlled disable)



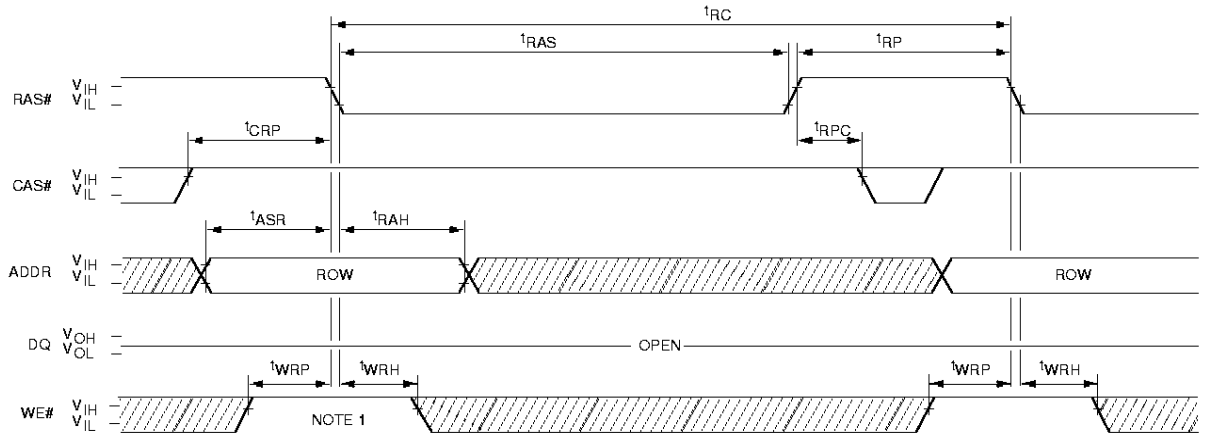
NOTE: 1. Although WE# is a "don't care" at RAS# time during an access cycle (READ or WRITE), the system designer should implement WE# HIGH for tWRP and tWRH. This design implementation will facilitate compatibility with future EDO DRAMs.

TIMING PARAMETERS

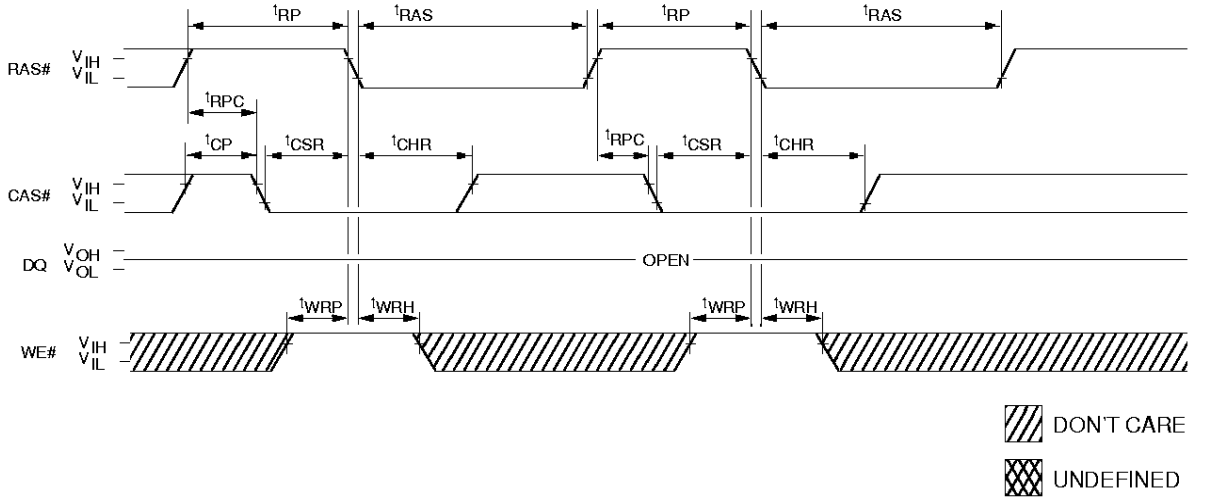
	-5		-6		-7		
SYM	MIN	MAX	MIN	MAX	MIN	MAX	UNITS
tAA		25		30		35	ns
tAR	38		45		50		ns
tASC	0		0		0		ns
tASR	0		0		0		ns
tCAC		15		15		20	ns
tCAH	8		10		12		ns
tCAS	10	10,000	12	10,000	12	10,000	ns
tCLZ	0		0		0		ns
tCP	8		10		10		ns
tCRP	5		5		5		ns
tCSH	40		45		50		ns
tOD	0	12	0	15	0	15	ns

	-5		-6		-7		
SYM	MIN	MAX	MIN	MAX	MIN	MAX	UNITS
tOE		12		15		20	ns
tRAC		50		60		70	ns
tRAD	9	25	12	30	12	35	ns
tRAH	9		10		10		ns
tRCD	11	35	14	45	14	50	ns
tRCH	0		0		0		ns
tRCS	0		0		0		ns
tWHZ		12		15		15	ns
tWPZ	7		10		12		ns
tWRH	8		10		10		ns
tWRP	8		10		10		ns

RAS#-ONLY REFRESH CYCLE



CBR REFRESH CYCLE
(Addresses and OE# = DON'T CARE)



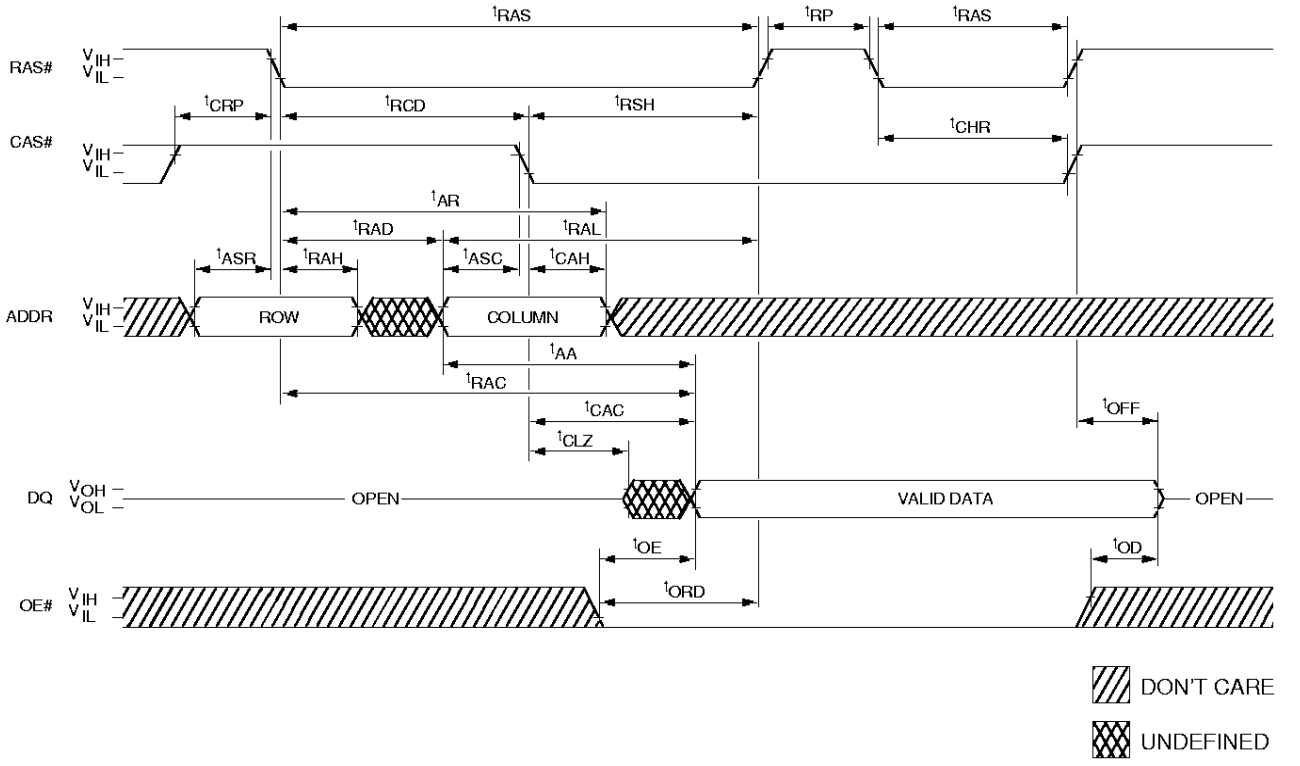
NOTE: 1. Although WE# is a "don't care" at RAS# time during an access cycle (READ or WRITE), the system designer should implement WE# HIGH for tWRP and tWRH. This design implementation will facilitate compatibility with future EDO DRAMs.

TIMING PARAMETERS

	-5		-6		-7		
SYM	MIN	MAX	MIN	MAX	MIN	MAX	UNITS
tASR	0		0		0		ns
tCHR	8		10		12		ns
tCP	8		10		10		ns
tCRP	5		5		5		ns
tCSR	5		5		5		ns
tRAH	9		10		10		ns

	-5		-6		-7		
SYM	MIN	MAX	MIN	MAX	MIN	MAX	UNITS
tRAS	50	10,000	60	10,000	70	10,000	ns
tRC	90		105		125		ns
tRP	30		40		50		ns
tRPC	5		5		5		ns
tWRH	8		10		10		ns
tWRP	8		10		10		ns

HIDDEN REFRESH CYCLE [24]
(WE# = HIGH; OE# = LOW)

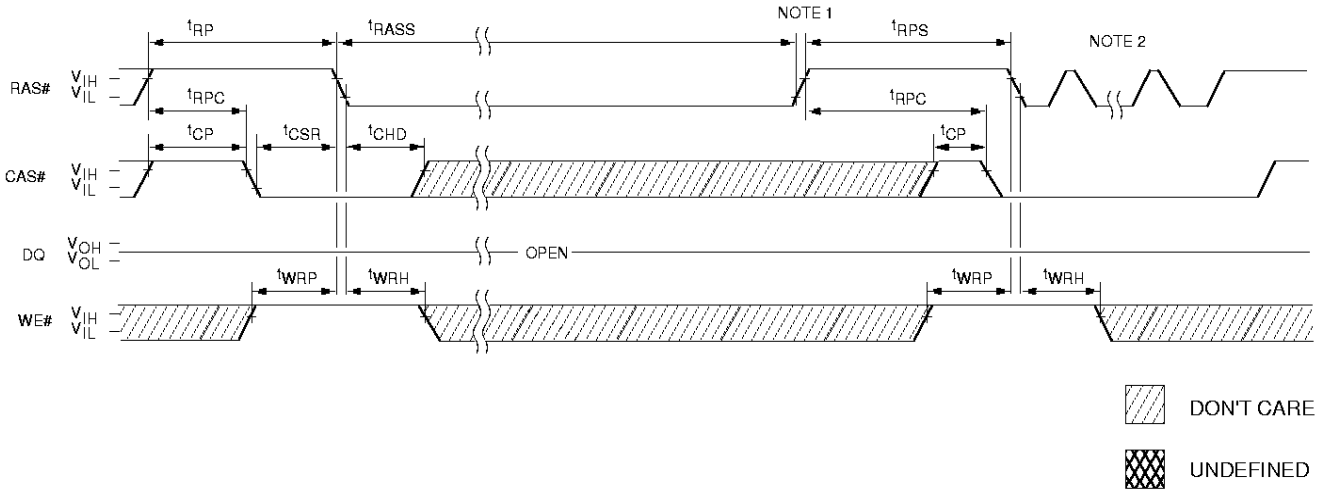


TIMING PARAMETERS

	-5		-6		-7		
SYM	MIN	MAX	MIN	MAX	MIN	MAX	UNITS
tAA		25		30		35	ns
tAR	38		45		50		ns
tASC	0		0		0		ns
tASR	0		0		0		ns
tCAC		15		15		20	ns
tCAH	8		10		12		ns
tCHR	8		10		12		ns
tCLZ	0		0		0		ns
tCRP	5		5		5		ns
tOD	0	12	0	15	0	15	ns
tOE		12		15		20	ns

	-5		-6		-7		
SYM	MIN	MAX	MIN	MAX	MIN	MAX	UNITS
tOFF	0	12	0	15	0	15	ns
tORD	0		0		0		ns
tRAC		50		60		70	ns
tRAD	9	25	12	30	12	35	ns
tRAH	9		10		10		ns
tRAL	24		30		35		ns
tRAS	50	10,000	60	10,000	70	10,000	ns
tRCD	11	35	14	45	14	50	ns
tRP	30		40		50		ns
tRSH	12		13		15		ns

SELF REFRESH CYCLE
(Addresses and OE# = DON'T CARE)



NOTE: 1. Once tRASS (MIN) is met and RAS# remains LOW, the DRAM will enter SELF REFRESH mode.
2. Once tRPS is satisfied, a complete burst of all rows should be executed.

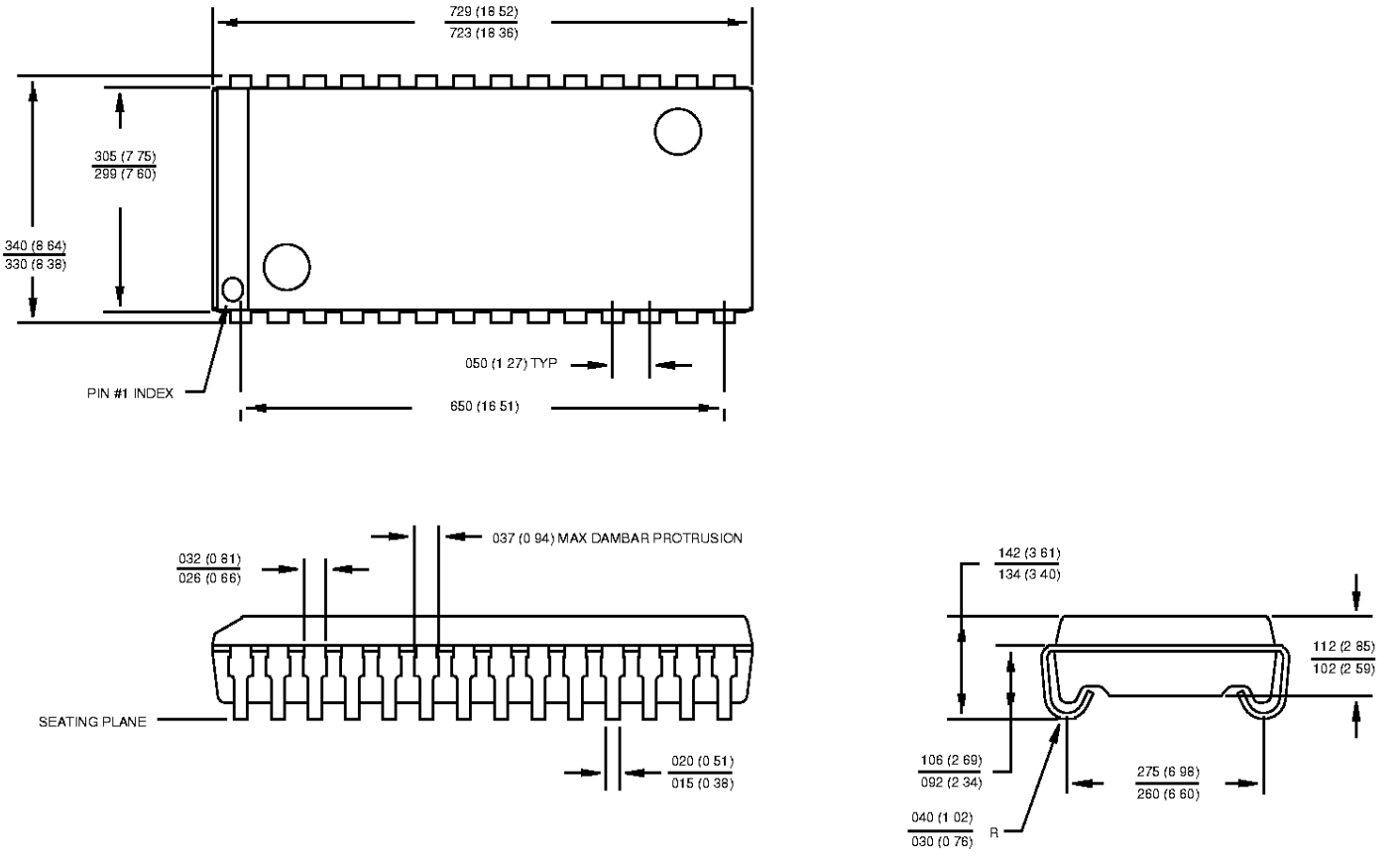
TIMING PARAMETERS

	-5		-6		-7		
SYM	MIN	MAX	MIN	MAX	MIN	MAX	UNITS
tCHD	15		15		15		ns
tCP	8		10		10		ns
tCSR	5		5		5		ns
tRASS	100		100		100		µs
tRP	30		40		50		ns

	-5		-6		-7		
SYM	MIN	MAX	MIN	MAX	MIN	MAX	UNITS
tRPC	5		5		5		ns
tRPS	90		105		125		ns
tWRH	8		10		10		ns
tWRP	8		10		10		ns

28-PIN PLASTIC SOJ (300 mil)

DA-3

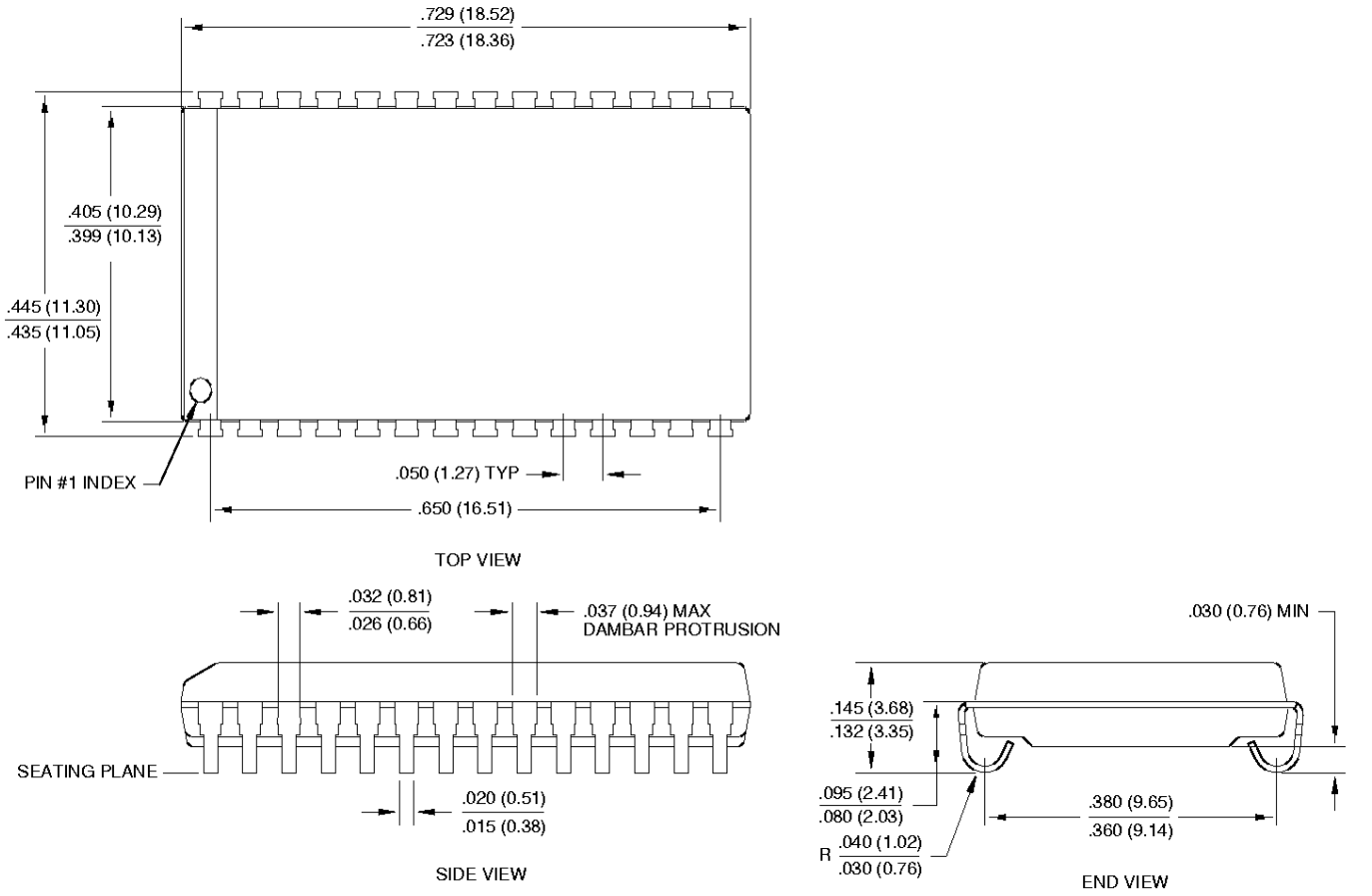


NOTE: 1. All dimensions in inches (millimeters) $\frac{\text{MAX}}{\text{MIN}}$ or typical where noted.

2. Package width and length do not include mold protrusion; allowable mold protrusion is .01" per side.

28-PIN PLASTIC SOJ (400 mil)

DA-4

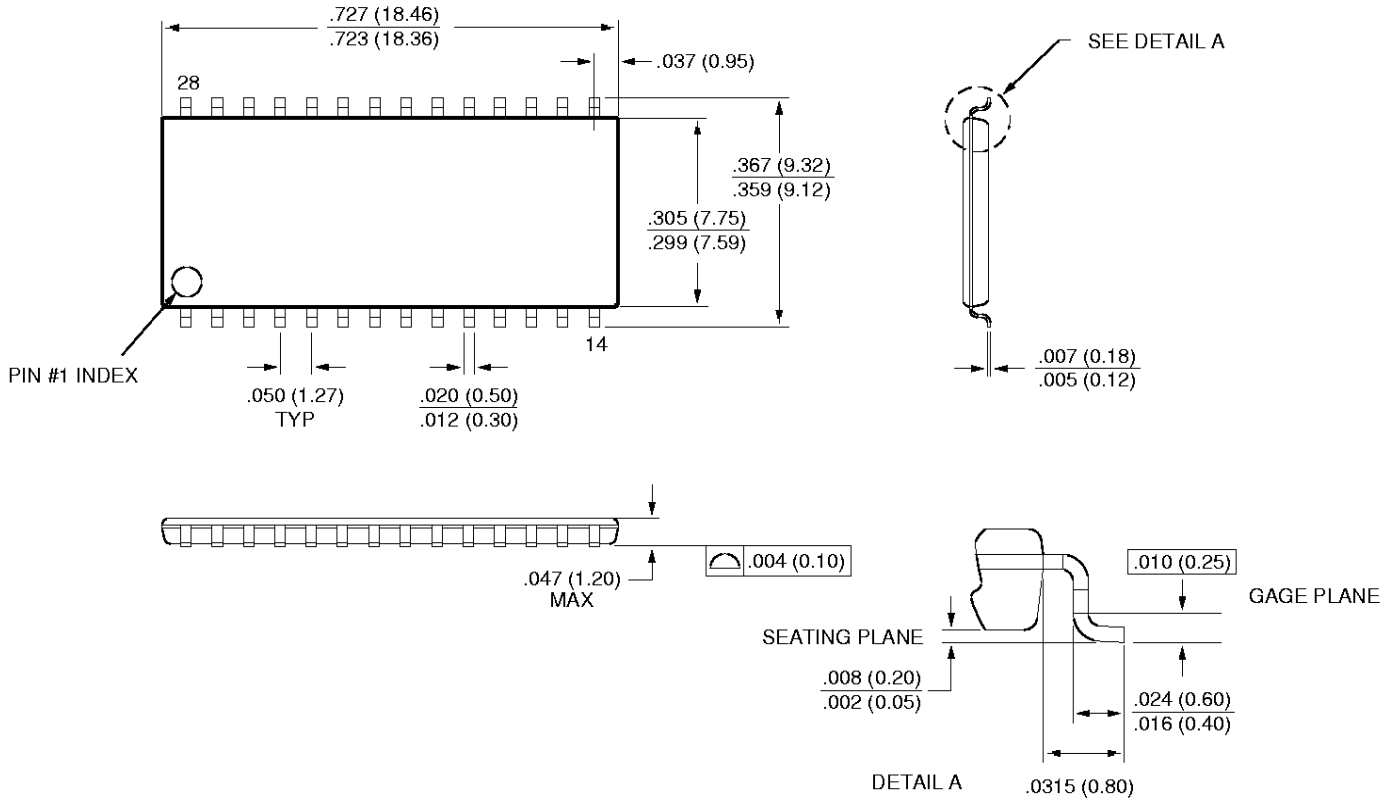


NOTE: 1. All dimensions in inches (millimeters) $\frac{\text{MAX}}{\text{MIN}}$ or typical where noted.

2. Package width and length do not include mold protrusion; allowable mold protrusion is .01" per side.

28-PIN PLASTIC TSOP (300 mil)

DB-3



NOTE: 1. All dimensions in inches (millimeters) $\frac{\text{MAX}}{\text{MIN}}$ or typical where noted.

2. Package width and length do not include mold protrusion; allowable mold protrusion is .01" per side.

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