FLASH AND CellularRAM™ COMBO MEMORY

MT28C128532W18/W30E
MT28C128564W18/W30E

Low Voltage, Wireless Temperature

Features

Stacked die Combo package
- Includes two 64Mb Flash devices
- Choice of either one 32Mb or one 64Mb CellularRAM™ device

Basic configuration

Flash
- Flexible multibank architecture
- 4 Meg x 16 Async/Page/Burst interface
- Support for true concurrent operations with no latency

CellularRAM
- Low-power, high-density design
- 2 Meg x 16 or 4 Meg x 16 configurations
- Burst

F_VCC, VCCQ, F_VPP, C_VCC voltages
- 1.70V (MIN)/1.95V (MAX) F_VCC, C_VCC
- 1.70V (MIN)/2.24V (MAX) VCCQ (W18)
- 2.20V (MIN)/3.30V (MAX) VCCQ (W30)
- 1.80V (TYP) F_VPP (in-system PROGRAM/ERASE)
- 12V ±5% (HV) F_VPP tolerant (factory programming compatibility)

Fast programming Algorithm (FPA)

Enhanced suspend options
- ERASE-SUSPEND-to-READ within same bank
- PROGRAM-SUSPEND-to-READ within same bank
- ERASE-SUSPEND-to-PROGRAM within same bank

Each Flash contains two 64-bit chip protection registers for security purposes

100,000 ERASE cycles per block

Cross-compatible command set support
- Extended command set
- Common Flash interface (CFI) compliant

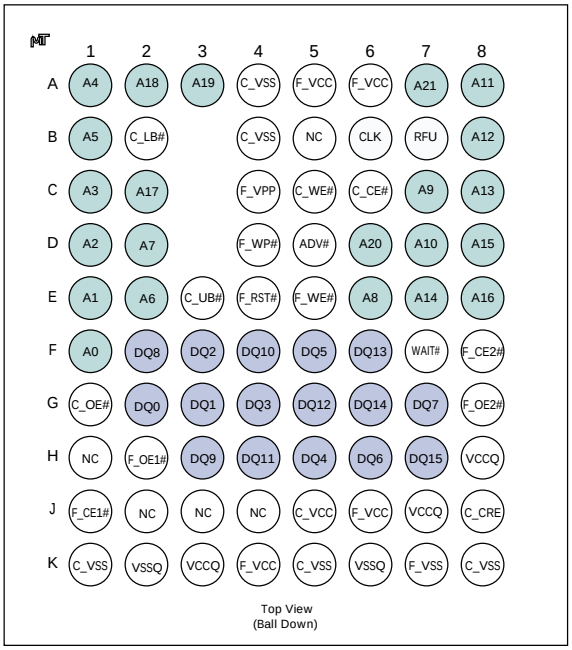
Manufacturer's Identification Code (ManID)
- Micron®
- Intel®

Options

Flash Timing
- 60ns[1] (W18)
- 70ns (W18/W30)

Flash Burst Frequency
- 66 MHz[1] (W18)
- 54 MHz (W18/W30)

Figure 1: 77-Ball FBGA



Flash Boot Block Configuration
- Top/Top
- Top/Bottom
- Bottom/Top
- Bottom/Bottom

CellularRAM Timing
- 70ns
- 85ns

CellularRAM Burst Frequency
- 66 MHz

I/O Voltage Range
- VccQ 1.70V–2.24V (W18)
- VccQ 2.20V–3.30V (W30)

Manufacturer's Identification Code (ManID)
- Micron (0x2Ch)
- Intel (0x89h)

Operating Temperature Range
- Wireless Temperature (-25°C to +85°C)

Package
- 77-ball FBGA (Standard) 8 x 10 grid
- 77-ball FBGA (Lead-free) 8 x 10 grid[2]

NOTE: 1. Contact factory for availability.
2. Contact factory for details.

Table of Contents

List of Figures

List of Tables

Device General Description

The MT28C128532W18/W30E/MT28C128564W18/W30E combination Flash and CellularRAM devices are a high-performance, high-density, memory solution that can significantly improve system performance. This memory solution is comprised of two 64Mb Flash devices and one 32Mb or one 64Mb CellularRAM device.

It is important to note that the specifications contained in this document supersede the specifications listed in the referenced individual Flash and CellularRAM data sheets.

Flash General Description

The Flash architecture features a multipartition configuration that supports READ-While-PROGRAM/ERASE operations with no latency. A 4Mb partition size enables optimal design flexibility.

Two Flash devices are stacked to achieve the 128Mb density. Each Flash die has a dedicated CE# and OE# control.

The stacked Flash device enables soft protection for blocks, as read only, by configuring soft protection registers with dedicated command sequences. For security purposes, two user-programmable 64-bit chip protection registers are provided for each Flash device.

The embedded WORD PROGRAM and BLOCK ERASE functions are fully automated by an on-chip write state machine (WSM). An on-chip device status register can be used to monitor the WSM status and determine the progress of the PROGRAM/ERASE tasks.

Each Flash device has a read configuration register (RCR) that defines how the Flash interacts with the memory bus. For device specifications and additional documentation concerning Flash features, please refer to the MT28F644W18 data sheet at www.micron.com/flash.

Flash Configurations

Each Flash memory implements a multibank architecture (16 banks of 4Mb each) to allow concurrent operations. Any address within a block address range selects that block for the required READ, PROGRAM, or ERASE operation.

Each Flash memory features eight 4K-word sectors (8 x 65,536 bits), designated as parameter blocks, and the remaining part is organized in main blocks of 32K words each (524,288 bits). The parameter blocks are addressed either by the low order addresses (bottom boot) or by the higher order addresses (top boot).

The two Flash devices can be supplied with any combination of top or bottom boot (e.g., top/top, bottom/bottom, top/bottom, or bottom/top).

CellularRAM General Description

The CellularRAM architecture features high-speed CMOS, dynamic random-access memories developed for low-power portable applications The CellularRAM device is available in either 32Mb or 64Mb densities.

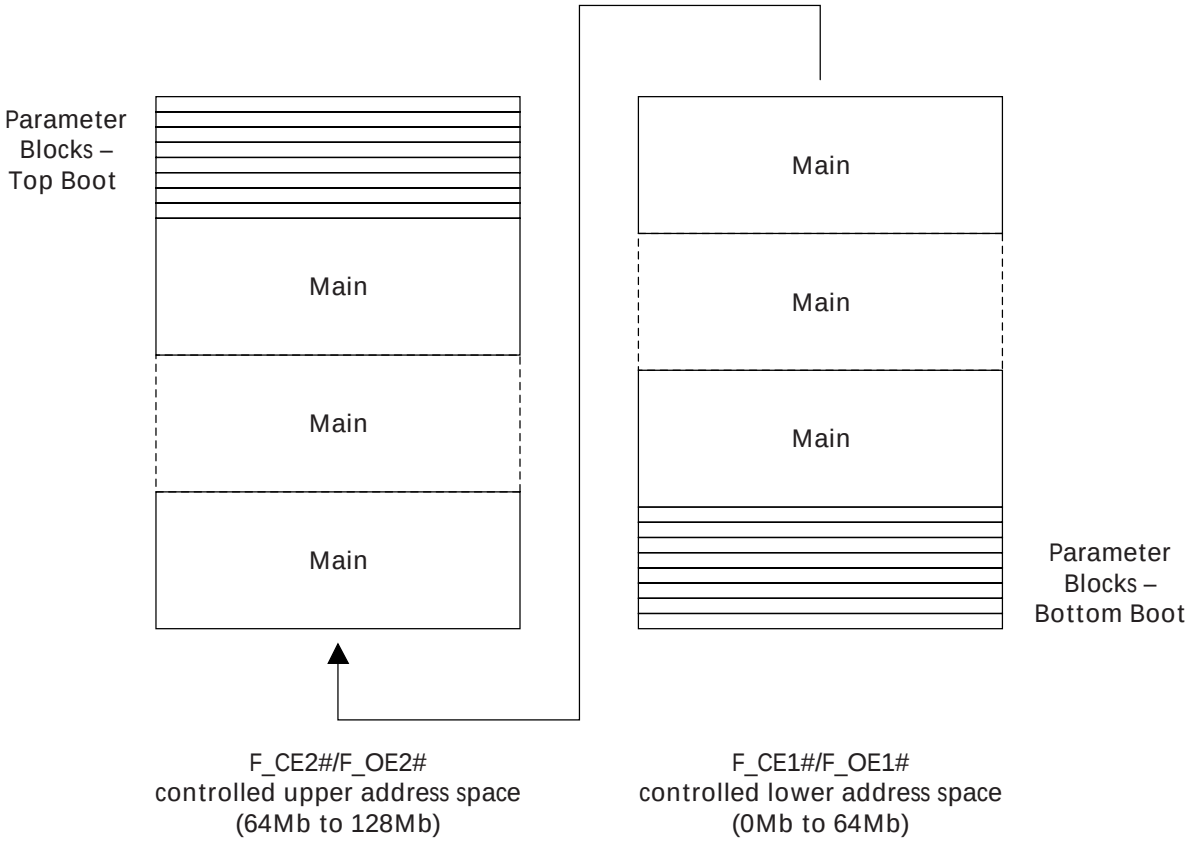
Two user-accessible control registers define the device operation. The bus configuration register (BCR) defines how the CellularRAM device interacts with the system memory bus and is nearly identical to its counterpart on burst mode Flash devices. The refresh configuration register (RCR) is used to control how refresh is performed on the CellularRAM array. These registers are automatically loaded with default settings during power-up and can be updated anytime during normal operation.

To operate seamlessly on a burst Flash bus, CellularRAM products have incorporated a transparent self-refresh mechanism. The hidden refresh requires no additional support from the system memory controller and has no significant impact on device read/write performance.

CellularRAM products include three system-accessible mechanisms used to minimize standby current. Partial array refresh (PAR) limits refresh to the portion of the memory array being used. Temperature compensated refresh (TCR) is used to adjust the refresh rate according to the ambient temperature. The refresh rate can be decreased at lower temperatures to minimize current consumption during standby. Deep sleep mode halts the refresh operation altogether and is used when no vital information is stored in the device. These three refresh mechanisms are adjusted through the refresh configuration register (RCR).

For device specifications and additional documentation concerning CellularRAM features, please refer to the MT45W2MW16BFB and MT45W4MW16BFB data sheets at www.micron.com/cellularram.

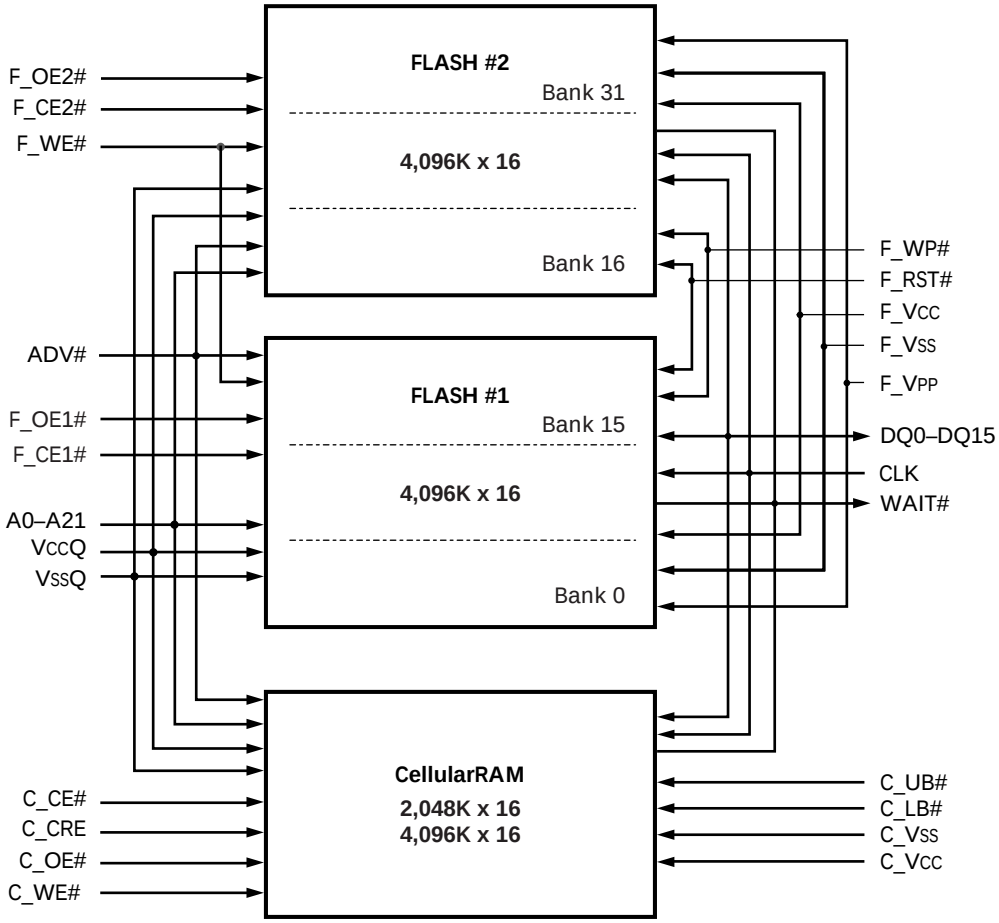
Figure 2: Flash Memory Map



NOTE:

Figure 2 shows a TB (top/bottom) dual Flash configuration.

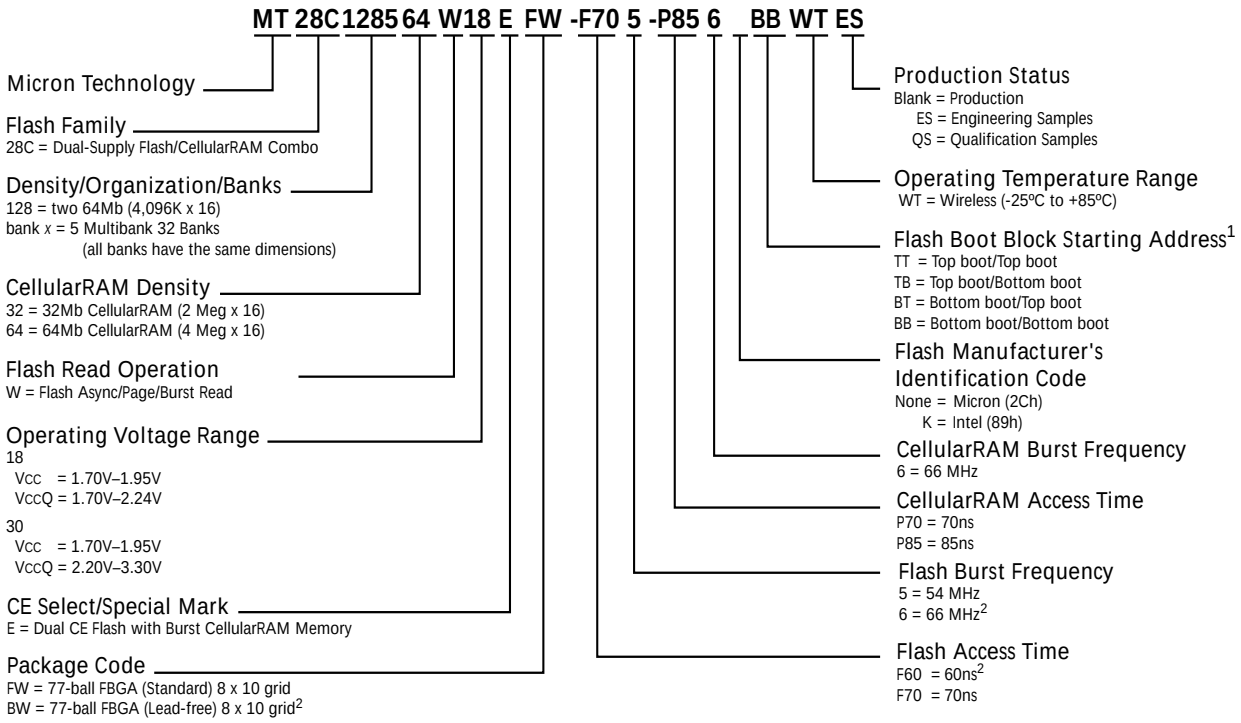
Figure 3: Block Diagram



Part Number Information

Micron's combination memory devices are available with several different combinations of features (see Figure 4).

Figure 4: Part Number Chart



NOTE:

1. The first character in this field refers to Flash die #2. The second character in this field refers to Flash die #1.
2. Contact factory for availability.

Valid Part Number Combinations

After building the part number from the part number chart above, please go to Micron's Part Marking Decoder Web site at www.micron.com/decoder to verify that the part number is offered and valid. If the device required is not on this list, please contact the factory.

Device Marking

Due to the size of the package, the Micron standard part number is not printed on the top of each device. Instead, an abbreviated device mark comprised of a five-digit alphanumeric code is used. The abbreviated device marks are cross-referenced to the Micron part numbers at www.micron.com/decoder. To view the location of the abbreviated mark on the device, please refer to customer service note CSN-11, "Product Mark/Label," at www.micron.com/csn.

Table 1: Ball Descriptions

77-BALL FBGA NUMBERS	SYMBOL	TYPE	DESCRIPTIONS
F1, E1, D1, C1, A1, B1, E2, D2, E6, C7, D7, A8, B8, C8, E7, D8, E8, C2, A2, A3, D6, A7	A0–A21	Input	Addresses: Flash: A0–A21 (128Mb). CellularRAM: A0–A21 (64Mb). CellularRAM: A0–A20 (32Mb).
J1	F_CE1#	Input	Flash Chip Enable #1.
F8	F_CE2#	Input	Flash Chip Enable #2.
H2	F_OE1#	Input	Flash Output Enable #1.
G8	F_OE2#	Input	Flash Output Enable #2.
E5	F_WE#	Input	Flash Write Enable.
D4	F_WP#	Input	Flash Write Protect.
E4	F_RST#	Input	Flash Reset.
B2	C_LB#	Input	CellularRAM Lower Byte Control.
E3	C_UB#	Input	CellularRAM Upper Byte Control.
C5	C_WE#	Input	CellularRAM Write Enable.
G1	C_OE#	Input	CellularRAM Output Enable.
C6	C_CE#	Input	CellularRAM Chip Enable.
J8	C_CRE	Input	CellularRAM Deep Sleep Mode and Configuration Mode.
D5	ADV#	Input	Address Valid (burst operation only).
B6	CLK	Input	Clock (burst operation only).
G2, G3, F3, G4, H5, F5, H6, G7, F2, H3, F4, H4, G5, F6, G6, H7	DQ0–DQ15	I/O	Flash/CellularRAM Data Input/Output.
F7	WAIT#	Output	WAIT#. See “WAIT Ball Operation” on page 10.
K7	F_V_{SS}	Supply	Flash Core Ground.
C4	F_V_{PP}	Supply	Flash V_{PP}.
A5, A6, J6, K4	F_V_{CC}	Supply	Flash Core Power Supply.
A4, B4, K1, K5, K8	C_V_{SS}	Supply	CellularRAM Core Ground.
J5	C_V_{CC}	Supply	CellularRAM Core Power Supply.
H8, J7, K3	$V_{CC}Q$	Supply	Flash/CellularRAM I/O Supply.
K2, K6	$V_{SS}Q$	Supply	Flash/CellularRAM I/O Ground.
B5, H1, J2, J3, J4	NC	–	No Connect. Not internally connected to the die.
B7	RFU	–	Reserved for Future Use (A22).
B3, C3, D3	–	–	Ball not Mounted. Reserved for Future Use (A23, A24, A25).

Boot Configurations

The possible configurations for Flash die are shown in Table 2 below. This table shows the possible configurations of the two Flash devices for either top boot or bottom boot: F_CE1# and F_CE2# indicate to which Flash die the configuration is referred.

Table 2: Possible Boot Configurations for Flash Die

CONFIGURATION	F_CE2#	F_CE1#	ORDER CODE
Top/Top	Top	Top	TT
Top/Bottom	Top	Bottom	TB
Bottom/Top	Bottom	Top	BT
Bottom/Bottom	Bottom	Bottom	BB

MultiChip Packaging Considerations

Multichip packaging presents unique challenges when controlling complex memory devices.

The MT28C128532W18/W30E and MT28C128564W18/W30E devices combine two Micron Flash devices with a single CellularRAM device.

Unique IDs, State Machines, and Registers

Each Flash device has a separate command state machine (CSM) and status register (SR) and read configuration register (RCR). The read configuration register (RCR) settings are separate and can be different for the upper and lower device. Each Flash device has its own OTP, CFI, and device code. Depending on the boot configuration of each Flash device, the OTP, CFI, and device code information may differ.

Both Flash devices will share the same ManID, either Micron (0x2Ch) or Intel (0x89h), which is defined by the part number.

The CellularRAM memory has a refresh configuration register (RCR) that defines how the device performs self refresh, and a bus configuration register (BCR) to define the interface configuration.

Command Codes

All Flash command codes are independent within each device. Care must be taken when crossing the array boundary between the upper and lower Flash and the CellularRAM memory to ensure that only one device is enabled at one time.

In a two-cycle command sequence such as word program (0x40/data), it is required that both commands be issued to the same device.

It is not recommended that simultaneous READ, simultaneous WRITE, or simultaneous ERASE operations occur on both Flash devices.

READ Operation

All READ operations are limited to the address boundaries of each device. A new READ operation must be started when crossing a device boundary.

Flash Reset

The reset control is shared by both Flash die. Bringing F_RST# control LOW will reset both the upper and lower device.

WAIT Ball Operation

It is important to note that the Flash and CellularRAM devices share the WAIT ball functionality and must be configured correctly for proper burst mode operation. The Flash and CellularRAM devices use different registers to configure the WAIT polarity and have opposite default values.

The WAIT ball polarity for the Flash device is configured by programming bit 10 in the read configuration register (RCR). The default is active LOW.

The WAIT ball polarity for the CellularRAM device is configured by programming bit 10 in the bus configuration register (BCR). The default is active HIGH.

Both the Flash and CellularRAM WAIT ball polarities must be set to the same active level for proper operation.

Power Consumption

Multiple chip packaging requires that power calculations consider the active operation of the upper and lower Flash as well as that of the CellularRAM device. Total power consumed will be the sum of the currents associated with the state of each device.

Table 3: Truth Table

MODES		FLASH SIGNALS						SHARED SIGNALS		CellularRAM SIGNALS					MEMORY OUTPUT	
		F_CE1#	F_CE2#	F_OE1#	F_OE2#	F_WE#	F_RST#	ADV#	WAIT#	C_CE#	C_CRE	C_OE#	C_UB/LB#	C_WE#	MEMORY BUS CONTROL	DQ0–DQ15
FLASH F_CE1#	Read	L	H	L	X	H	H	L	Active[1]	CellularRAM memory must be in High-Z					Flash	DOUT
	Write	L	H	H	X	L	H	X	Asserted						Flash	DIN
	Standby	H	X	X	X	X	H	X	High-Z	CellularRAMmemory any mode allowable					Other	High-Z
	Output Disable	L	X	H	X	H	H	X	Active[1]						Other	High-Z
	Reset	X	X	X	X	X	L	X	High-Z						None	High-Z
FLASH F_CE2#	Read	H	L	X	L	H	H	L	Active[1]	CellularRAM memory must be in High-Z					Flash	DOUT
	Write	H	L	X	H	L	H	X	Asserted						Flash	DIN
	Standby	X	H	X	X	X	H	X	High-Z	CellularRAM memory any mode allowable					Other	High-Z
	Output Disable	X	L	X	H	H	H	X	Active[1]						Other	High-Z
	Reset	X	X	X	X	X	L	X	High-Z						None	High-Z
CELLULARRAM MEMORY	Read	Flash must be in High-Z						L	Active[1]	L	L	L	L	H	Cellular RAM	DOUT
	Write							L	Active[1]	L	L	H	L	L	Cellular RAM	DIN
	Standby	Flash any mode allowable						X	X	H	L	X	X	X	Other	High-Z
	Output Disable							X	X	L	L	H	X	H	Other	High-Z
	Deep Sleep Mode							X	X	H	H	X	X	X	Other	High-Z

NOTE:

1. WAIT status is only valid for burst mode operation. WAIT should be ignored for all other operating modes.

Electrical Specifications

Table 4: Absolute Maximum Ratings

Note 1

PARAMETERS/CONDITIONS	MIN	MAX	UNITS	NOTES
Operating Temperature Range	-25	+85	°C	
Storage Temperature Range	-55	+125	°C	
Soldering Cycle		+260	°C	2

NOTE:

1. Stresses greater than those listed in Table 5 may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.
2. See technical note TN-00-15 for more information.

Table 5: Recommended Operating Conditions

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS
VCC Supply Voltage (F_VCC and C_VCC)	VCC	1.70	–	1.95	V
I/O Supply Voltage	VccQ (W18)	1.70	–	2.24	V
	VccQ (W30)	2.20		3.30	

Table 6: Capacitance

T_A = +25°C; f = 1 MHz

PARAMETER/CONDITION	SYMBOL	TYP	MAX	UNITS
Input Capacitance	CIN	13	17	pF
Output Capacitance	COUT	18	20	pF
Clock Capacitance	CCLK	22	23	pF

Table 7: DC Characteristics

It is important to note that the specifications contained in this document supersede the specifications listed in the referenced individual Flash and CellularRAM data sheets. All currents are in RMS unless otherwise noted.

PARAMETER	SYMBOL	W18/W30		UNITS	NOTES
		TYP	MAX		
V_{CC} Standby Current with 32Mb CellularRAM device with 64Mb CellularRAM device	I_{CCS}		 140 150	µA	4
V_{CC} Standby with CellularRAM device in deep power-down (DPD) mode with 32Mb CellularRAM device with 64Mb CellularRAM device	I_{SBZZ}	 60 60		µA	1, 4
V_{CC} Program Suspend Current with 32Mb CellularRAM device with 64Mb CellularRAM device	I_{CCWS}		 140 150	µA	2, 4
V_{CC} Erase Suspend Current with 32Mb CellularRAM device with 64Mb CellularRAM device	I_{CCES}		 140 150	µA	2, 4
V_{CC} Automatic Power Save Current with 32Mb CellularRAM device with 64Mb CellularRAM device	I_{CCAPS}		 140 150	µA	3, 4

NOTE:

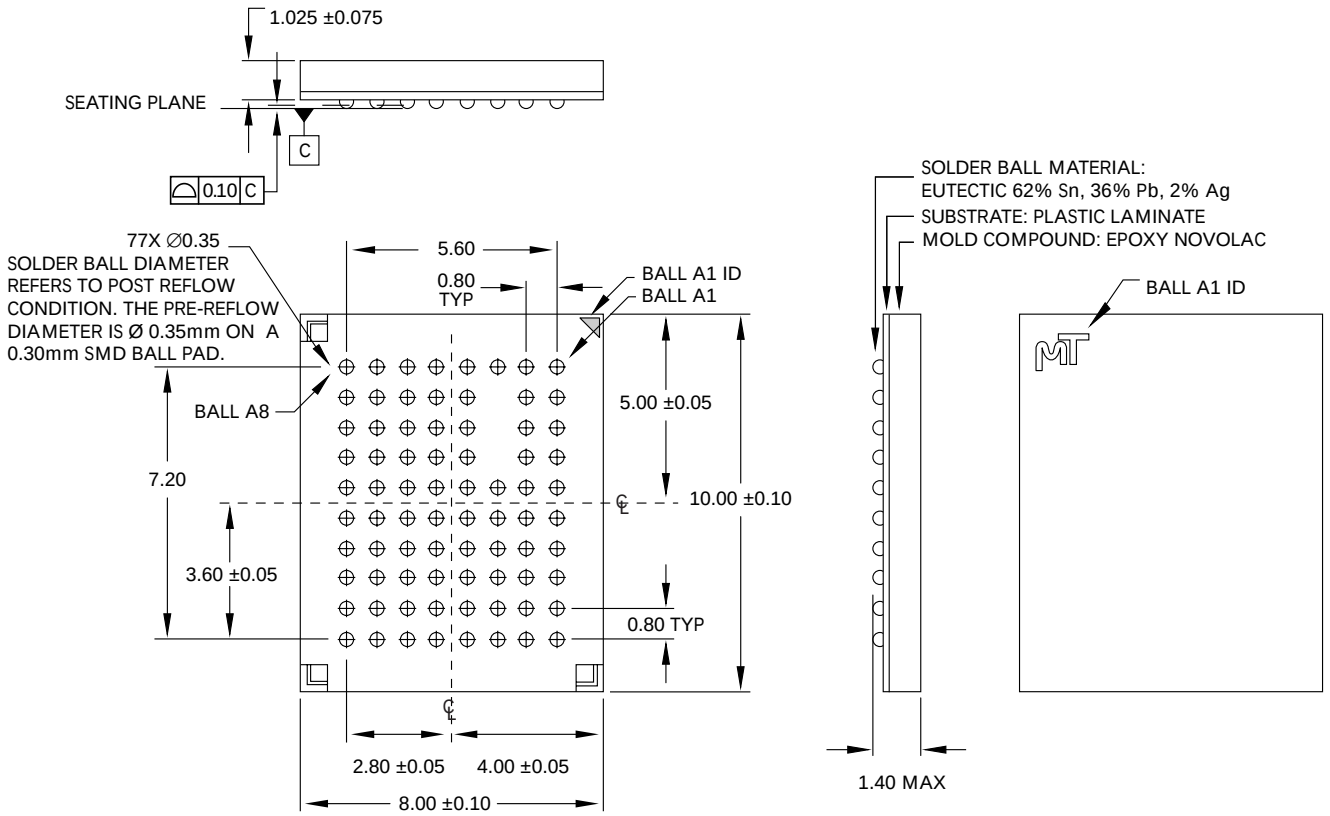
1. C_CRE ball HIGH, CR4 bit in the CellularRAM refresh configuration register set to zero. Measured at 25°C, this standby current is the sum of the Flash standby current and the CellularRAM deep-power down mode current.
2. I_{CCES} and I_{CCWS} values are valid when the device is deselected. Any READ operation performed while in suspend mode will have an additional current draw of suspend current.
3. Automatic power save (APS) mode reduces I_{CC} to approximately I_{CCS} levels.
4. Currents are measured using CellularRAM full array self-refresh. Currents may be further reduced by using the TCR or PAR features.

Table 8: CFI

It is important to note that the specifications contained in this document supersede the specifications listed in the referenced individual Flash and CellularRAM data sheets.

OFFSET	DATA	DESCRIPTION
78	32Mb: 0020	CellularRAM Density
	64Mb: 0040	

Figure 5: 77-Ball FBGA



NOTE:
1. All dimensions in millimeters.

Data Sheet Designation

Preliminary: This data sheet contains initial characterization limits that are subject to change upon full characterization of production devices.

For additional documentation concerning Flash and CellularRAM features, functional descriptions, programming, and timing, please refer to the table below.

Table 9: References

DEVICE	PART NUMBER	LINK
Flash	MT28F644W18/W30	www.micron.com/flash
CellularRAM	MT45W2MW16PFA and MT45W4MW16PFA	www.micron.com/cellularram

8000 S. Federal Way, P.O. Box 6, Boise, ID 83707-0006, Tel: 208-368-3900
E-mail: prodmktg@micron.com, Internet: http://www.micron.com, Customer Comment Line: 800-932-4992

Revision History

Rev B, Preliminary 11/03

Original document, Rev. A, Preview 8/03