SGS-THOMSON MICROELECTRONICS

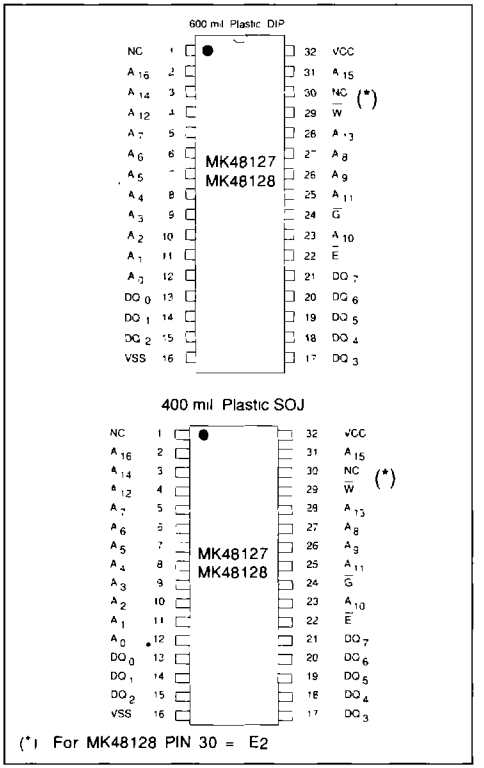
MK48127/128(N,X) -55/70/85

1 MEG (1,048,576-BIT) 128 K X 8 CMOS SRAM

ADVANCE DATA

- BYTEWYDE™ 128K X 8 CMOS SRAM
- EQUAL CYCLE/ACCESS TIMES, 55,70,85NS MAX.
- LOW V_{CC} DATA RETENTION 2 VOLTS
- THREE STATE OUTPUT
- JEDEC STANDARD 32-PIN PACKAGE IN 600 MIL PLASTIC DIP, 400 MIL PLASTIC SOJ

PIN CONNECTION



DESCRIPTION

The MK48127 is a Mega-bit (1,048,576-bit) CMOS SRAM, organized as 131,072 words x 8 bits. It is fabricated using SGS-Thomson's low power, high performance, CMOS technology. The device features fully static operation requiring no external clocks or timing strobes, with equal address access and cycle times. It requires a single +5V ± 10% supply, and all inputs and outputs are TTL compatible.

PIN NAMES

A_0-A_{16}	Address Inputs
DQ_0-DQ_7	Data I/O_{0-7}
$\overline{E}_1$	Chip Enable 1, Active Low
E_2 (*)	Chip Enable 2, Active High
$\overline{G}$	($\overline{OE}$) Output Enable
$\overline{W}$	Write/read Enable
V_{CC},V_{SS}	+5V, GND
NC	No Connection

NOTES :
(*) For MK48128 ONLY

MK48127/128 THRUTH TABLE

$\overline{W}$	$\overline{E}_1$	E_2(*)	$\overline{G}$	MODE	DQ	POWER
X	H	X	X	Deselect	Hi-Z	Standby
X	X	L	X	Deselect	Hi-Z	Standby
H	L	H	H	Read	Hi-Z	Active
H	L	H	L	Read	Q_{OUT}	Active
L	L	H	X	Write	D_{IN}	Active

NOTES :
(*) For MK48128 ONLY

READ MODE

The MK48127 is in the Read mode whenever Write Enable ($\overline{W}$) is high with Output Enable ($\overline{G}$) low, and Chip Enable ($\overline{E}$) is active low. This provides access to data from eight of 1,048,576 locations in the static memory array, specified by the 17 address inputs. Valid data will be available at the eight Output pins within t_{AVQV} after the last stable address, providing $\overline{G}$ is low, and $\overline{E}$ is low. If Chip Enable or Output Enable access times are not met, data access will be measured from the limiting parameter (t_{ELQV}, or t_{GLQV}) rather than the address. Data out may be indeterminate at t_{ELQX}, and t_{GLQX}, but data lines will always be valid at t_{AVQV}.

WRITE MODE

The MK48127 is in the Write mode whenever the $\overline{W}$ and $\overline{E}$ pins are low. Either Chip Enable or $\overline{W}$ must be inactive during Address transitions. The Write begins with the concurrence of Chip Enable being low with $\overline{W}$ low. Therefore, address setup times are referenced to Write Enable and Chip Enable as t_{AVWL}, and t_{AVEL} respectively, and is determined to the latter occuring edge. The Write cycle can be terminated by the earlier rising edge of $\overline{W}$ or Chip Enable ($\overline{E}$).

If the Output is enabled ($\overline{E}$ = low, $\overline{G}$ = low), then $\overline{W}$ will return the outputs to high impedance within t_{WLQZ} of its falling edge. Care must be taken to avoid bus contention in this type of operation. Data-in must be valid for t_{DVWH} to the rising edge of Write Enable, or to the rising edge of $\overline{E}$, whichever occurs first, and remain valid t_{WHDX}.

OPERATIONAL MODES

The MK48127 has a Chip Enable power down feature which sustains an automatic standby mode whenever Chip Enable ($\overline{E}$) goes inactive high. An Output Enable ($\overline{G}$) pin provides a high speed tristate control, allowing fast read/write cycles to be achieved with the common-I/O data bus. Operational modes are determined by device control inputs $\overline{W}$, $\overline{G}$, and $\overline{E}$, as summarized in the truth table.

MK48127/128 BLOCK DIAGRAM