FAST PAGE MODE DYNAMIC RAM 8M ×36 288M BIT

Type name		Max. Access time (ns)	Load memory	Outward dimensions W × H × D (mm)	Data sheet page
MH8M36AUJ-65	★	65	M5M417400ATP, RT ×8 + M5M44100BTP, RT ×4	107.95 × 41.6 × 7	3/13
MH8M36ANUJ-65	★				
MH8M36AUJ-75	★	75			
MH8M36ANUJ-75	★				
COMMON DATA					4/13

★ : New product

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MH8M36AUJ-65,-75/ MH8M36ANUJ-65,-75

FAST PAGE MODE 301989888-BIT (8388608-WORD BY 36-BIT) DYNAMIC RAM

DESCRIPTION

The MH8M36AUJ/ANUJ is 8388608-word × 36-bit dynamic RAM. This consists of sixteen industry standard 4M × 4 dynamic RAMs in TSOP, eight industry standard 4M × 1 dynamic RAMs in TSOP and two input buffers in SSOP.

The mounting of TSOP and SSOP on a single in-line package provides any application where high densities and large quantities of memory are required.

This is a socket-type memory module, suitable for easy interchange or addition of modules.

FEATURES

Type name	Access time (max. ns)	Cycle time (min. ns)	Power dissipation (typ. mW)
MH8M36AUJ/ANUJ-65	65	110	6760
MH8M36AUJ/ANUJ-75	75	130	6040

- Utilizes industry standard 4M × 4 RAMs in TSOP, industry standard 4M × 1 RAMs in TSOP and industry standard buffer in SSOP
- 72-pins single in-line package
- Single +5V (±10%) supply operation
- Low stand-by power dissipation
  924mW(max) ···························· CMOS input level
- Low operating power dissipation
  MH8M36AUJ/ANUJ-65 ····················· 8.40W(max)
  MH8M36AUJ/ANUJ-75 ····················· 7.41W(max)
- All inputs are directly TTL compatible
- All outputs are three-state and directly TTL compatible
- Includes (0.22μF × 24) decoupling capacitors
- 2048 refresh cycles every 32ms ($A_0 \sim A_{10}$)
- Fast-page mode capabilities
- The common I/O feature dicatates the use of only early write operation to prevent contention on Data-in and Data-out
- MH8M36AUJ is gold plating contact
  MH8M36ANUJ is solder with Nickel underplating contact

APPLICATION

Main memory unit for computers, Microcomputer memory, Refresh memory for CRT

PIN CONFIGURATION (TOP VIEW) (Both side)
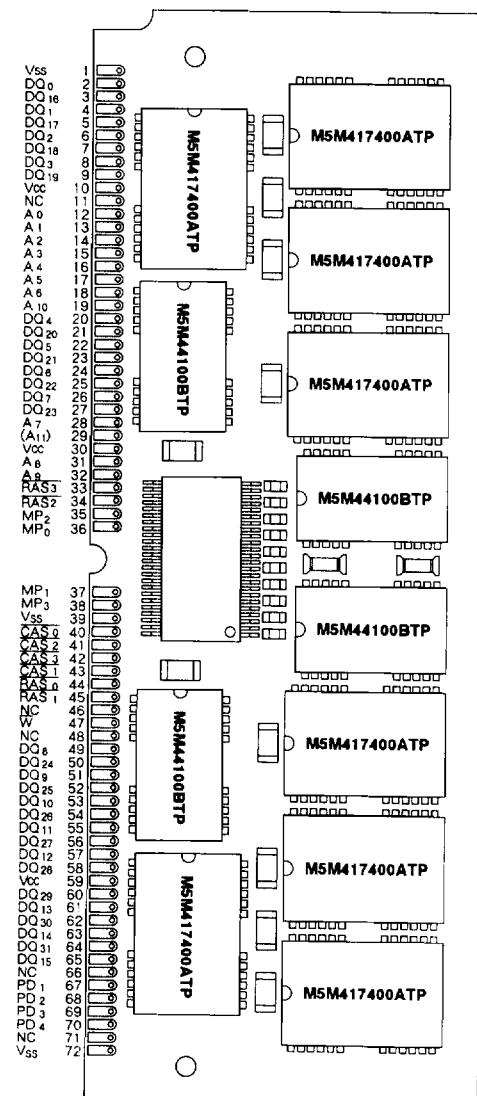
Outline 72N9S-B

	-65	-75
PD1	NC	NC
PD2	Vss	Vss
PD3	NC	Vss
PD4	NC	NC

NC : NO CONNECTION

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FUNCTION

In addition to normal read, and early write operations, a number of other functions, e.g., fast-page mode, $\overline{RAS}$-only refresh and $\overline{CAS}$ before $\overline{RAS}$ refresh. The input conditions for each are shown in Table 1.

Table 1 Input conditions for each mode

Operation	Inputs					Input/Output		Refresh	Remark
	$\overline{RAS}$	$\overline{CAS}$	$\overline{W}$	Row address	Column address	Input	Output		
Read	ACT	ACT	NAC	APD	APD	OPN	VLD	YES	
Write (Early write)	ACT	ACT	ACT	APD	APD	VLD	OPN	YES	Fast page mode identical
$\overline{RAS}$-only refresh	ACT	NAC	DNC	APD	DNC	DNC	OPN	YES	
Hidden refresh	ACT	ACT	DNC	APD	DNC	OPN	VLD	YES	
$\overline{CAS}$ before $\overline{RAS}$ refresh	ACT	ACT	NAC	DNC	DNC	DNC	OPN	YES	
Stand-by	NAC	DNC	DNC	DNC	DNC	DNC	OPN	NO	

Note. ACT : active, NAC : nonactive, DNC : don't care, VLD : valid, APD : applied, OPN : open

BLOCK DIAGRAM

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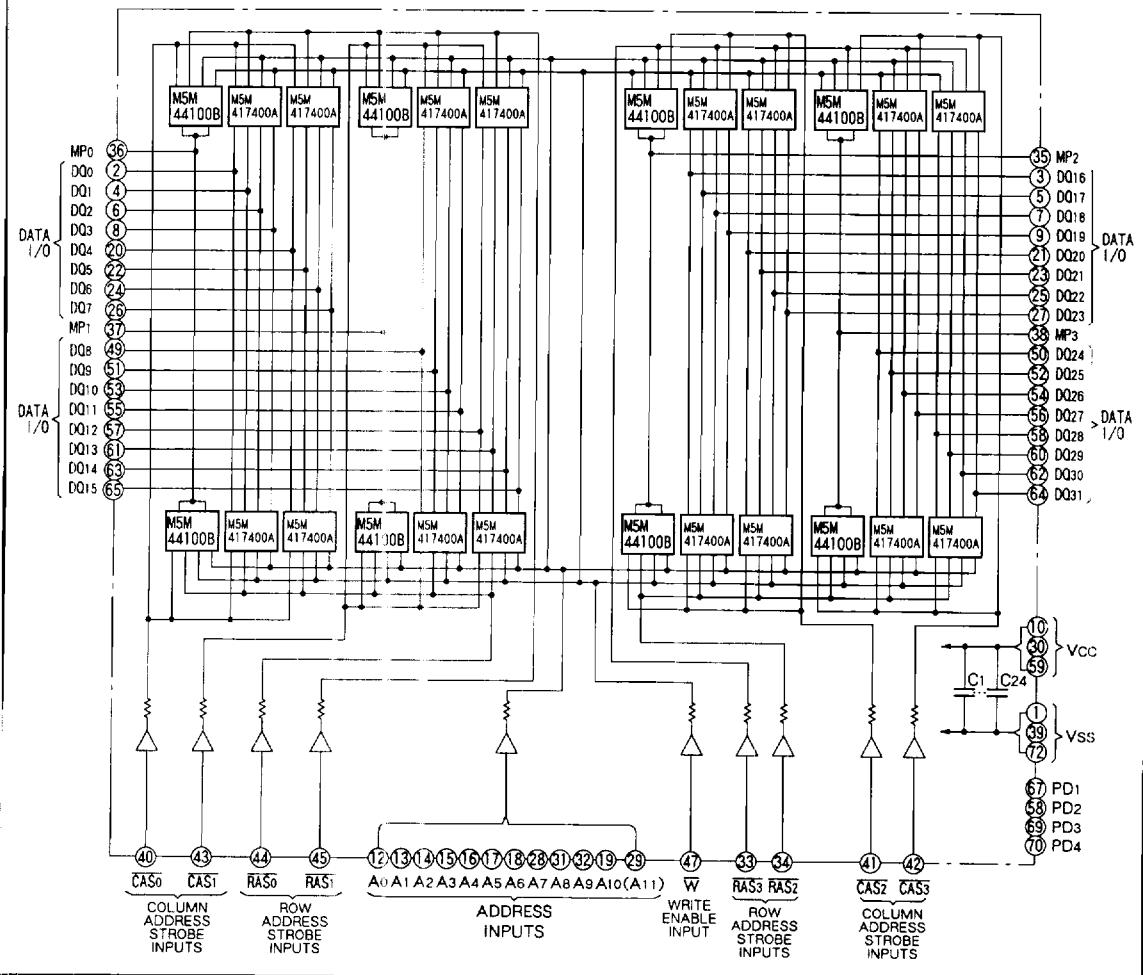
MH8M36AUJ
MH8M36ANUJ

FAST PAGE MODE 301989838-BIT

(8388608-WORD BY 36-BIT) DYNAMIC RAM

ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Conditions	Ratings	Unit
V_{cc}	Supply voltage	With respect to Vss	-0.5~7	V
V_I	Input voltage		-1~7	V
V_O	Output voltage		-1~7	V
I_O	Output current		50	mA
P_d	Power dissipation	$T_a = 25℃$	26	W
T_{opr}	Operating temperature		0~70	℃
T_{stg}	Storage temperature		-40~100	℃

RECOMMENDED OPERATING CONDITIONS (Ta = 0~70℃, unless otherwise noted) (Note 1)

Symbol	Parameter	Limits			Unit
		Min	Nom	Max	
V_{cc}	Supply voltage	4.5	5.0	5.5	V
V_{ss}	Supply voltage	0	0	0	V
V_{IH}	High-level Input voltage, all Inputs	2.4		6.0	V
V_{IL}	Low-level Input voltage, all Inputs	-1.0		0.8	V

Note 1. All voltage values are with respect to VSS

ELECTRICAL CHARACTERISTICS (Ta = 0~70℃, Vcc = 5V ± 10%, Vss = 0V, unless otherwise noted) (Note 2)

Symbol	Parameter		Test conditions	Limits			Unit
				Min	Typ	Max	
V_{OH}	High-level output voltage		$I_{OH} = -5mA$	2.4		Vcc	V
V_{OL}	Low-level output voltage		$I_{OL} = 4.2mA$	0		0.4	V
I_{OZ}	Off-state output current		Q floating $0V \leq V_{OUT} \leq 5.5V$	-20		20	μA
I_I	Input current		$0V \leq V_{IN} \leq 6.5V$, Other Input pins=0V	-1		1	μA
$I_{CC1(AV)}$	Average supply current from Vcc, operating (Note 3, 4)	MH8M36A-65	$\overline{RAS}$, $\overline{CAS}$ cycling $t_{RC} = t_{WC} = min.$ output open			1528	mA
		MH8M36A-75				1348	
$I_{CC2(AV)}$	Supply current from Vcc, stand-by		$\overline{RAS} = \overline{CAS} = V_{IH}$, output open			192	mA
			$\overline{RAS}=\overline{CAS} \geq Vcc-0.5V$, output open			168	
$I_{CC3(AV)}$	Average supply current from Vcc, refreshing (Note 3)	MH8M36A-65	$\overline{RAS}$ cycling, $\overline{CAS} = V_{IH}$ $t_{RC} = min.$ output open			1528	mA
		MH8M36A-75				1348	
$I_{CC4(AV)}$	Average supply current from Vcc Fast-Page-Mode (Note 3, 4)	MH8M36A-65	$\overline{RAS} = V_{IL}$, $\overline{CAS}$ cycling $t_{PC} = min.$ output open			1048	mA
		MH8M36A-75				912	
$I_{CC6(AV)}$	Average supply current from Vcc $\overline{CAS}$ before $\overline{RAS}$ refresh mode (Note 3)	MH8M36A-65	$\overline{CAS}$ before $\overline{RAS}$ refresh cycling $t_{RC} = min.$ output open			1528	mA
		MH8M36A-75				1164	

Note 2. Current flowing into an IC is positive, out is negative.
  3. ICC1(AV), ICC3(AV), ICC4(AV) and ICC6(AV) are dependent on cycle rate. Maximum current is measured at the fastest cycle rate.
  4. ICC1(AV) and ICC4(AV) are dependent on output loading. Specified values are obtained with the output open.

CAPACITANCE (Ta = 0~70℃, Vcc = 5V ± 10%, Vss = 0V, unless otherwise noted)

Symbol	Parameter	Test conditions	Limits			Unit
			Min	Typ	Max	
$C_{I(A)}$	Input capacitance, address inputs	$V_I = Vss$ $f = 1MHz$ $V_i = 25mVrms$			30	pF
$C_{I(DQ)}$	Data input/data output capacitance				30	pF
$C_{I(W)}$	Input capacitance, write control input				30	pF
$C_{I(\overline{RAS})}$	Input capacitance, $\overline{RAS}$ input				30	pF
$C_{I(\overline{CAS})}$	Input capacitance, $\overline{CAS}$ input				30	pF

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SWITCHING CHARACTERISTICS (Ta = 0~70°C, Vcc = 5V ± 10%, Vss = 0V, unless otherwise noted) (Notes 5, 12, 13)

Symbol	Parameter		MH8M36A-65 Min	MH8M36A-65 Max	MH8M36A-75 Min	MH8M36A-75 Max	Unit
tCAC	Access time from $\overline{CAS}$	(Note 6, 7)		20		25	ns
tRAC	Access time from $\overline{RAS}$	(Note 6, 8)		65		75	ns
tAA	Column address access time	(Note 6, 9)		35		40	ns
tCPA	Access time from $\overline{CAS}$ precharge	(Note 6, 10)		40		45	ns
tCLZ	Output low impedance time from $\overline{CAS}$ low	(Note 6)	5		5		ns
tOFF	Output disable time after $\overline{CAS}$ high	(Note 11)	0	20	0	25	ns

Note 5. An initial pause of 500μs is required after power-up followed by a minimum of eight initialization cycles (any combination of cycles containing a $\overline{RAS}$ clock such as $\overline{RAS}$-Only refresh).
Note the $\overline{RAS}$ may be cycled during the initial pause. And any 8 $\overline{RAS}$ or $\overline{RAS}/\overline{CAS}$ cycles are required after prolonged periods (greater than 32ms) of $\overline{RAS}$ inactivity before proper device operation is achieved.
6. Measured with a load circuit equivalent to 2TTL loads and 100pF.
7. Assumes that tRCD ≥ tRCD(max) and tASC ≥ tASC(max).
8. Assumes that tRCD ≤ tRCD(max) and tRAD ≤ tRAD(max). If tRCD or tRAD is greater than the maximum recommended value shown in this table, tRAC will increase by amount that tRCD or tRAD exceeds the value shown.
9. Assumes that tASC ≥ tRAD(max) and tASC ≤ tASC(max).
10. Assumes that tCP ≤ tCP(max) and tASC ≥ tASC(max).
11. tOFF(max) defines the time at which the output achieves the high impedance state (IOUT ≤ | ±20μA |) and is not reference to VOH(min) or VOL(max).

TIMING REQUIREMENTS (For Read, Early Write, Fast-Page Mode Cycles)
(Ta = 0~70°C, Vcc = 5V ± 10%, Vss = 0V, unless otherwise noted) (Notes 12, 13)

Symbol	Parameter		MH8M36A-65 Min	MH8M36A-65 Max	MH8M36A-75 Min	MH8M36A-75 Max	Unit
tREF	Refresh cycle time			32		32	ms
tRP	$\overline{RAS}$ high pulse width		40		50		ns
tRCD	Delay time, $\overline{RAS}$ low to $\overline{CAS}$ low	(Note 14)	20	45	20	50	ns
tCRP	Delay time, $\overline{CAS}$ high to $\overline{RAS}$ low		10		10		ns
tRPC	Delay time, $\overline{RAS}$ high to $\overline{CAS}$ low		0		0		ns
tCPN	$\overline{CAS}$ high pulse width		10		10		ns
tRAD	Column address delay time from $\overline{RAS}$ low	(Note 15)	15	30	15	35	ns
tASR	Row address setup time before $\overline{RAS}$ low		0		0		ns
tASC	Column address setup time before $\overline{CAS}$ low	(Note 16)	0	10	0	10	ns
tRAH	Row address hold time after $\overline{RAS}$ low		10		10		ns
tCAH	Column address hold time after $\overline{CAS}$ low		15		15		ns
tT	Transition time	(Note 17)	1	50	1	50	ns

Note 12. The timing requirements are assumed tT = 5ns.
13. VIH(min) and VIL(max) are reference levels for measuring timing of input signals.
14. tRCD(max) is specified as a reference point only. If tRCD is less than tRCD(max), access time is tRAC. If tRCD is greater than tRCD(max), access time is controlled exclusively by tCAC or tAA. tRCD(min) is specified as tRCD(min) = tRAH(min) + 2tT + tASC(min).
15. tRAD(max) is specified as a reference point only. If tRAD ≥ tRAD(max) and tASC ≤ tASC(max), access time is controlled exclusively by tAA.
16. tASC(max) is specified as a reference point only. If tRCD ≥ tRCD(max) and tASC ≥ tASC(max), access time is controlled exclusively by tCAC.
17. tT is measured between VIH(min) and VIL(max).

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Read and Refresh Cycles

Symbol	Parameter		Limits				Unit
			MH8M36A-65		MH8M36A-75		
			Min	Max	Min	Max	
tRC	Read cycle time		110		130		ns
tRAS	RAS low pulse width		60	10000	70	10000	ns
tCAS	CAS low pulse width		15	10000	20	10000	ns
tCSH	CAS hold time after RAS low		60		70		ns
tRSH	RAS hold time after CAS low		15		20		ns
tRCS	Read setup time before CAS low		0		0		ns
tRCH	Read hold time after CAS high	(Note 18)	0		0		ns
tRRH	Read hold time after RAS high	(Note 18)	10		10		ns
tRAL	Column address to RAS hold time		30		35		ns

Note 18. Either tRCH or tRRH must be satisfied for a read cycle.

Write Cycle (Early Write Cycles)

Symbol	Parameter		Limits				Unit
			MH8M36A-65		MH8M36A-75		
			Min	Max	Min	Max	
tWC	Write cycle time		110		130		ns
tRAS	RAS low pulse width		60	10000	70	10000	ns
tCAS	CAS low pulse width		15	10000	20	10000	ns
tCSH	CAS hold time after RAS low		60		70		ns
tRSH	RAS hold time after CAS low		15		20		ns
tWCS	Write setup time before CAS low	(Note 19)	0		0		ns
tWCH	Write hold time after CAS low		10		10		ns
tCWL	CAS hold time after W low		15		20		ns
tRWL	RAS hold time after W low		15		20		ns
tWP	Write pulse width		10		15		ns
tDS	Data setup time before CAS low or W low		0		0		ns
tDH	Data hold time after CAS low or W low		15		20		ns

Note 19. tWCS is specified as reference points only. If tWCS ≥ tWCS(min) the cycle is an early write cycle and the DQ pins will remain high impedance throughout the entire cycle.

Fast-Page Mode Cycle (Read, Early Write Cycle) (Note 20)

Symbol	Parameter		Limtis				Unit
			MH8M36A-65		MH8M36A-75		
			Min	Max	Min	Max	
tPC	Fast page mode read/write cycle time		40		45		ns
tRAS	RAS low pulse width for read write cycle	(Note 21)	100	125000	115	125000	ns
tCP	CAS high pulse width	(Note 22)	10	15	10	15	ns
tCPRH	RAS hold time after CAS precharge		35		40		ns

Note 20. All previously specified timing requirements and switching characteristics are applicable to their respective fast page mode cycle.
21. tRAS(min) is specified as two cycles of CAS input are performed.
22. tCP(max) is specified as a reference point only.

## CAS before RAS Refresh Cycle (Note 23)

Symbol	Parameter		Limits				Unit
			MH8M36A-65		MH8M36A-75		
			Min	Max	Min	Max	
tCSR	CAS setup time before RAS low		10		10		ns
tCHR	CAS hold time after RAS low		10		15		ns
tRSR	Read setup time before RAS low		10		10		ns
tRHR	Read hold time after RAS low		10		15		ns

Note 23. Eight to more CAS before RAS cycles instead of eight RAS cycles are necessary for proper operation of CAS before RAS refresh mode.

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Timing Diagrams (Note 24)
Read Cycle
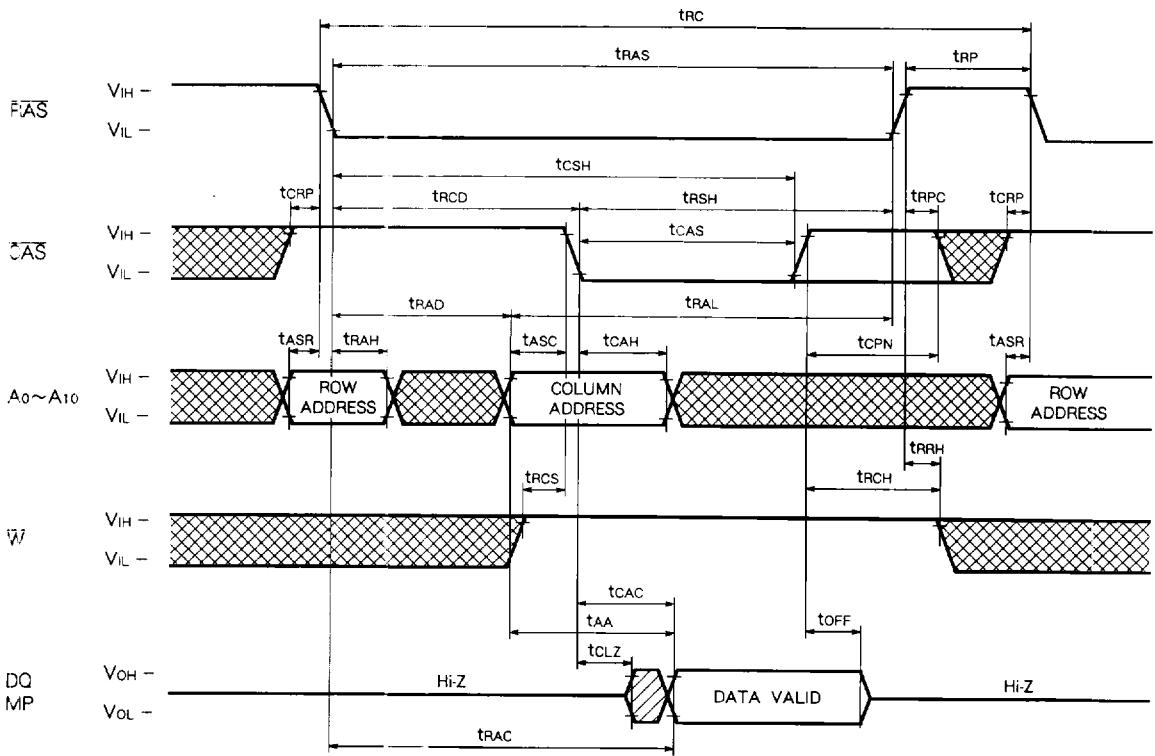
Note 24

Indicates the don't care input.
$V_{IH(min)} \leq V_{IN} \leq V_{IH(max)}$ or $V_{IL(min)} \leq V_{IN} \leq V_{IL(max)}$

Indicates the invalid output.

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Write Cycle (Early write)

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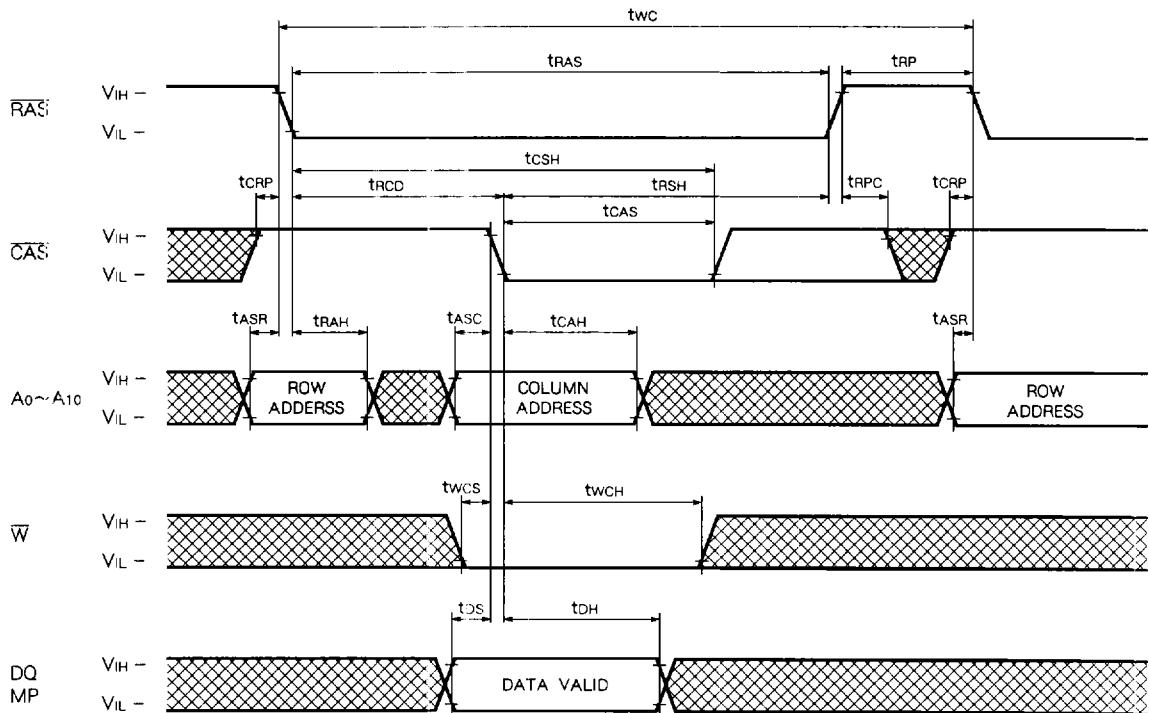
MH8M36AUJ
MH8M36ANUJ

**FAST PAGE MODE 301989888-BIT
(8388608-WORD BY 36-BIT) DYNAMIC RAM**

$\overline{\text{RAS}}$-only Refresh Cycle
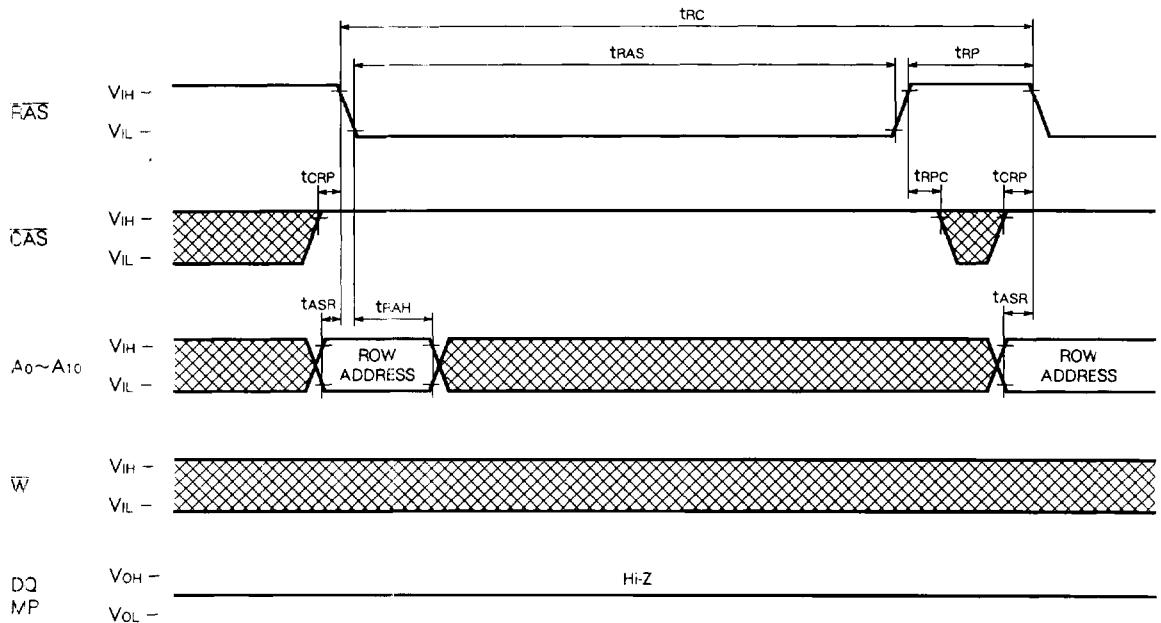
$\overline{\text{CAS}}$ before $\overline{\text{RAS}}$ Refresh Cycle
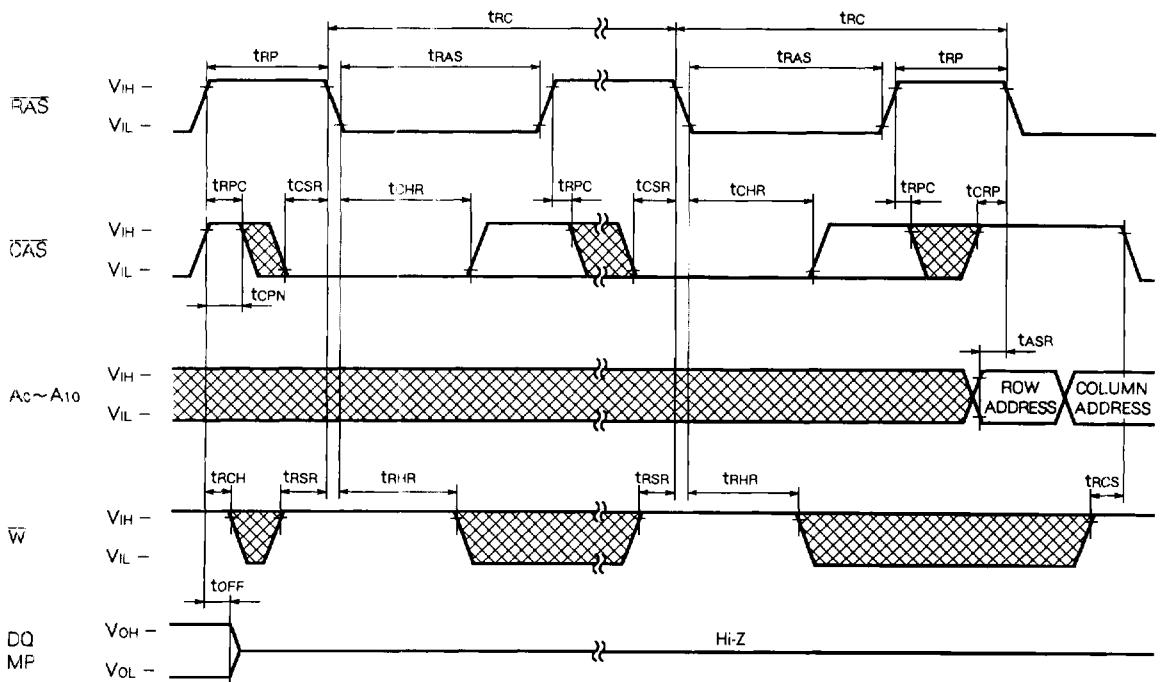
MITSUBISHI ELECTRIC

MH8M36AUJ
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**FAST PAGE MODE 301989888-BIT
(8388608-WORD BY 36-BIT) DYNAMIC RAM**

Fast Page Mode Read Cycle
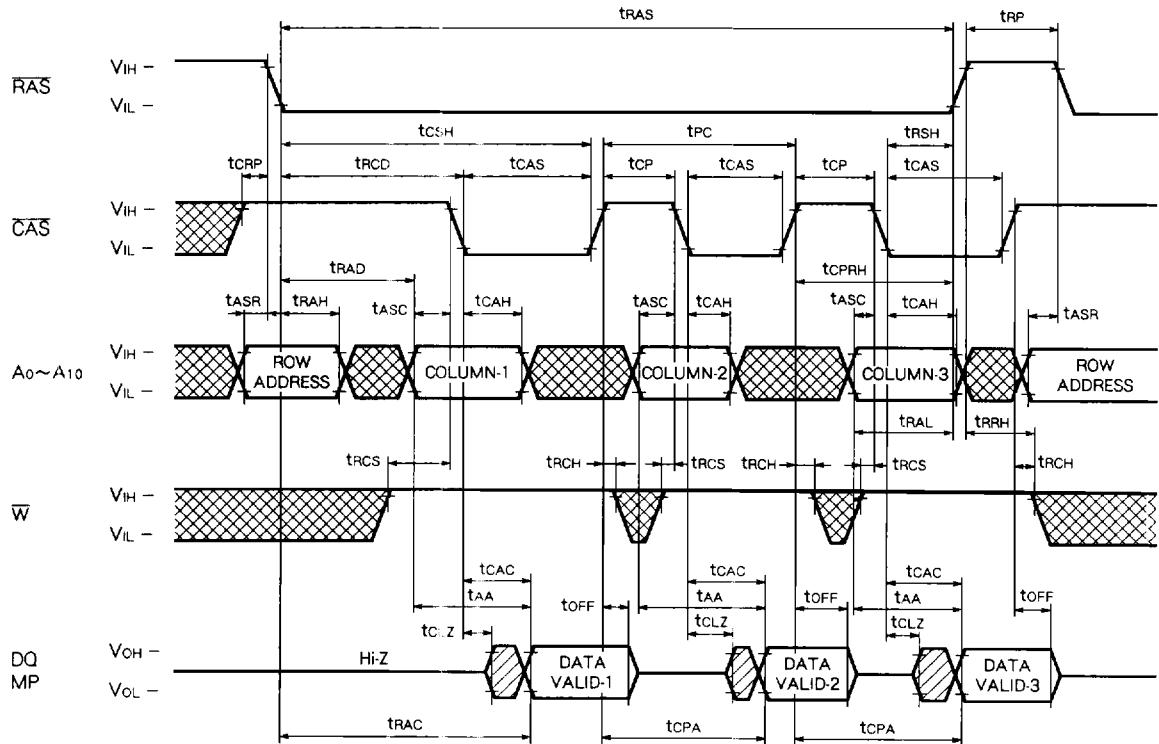
MH8M36AUJ
MH8M36ANUJ

FAST PAGE MODE 301989888-BIT
(8388608-WORD BY 36-BIT) DYNAMIC RAM

Fast-Page-Mode Write Cycle (Early Write)

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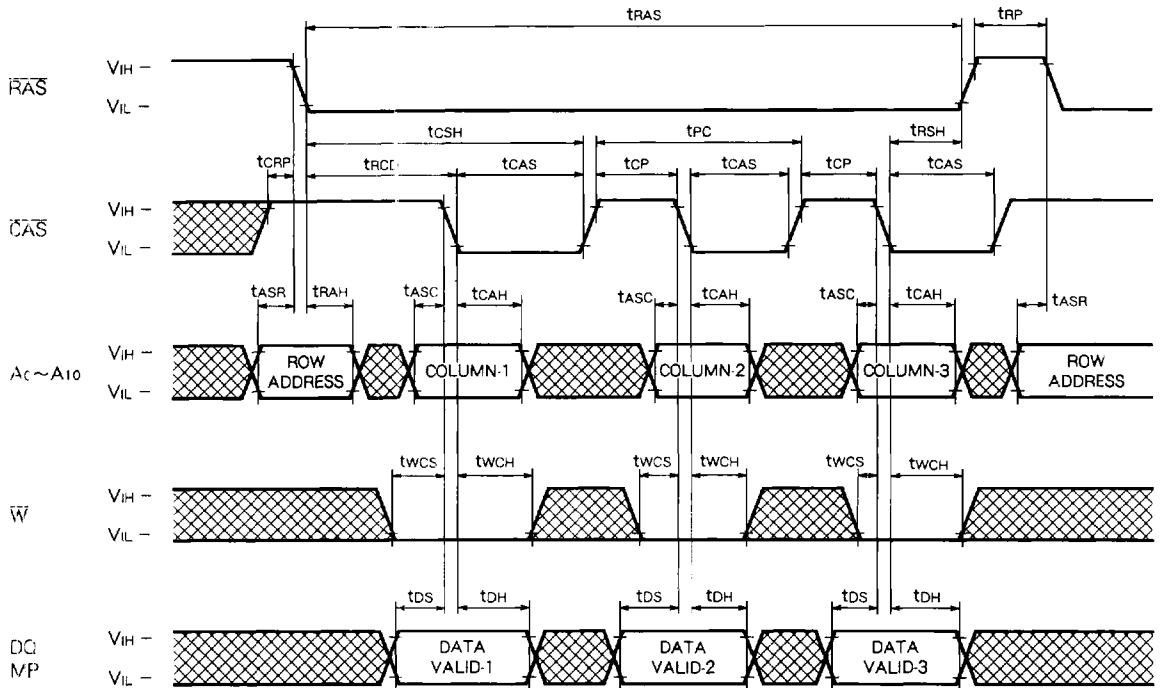
MH8M36AUJ
MH8M36ANUJ

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Hidden Refresh Cycle (Read)

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