MtronPTI

...when timing matters

Introduces

M210x Series
PECL/LVDS/CML Clock Oscillator

Featuring ***QiK Chip™*** Technology

Features:

- Superior Jitter Performance (comparable to SAW based)
- Frequencies from 150 MHz to 1.4 GHz
- Designed for a short 2 week cycle time

Applications:

- Telecommunications such as SONET / SDH / DWDM / FEC / SERDES / OC-3 thru OC-192
- Wireless base stations / WLAN / Gigabit Ethernet
- Avionic flight controls and military communications

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M210x Series

PECL/LVDS/CML Clock Oscillator – 3.3/2.5/1.8 Volt – 5x7/9x14 mm

Product Specifications

Product Features:

- **Superior** *Jitter Performance* **comparable to SAW-based products (0.30pS typical at 622.08 MHz)**
- *Frequencies* **from 150 MHz to 1.4 GHz**
- **Crystal resonator based product offering** *far better Stability* **than SAW (+/-20ppm)**
- **Designed for** *Short Cycle Time* **manufacturing (2 weeks or less)**
- **0.01 µF bypass capacitor from Vcc to ground built into** *both* **5x7 and 9x14 packages**

Description:

The M210x Series oscillators are high performance PECL, LVDS, or CML output oscillators featuring exceptional performance while addressing the demands for shortened manufacturing cycle times.

Applications:

- **Telecommunications such as SONET / SDH / DWDM / FEC / SERDES / OC-3 thru OC-192**
- **Wireless base stations / WLAN / Gigabit Ethernet**
- **Avionic flight controls and military communications**
- **Test Equipment and Instrumentation**

Ordering Information:

Part Number Example: **M210 0 6 8 B P N 622.080000MHz**

0	6	8	B	P	N	622.080000 MHz
Supply Voltage	Operating Temperature	Stability	Enable/Disable	Logic Type	Package/Lead Configuration	Frequency
0 3.3 V 1 2.5 V 2 1.8 V	2 -40°C to +85°C 6 -20°C to +70°C	4 ±50ppm 6 ±25 ppm 8 ±20ppm	B Enable High (pin 1) G Enable High (pin 2) S Enable Low (pin 1) M Enable Low (pin 2) U No Enable/Disable	P PECL L LVDS M CML	N 5x7 mm Leadless J 9x14 mm J-Lead	150 – 1400 MHz

Part Number Example: M210068BPN – 622.080000 MHz

Applications Note:

The MtronPTI M210x series of clock oscillators, featuring *QiK Chip™* technology, provides for extremely low jitter of 0.30 ps RMS. For applications requiring low jitter, frequencies from 150 MHz to 1.4 GHz are available. LVPECL, LVDS, or CML compatible outputs, as well as operating voltage of 1.8 V, 2.5 V, and 3.3 V are also options on the M210x.

The M210x is available at a stability of ± 20 ppm, all-inclusive, over the industrial operating temperature range of -40°C to +85°C. By providing this specification, the M210x will perform at a much superior level than SAW based oscillator designs (Figure 1). This level of performance is achieved by utilizing a precision AT-cut crystal. An enable/disable function is also an available option on the M210x. The internal 0.01 µF by-pass capacitor also assures optimum noise suppression on the supply voltage pad.

The superior integrated jitter performance of 0.3 pS RMS makes the M210x suitable for 10 Gig-E, broadband networks, network switches, SONET, SDH, SERDES, DWDM, FEC, WLAN, and OC-3 thru OC-192 systems. The M210x is available in a nine-pad, 5x7x1.9 mm, leadless, ceramic, surface mount package (see page 4) that is RoHS and 260°C reflow compatible. (No PCB traces should be located directly under the 5x7 product). A six-J-lead, 9x14 mm, ceramic, surface mount package, that is RoHS and 260°C reflow compatible, is also available (see page 4). Figures 2 and 3 below show load termination conditions for LVPECL and LVDS. The M210x oscillators offer a pin 1 tristate for backward compatibility to many of the existing products in the industry from Vectron, Epson, and others.

For superior performance in a high frequency clock oscillator, the M210x is a logical choice for designers. The unique design architecture allows the M210x fast turn around on engineering design samples, as well as production quantities in 2 weeks or less.

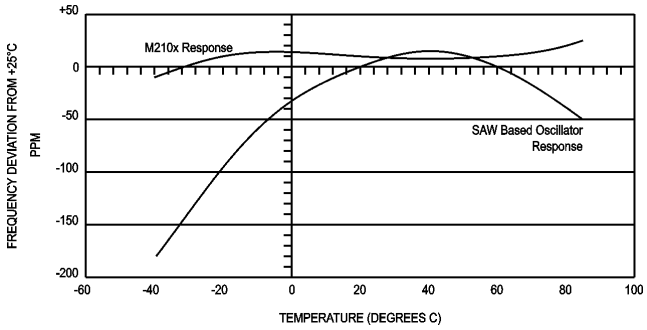


Figure 1. Frequency/Temperature Curves, M210x vs. SAW Based Oscillator Devices

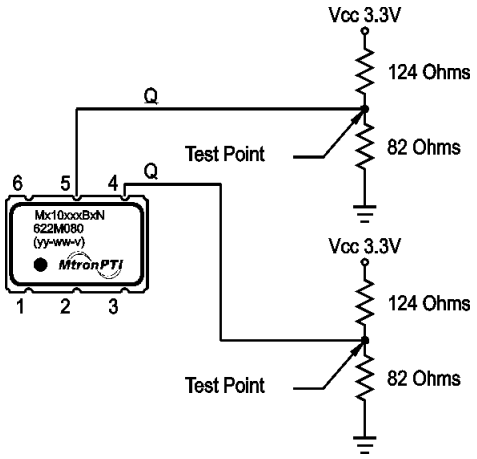


Figure 2. 3.3V LVPECL Load Circuit

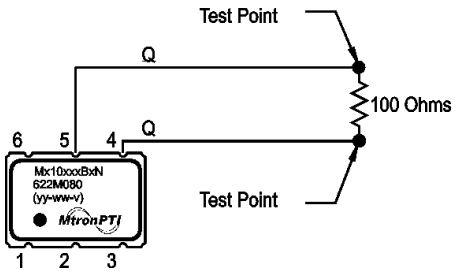


Figure 3. LVDS Load Circuit

Performance Characteristics:

Electrical Specifications	PARAMETER	Symbol	Min.	Typ.	Max.	Units	Condition/Notes
	Frequency Range	F	150		1400	MHz	Note 1
	Operating Temperature	T_A	(See ordering information)				
	Storage Temperature	T_S	-55		+125	°C	
	Frequency Stability	ΔF/F	(See ordering information)				See Note 2
	Aging						
	1st Year		-3		+3	ppm	
	Thereafter (per year)		-1		+1	ppm	
	Supply Voltage	Vcc	1.71	1.8	1.89	V	
			2.375	2.5	2.625	V	
			3.135	3.3	3.465	V	
	Input Current	Icc			125	mA	PECL/LVDS/CML
	Load		50 Ohms to (Vcc -2) Vdc 100 Ohm differential load				See Note 3 PECL Waveform LVDS/CML Waveform
	Symmetry (Duty Cycle)		45		55	%	@ 50% of waveform
	Output Skew			TBD			
	Differential Voltage		350	425 TBD	500	mVppd	LVDS CML
	Common Mode Output Voltage	Vcm		1.2		V	LVDS
	Logic "1" Level	Voh	Vcc -1.02			V	LVPECL
	Logic "0" Level	Vol			Vcc -1.63	V	LVPECL
	Rise/Fall Time	Tr/Tf		0.23	0.35	ns	@ 20/80% LVPECL
	Enable Function		80% Vcc min. or N/C: output active 20% Vcc max.: output disables to high-Z				Output Option B or G
			20% Vcc max: output active 80% Vcc min.: output disables to high-Z				Output Option S or M
	Start up Time			10		ms	
	Phase Jitter @ 622.08 MHz	ϕJ		0.3		ps RMS	Integrated 12 kHz – 20 MHz
	Phase Noise 10 Hz 100 Hz 1 KHz 10 KHz 100 KHz 1 MHz 10 MHz 40 MHz			 -50 -80 -106 -117 -120 -130 -147 -150			@ 622.08 MHz dBc/Hz dBc/Hz dBc/Hz dBc/Hz dBc/Hz dBc/Hz dBc/Hz dBc/Hz

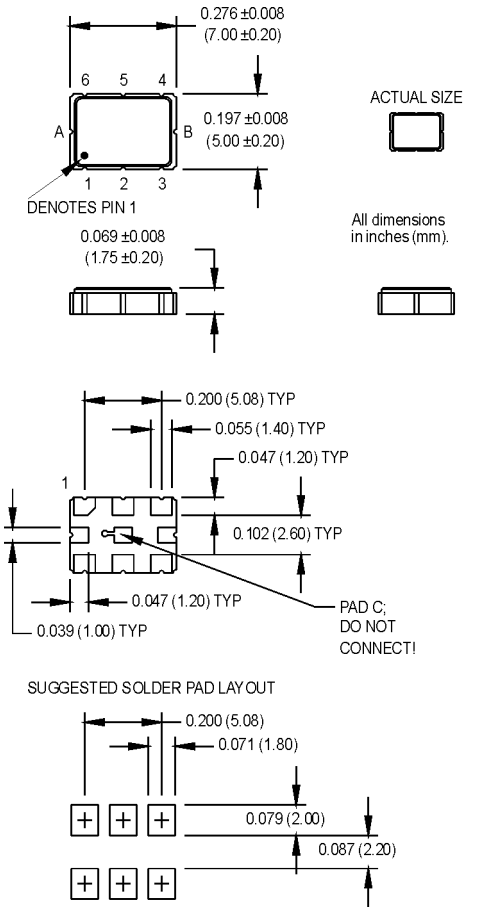
Note 1: Contact factory for exact frequency availability over 945 MHz

Note 2: Stability is inclusive of initial tolerance, deviation over temperature, shock, vibration, supply voltage, and aging for one year at 50°C mean ambient temperature.

Note 3: See Load Circuit Diagram in this Datasheet. Consult factory with nonstandard output load requirements.

Product Dimensions & Pinout Information:

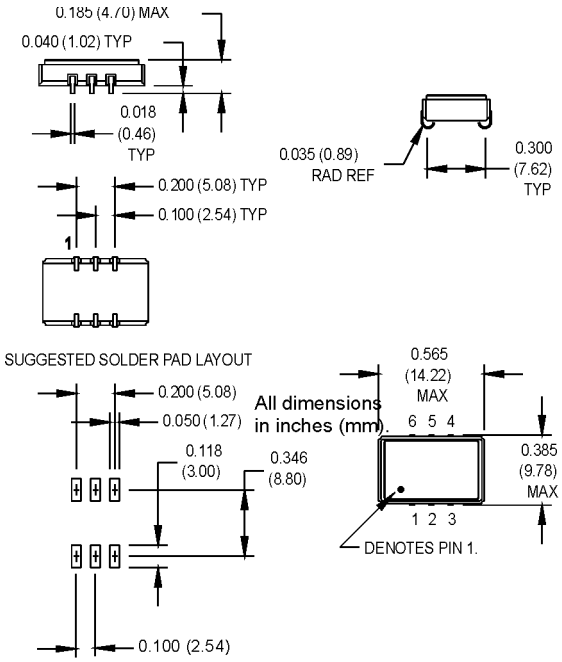
5x7 mm (N) Package



PIN 1 ENABLE
Pad1: Enable/Disable
Pad2: N/C
Pad3: Ground
Pad4: Output Q (PECL,LVDS,CML)
Pad5: Output $\overline{Q}$ (PECL,LVDS,CML)
Pad6: Vcc
PadA: Do not connect!
PadB: Do not connect!
PadC: Do not connect!

PIN 2 ENABLE
Pad1: N/C
Pad2: Enable/Disable
Pad3: Ground
Pad4: Output Q (PECL,LVDS,CML)
Pad5: Output $\overline{Q}$ (PECL,LVDS,CML)
Pad6: Vcc
PadA: Do not connect!
PadB: Do not connect!
PadC: Do not connect!

9x14 mm (J) Package



PIN 1 ENABLE
Pin1: Enable/Disable
Pin2: N/C
Pin3: Ground
Pin4: Output Q (PECL,LVDS,CML)
Pin5: Output $\overline{Q}$ (PECL,LVDS,CML)
Pin6: Vcc

PIN 2 ENABLE
Pin1: N/C
Pin2: Enable/Disable
Pin3: Ground
Pin4: Output Q (PECL,LVDS,CML)
Pin5: Output $\overline{Q}$ (PECL,LVDS,CML)
Pin6: Vcc

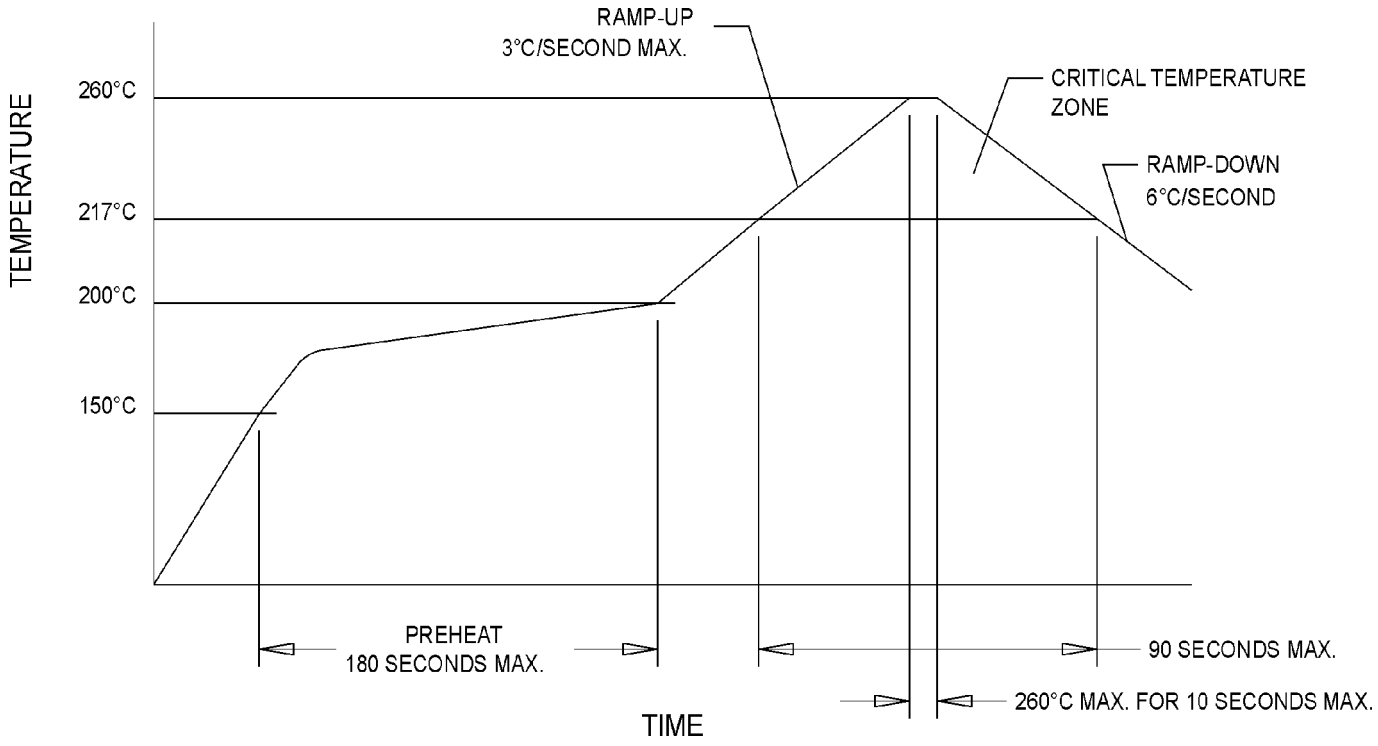
Handling Information:

Although protection circuitry has been designed into the M210x oscillator, proper precautions should be taken to avoid exposure to electrostatic discharge (ESD) during handling and mounting. MtronPTI utilizes a human-body model (HBM) and a charged-device model (CDM) for ESD-susceptibility testing and protection design evaluation. ESD voltage thresholds are dependent on the circuit parameters used to define the mode. Although no industry-wide standard has been adopted for the CDM, a standard HBM (resistance = 1500 Ω, capacitance = 100 pF) is widely used and therefore can be used for comparison purposes. The HBM ESD threshold presented here was obtained using these circuit parameters.

Model	ESD Threshold, Minimum	Unit
Human Body	1500*	V
Charged Device	1500*	V

* MIL-STD-833D, Method 3015, Class 1

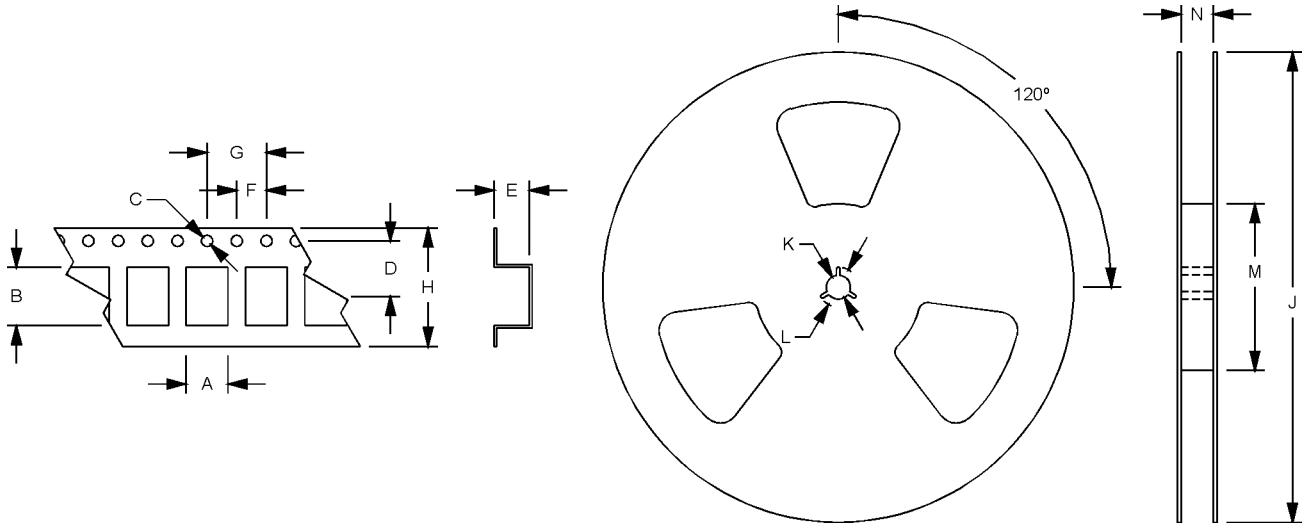
Solder Profile:



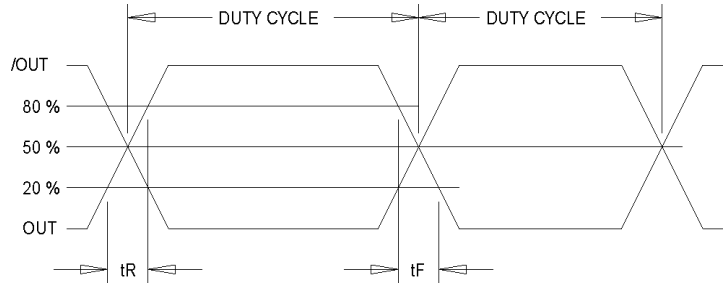
Quality Parameters:

Environmental Specifications/Qualification Testing Performed on the M210 Clock Oscillator		
Test	**Test Method**	**Test Condition**
Electrical Characteristics	Internal Specification	Per Specification
Frequency vs. Temperature	Internal Specification	Per Specification
Mechanical Shock	MIL-STD-202, Method 213, C	100 g's
Vibration	MIL-STD-202, Method 201-204	10 g's from 10-2000 Hz
Thermal Cycle	MIL-STD-883, Method 1010, B	-55 Deg. C to +125 Deg. C, 15 minute Dwell, 10 cycles
Aging	Internal Specification	168 Hours at 105 Degrees C
Gross Leak	MIL-STD-202, Method 112	30 Second Immersion
Fine Leak	MIL-STD-202, Method 112	Must meet $1x10^{-8}$
Solderability	MIL-STD-883, Method 2003	8 Hour Steam Age – Must Exhibit 95% coverage
Resistance to Solvents	MIL-STD-883, Method 2015	Three 1 minute soaks
Terminal Pull	MIL-STD-883, Method 2004, A	2 Pounds
Lead Bend	MIL-STD-883, Method 2004, B1	1 Bending Cycle
Physical Dimensions	MIL-STD-883, Method 2016	Per Specification
Internal Visual	Internal Specification	Per Internal Specification

Tape and Reel Specifications:



Product	A	B	C	D	E	F	G	H	I	J	K	L
M210x	6.51	9.29	1.5	7.5	2.8	4	8/12	16	180-330	13	21	60-100



Output Waveform: LVDS/CML/PECL

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