8Kx9 Static RAM CMOS, High Speed Monolithic

The EDI8908CA/LPA/PA is a high performance, low power, 65,536bit CMOS Static RAM organized as 8Kx9.

In addition to 13 address inputs, and 9 common data inputs and outputs, the device contains 4 control lines. The $\overline{E}$ and S lines perform chip enable functions and automatically power down the device when proper logic levels are applied. The $\overline{G}$ and $\overline{W}$ lines facilitate read and write operations.

The EDI8908CA/LPA/PA is available in standard power (CA), low power (PA) and low power with data retention (LPA) versions.

All inputs and outputs are TTL compatible and operate from a single 5V supply.

Military product compliant to MIL-STD-883, paragraph 1.2.1 is available.

Features

64K bit CMOS Static Random Access Memory

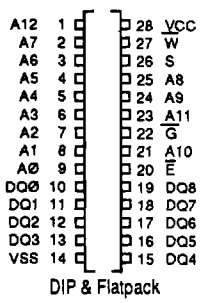
- Access Times 35, 45, 55, and 70ns
- $\overline{E}$, S, and $\overline{G}$ Functions for Bus Control
- Data Retention Function
- Military Low Power Operation (LP & LPA)
- Data Retention for Battery Back-up (LPA)
- Inputs and Outputs Directly TTL Compatible

Jedec Approved Pinouts

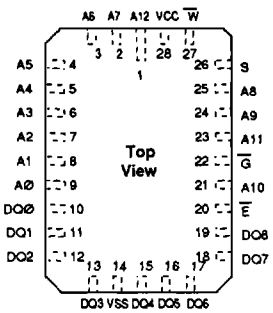
- 28 Pin Ceramic Dual-in-line Packages 300 mils Wide, No. 2
- 28 Lead Flatpack, No. 79
- 28 Pad Ceramic LCC, No. 14 (Non-Jedec)

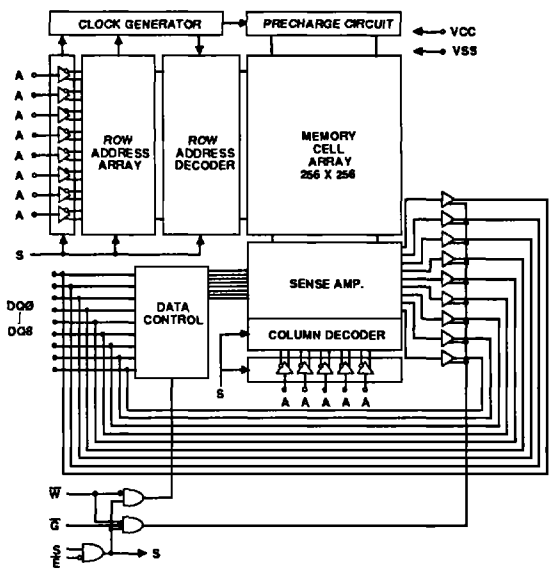
Single +5V (±10%) Supply Operation

Pin Configurations and Block Diagram



DIP & Flatpack





Pin Names

AØ-A12	Address Inputs
$\overline{E}$	Chip Enable
S	Chip Select
$\overline{W}$	Write Enable
$\overline{G}$	Output Enable
DQØ-DQ8	Data Input / Output
VCC	Power (+5V±10%)
VSS	Ground
NC	No Connection

Absolute Maximum Ratings*

Voltage on any pin relative to VSS ..... -0.5V to 7.0V
Operating Temperature TA (Ambient)
Military ..... -55°C to +125°C
Storage Temperature,Ceramic ..... -65°C to +150°C
Power Dissipation ..... 1 Watt
Output Current ..... 20 mA
Junction Temperature, TJ ..... 175°C

*Stress greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions greater than those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

Recommended DC Operating Conditions

Parameter	Sym	Min	Typ	Max	Units
Supply Voltage	VCC	4.5	5.0	5.5	V
Supply Voltage	VSS	0	0	0	V
Input High Voltage	VIH	2.2	--	6.0	V
Input Low Voltage	VIL	-0.3	--	0.8	V

AC Test Conditions

Input Pulse Levels ..... VSS to 3.0V
Input Rise and Fall Times 5ns
Input and Output Timing Levels 1.5V
Output Load ..... 1TTL, CL = 30pF
(note: For TEHQZ, TGHQZ and TWLQZ, CL = 5pF)

DC Electrical Characteristics

Parameter	Sym	Conditions		Min	Typ*	Max	Units
Operating Power Supply Current	ICC1	$\overline{W}$, $\overline{E}$ = VIL, II/O = 0mA, Min Cycle S = VIH, Min Cycle		--	50	140	mA
Standby (TTL) Power Supply Current	ICC2	$\overline{E}$ ≥ VIH, VIN ≤ VIL or ≥ VIH		--	2	30	mA
Full Standby Power Supply Current	ICC3	$\overline{E}$ ≥ VCC-0.2V	CA	--	0.1	1	mA
		VIN ≥ VCC-0.2V or VIN ≤ 0.2V	LPA/PA	--	50	600	µA
Input Leakage Current	IIL	VIN = 0V to VCC		--	--	±10	µA
Output Leakage Current	IOL	V I/O = 0V to VCC		--	--	±10	µA
Output High Voltage	VOH	IOH = -4.0mA		2.4	--	--	V
Output Low Voltage	VOL	IOL = 8.0mA		--	--	0.4	V

*Typical: TA = 25°C, VCC = 5.0V

Truth Table

$\overline{G}$	$\overline{E}$	S	$\overline{W}$	Mode	Output	Power
X	H	X	X	Standby	High Z	ICC2, ICC3
X	X	L	X	Output Deselect	High Z	ICC1
H	L	H	H	Output Deselect	High Z	ICC1
L	L	H	H	Read	DOUT	ICC1
X	L	H	L	Write	DIN	ICC1

Capacitance

(f=1.0MHz, VIN=VCC or VSS)

Parameter	Sym	Max			Unit
		LCC	FP	DIP	
Input Capacitance (Except DQ Pins)	CI	7	10	10	pF
Capacitance Control (DQ Pins)	CD/Q	8	12	12	pF

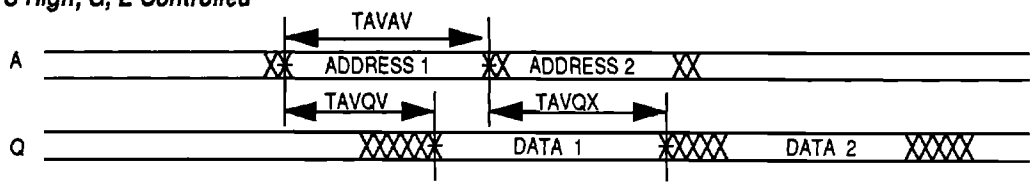
These parameters are sampled, not 100% tested.

AC Characteristics
Read Cycle

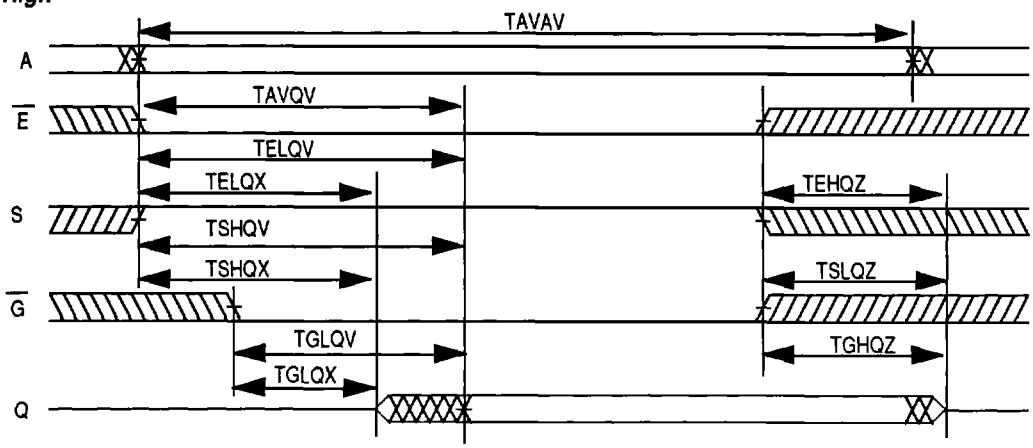
Parameter	Symbol		35ns Min	35ns Max	45ns Min	45ns Max	55ns Min	55ns Max	70ns Min	70ns Max	Units
Read Cycle Time	TAVAV		35		45		55		70		ns
Address Access Time	TAVQV			35		45		55		70	ns
Chip Enable Access Time	TELQV	$\overline{E}$		35		45		55		70	ns
	TSHQV	S		20		25		30		40	ns
Chip Enable to Output Low Z (1)	TELQX	$\overline{E}$	5		5		5		5		ns
	TSHQX	S	5		5		5		5		ns
Chip Disable to Output in High Z (1)	TEHQZ	$\overline{E}$	0	20	0	25	0	35	0	40	ns
	TSLQZ	S	0	20	0	25	0	35	0	40	ns
Output Hold from Address Change	TAVQX		5		5		5		5		ns
Output Enable to Output Valid	TGLQV			20		25		30		40	ns
Output Enable to Output in Low Z (1)	TGLQX		5		5		5		5		ns
Output Disable to Output in High Z (1)	TGHQZ			20		25		30		40	ns

Note 1: Parameter guaranteed, but not tested.

Read Cycle 1
$\overline{W}$, S High; $\overline{G}$, $\overline{E}$ Controlled



Read Cycle 2
$\overline{W}$ High

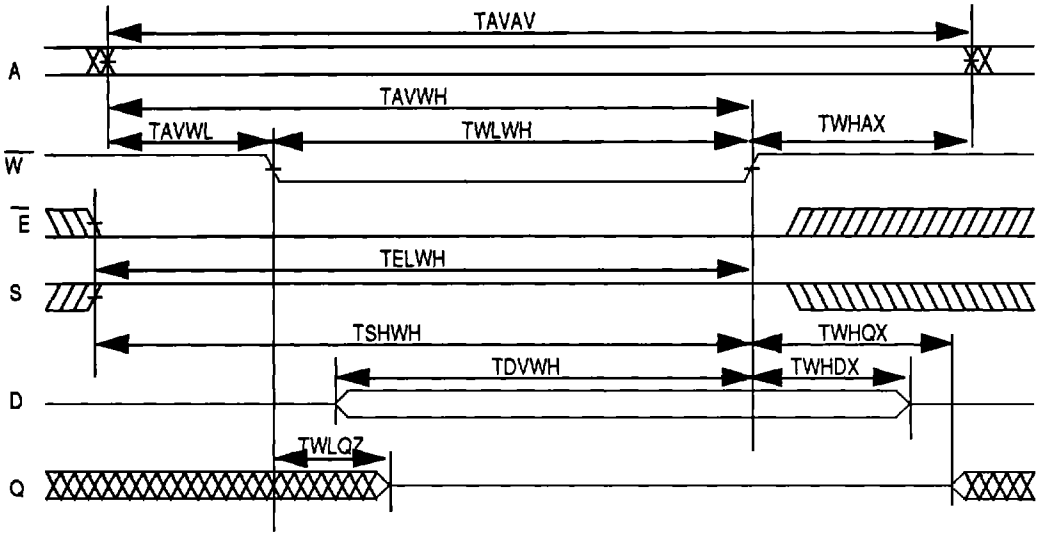


AC Characteristics
Write Cycle

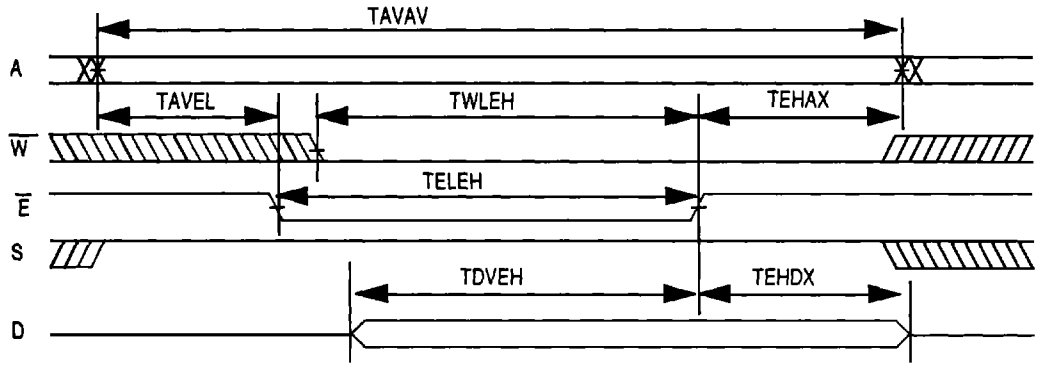
Parameter	Symbol		35ns		45ns		55ns		70ns		Units
			Min	Max	Min	Max	Min	Max	Min	Max	
Write Cycle Time	TAVAV		35		45		55		70		ns
Chip Enable to	TELWH	$\overline{E}$	30		40		45		50		ns
End of Write	TELEH	$\overline{E}$	30		40		45		50		ns
	TSHWH	S	25		35		40		45		ns
	TSHSL	S	25		35		40		45		ns
Address Setup Time	TAVWL	$\overline{W}$	5		5		5		5		ns
	TAVEL	$\overline{E}$	5		5		5		5		ns
	TAVSH	S	5		5		5		5		ns
Address Valid to End of Write	TAVWH		25		35		50		60		ns
Write Pulse Width	TWLWH	$\overline{W}$	15		25		30		40		ns
	TWLEH	$\overline{E}$	15		25		30		40		ns
	TWLSL	S	15		25		30		40		ns
Write Recovery Time	TWHAX	$\overline{W}$	5		5		5		5		ns
	TEHAX	$\overline{E}$	5		5		5		5		ns
	TSLAX	S	5		5		5		5		ns
Data Hold Time	TWHDX	$\overline{W}$	5		5		5		5		ns
	TEHDX	$\overline{E}$	5		5		5		5		ns
	TSLDX	S	5		5		5		5		ns
Write to Output in High Z (1)	TWLQZ			15		20		25		35	ns
Data to Write Time	TDVWH	$\overline{W}$	15		20		30		40		ns
	TDVEH	$\overline{E}$	15		20		30		40		ns
	TDVSL	S	15		20		30		40		ns
Output Active from End of Write (1)	TWHQX		5		5		5		5		ns

Note 1: Parameter guaranteed, but not tested.

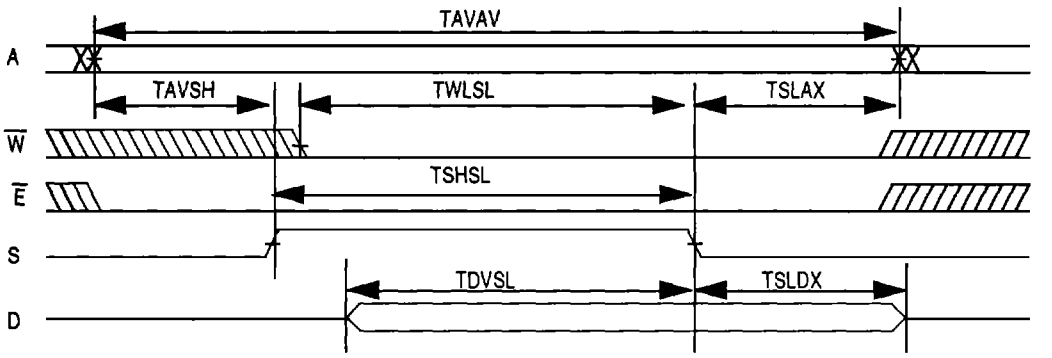
Write Cycle 1
Late Write, $\overline{W}$ Controlled



Write Cycle 2
Early Write, $\overline{E}$ Controlled



Write Cycle 3
Early Write, S Controlled



Data Retention Characteristics — *LPA Version Only*

Characteristic	Sym	Test Conditions	Min	Typ	Max	Unit
Data Retention Voltage	VDD	VDD = 2.0V	2	--	--	V
Data Retention Quiescent Current	ICCDR	$\overline{E}$≥ VDD -0.2V	--	2	200	µA
Chip Disable to Data Retention Time	TCDR	VIN ≥VDD -0.2V	0	--	--	ns
Operation Recovery Time	TR	or VIN ≤0.2V	TAVAV*	--	--	ns

*Read Cycle Time

Data Retention $\overline{E}$ Controlled