DPS128M8

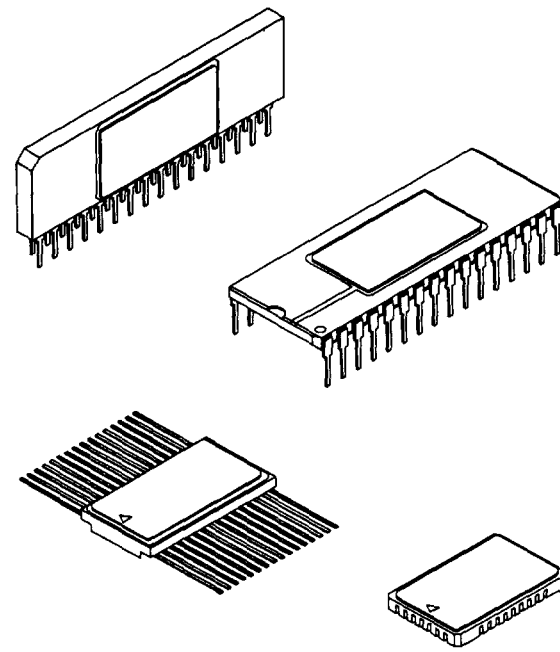
CERAMIC 128K X 8 CMOS SRAM MONOLITHIC

DESCRIPTION:

The DPS128M8 is a monolithic 128K X 8 Static Random Access Memory (SRAM) fabricated using CMOS technology. It is designed for use in high density, high speed, low power applications. All pins are TTL compatible and a single +5 Volt power supply is required.

The DPS128M8 has extremely low standby power dissipation making it suitable for battery backup.

The 600-mil wide, 32-pin ceramic, Dual-In-Line Package (DIP), conforms to the JEDEC standard. Dense-Pac also offers a 32-pin ceramic FLATPACK, a 32-Pad Leadless Chip Carrier (LCC), and a space saving 32-pin Zig-Zag-In-Line Package (ZIP).



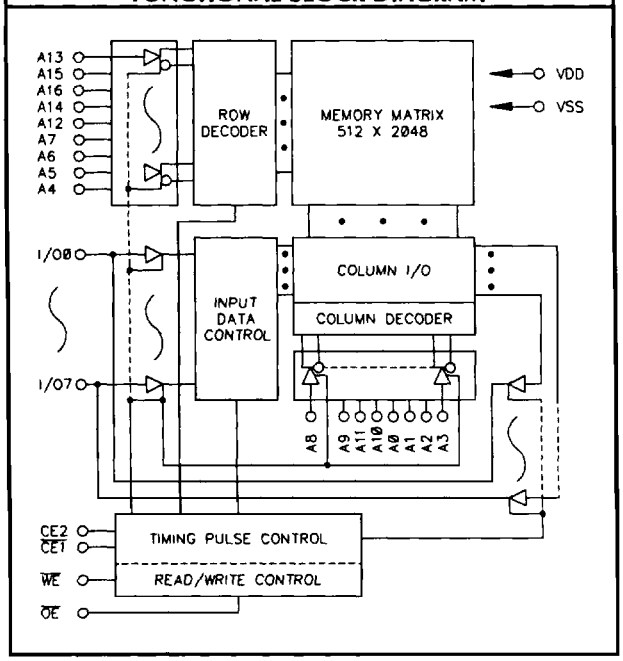
FEATURES:

- 131,072 by 8-Bits Organization
- Access Times: 70*, 85, 100, 120, 150ns (max.)
- Low Power: 10µW (typ.) Standby
  225mW (typ.) Operating
- Fully Static Operation; No Clock or Refresh Required
- TTL Compatible Input and Output
- Common Data Input and Output
- Single +5V Power Supply, ±10% Tolerance
- Two Chip Enables
- Output Enable Functions
- Faster Access Speeds Available Upon Request
- Package Types:
  32-Pin Ceramic Side Brazed DIP
  32-Pin Ceramic FLATPACK
  32-Pin Ceramic ZIP
  32-Pad Ceramic LCC

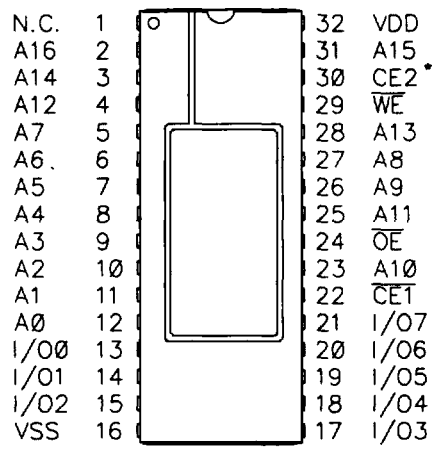
* Commercial Only

PIN NAMES	
A0-A16	Address Inputs
I/O0-I/O7	Data In/Out
$\overline{CE1}$ / CE2	Chip Enables
$\overline{WE}$	Write Enable
$\overline{OE}$	Output Enable
V_{DD}	Power (+5V)
V_{SS}	Ground
N.C.	No Connect

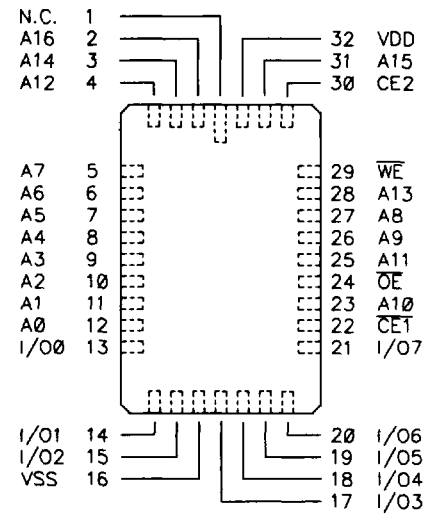
FUNCTIONAL BLOCK DIAGRAM



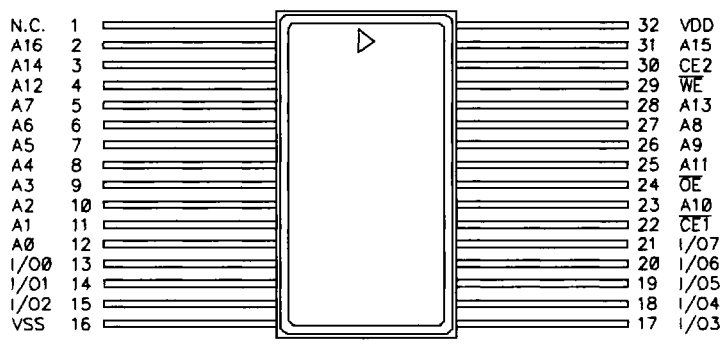
PIN-OUT DIAGRAMS (TOP VIEW)



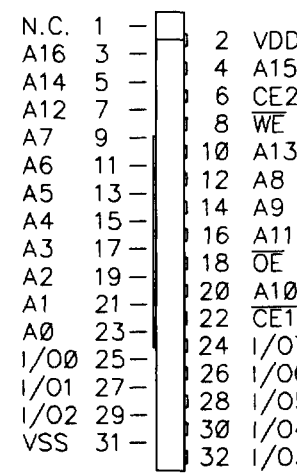
CERDIP



CERAMIC LCC



CERAMIC FLATPACK



CERAMIC ZIP

* Cerdip also available with one Chip Enable (DPS128M8NS). Pin 30 on this version is a no connect (N.C.) consult factory.

RECOMMENDED OPERATING RANGE[1]					
Symbol	Characteristic	Min.	Typ.	Max.	Unit
V_{DD}	Supply Voltage	4.5	5.0	5.5	V
V_{IH}	Input HIGH Voltage	2.2		V_{DD}+0.3	V
V_{IL}	Input LOW Voltage	-0.5[2]		0.8	V

ABSOLUTE MAXIMUM RATINGS[3]			
Symbol	Parameter	Value	Unit
T_{STC}	Storage Temperature	-65 to + 150	°C
T_{BIAS}	Temperature Under Bias	-55 to + 125	°C
V_{DD}	Supply Voltage[1]	-0.5 to + 7.0	V
$V_{I/O}$	Input/Output Voltage[1]	-0.5 to V_{DD}+0.5	V

3

TRUTH TABLE						
Mode	$\overline{CE1}$	CE2	$\overline{OE}$	$\overline{WE}$	I/O Pin	Supply Current
Not Selected	H	X	X	X	HIGH-Z	Standby
Not Selected	X	L	X	X	HIGH-Z	Standby
D_{OUT} Disable	L	H	H	H	HIGH-Z	Active
Read	L	H	L	H	D_{OUT}	Active
Write	L	H	X	L	D_{IN}	Active

L = LOW H = HIGH X = Don't Care

CAPACITANCE [4]: T_A = 25°C, F = 1.0MHz				
Symbol	Parameter	Max.	Unit	Condition
C_{CE}	Chip Enable	8	pF	V_{IN} = 0V
C_{ADR}	Address Input	8		
C_{WE}	Write Enable	8		
C_{OE}	Output Enable	8		
$C_{I/O}$	Data Input/Output	10		

DC OPERATING CHARACTERISTICS: Over operating ranges										
Symbol	Characteristics	Test Conditions	TYP. (*)	C		I		M/B		Unit
				Min.	Max.	Min.	Max.	Min.	Max.	
I_{IN}	Input Leakage Current	V_{IN} = 0V to V_{DD}	-	-2	2	-2	2	-2	2	µA
I_{OUT}	Output Leakage Current	$V_{I/O}$ = 0V to V_{DD}, $\overline{CE}$ or $\overline{OE}$ = V_{IH}, or $\overline{WE}$ = V_{IL}	-	-2	2	-2	2	-2	2	µA
I_{CC1}	Active Supply Current	$\overline{CE}$ = V_{IL}, V_{IN} = V_{IH} or V_{IL}, I_{OUT} = 0mA	15		35		45		50	mA
I_{CC2}	Operating Supply Current	Cycle = min., Duty = 100% I_{OUT} = 0mA	45		70		75		80	mA
I_{SB1}	Full Standby Supply Current (CMOS)	$\overline{CE}$ ≥ V_{DD} -0.2V	2		100		200		500	µA
I_{SB2}	Standby Supply (TTL)	$\overline{CE}$ = V_{IH}	1		3		3		3	mA
I_{DR3}	Data Retention Supply Current (3V)	V_{DR} = 3V, $\overline{CE1}$ ≥ V_{DR} -0.2V, CE2 ≥ V_{DR} -0.2V or CE2 ≤ 0.2V		1		50		100		400
I_{DR2}	Data Retention Supply Current (2V)	V_{DR} = 2V, $\overline{CE1}$ ≥ V_{DR} -0.2V, CE2 ≥ V_{DR} -0.2V or CE2 ≤ 0.2V	1		45		85		350	µA
V_{OL}	Output Low Voltage	I_{OUT} = 2.1mA	-		0.4		0.4		0.4	V
V_{OH}	Output High Voltage	I_{OUT} = -1.0mA	-	2.4		2.4		2.4		V

* Typical Values at +25°C and +5V.

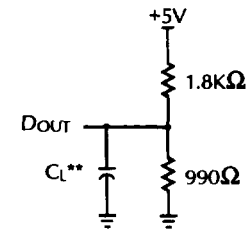
AC TEST CONDITIONS	
Input Pulse Levels	0V to 3.0V
Input Pulse Rise and Fall Times	5ns*
Input and Output Timing Reference Levels	1.5V

* Transition between 0.8V and 2.2V.

OUTPUT LOAD		
Load	C_L	Parameters Measured
1	100 pF	except t_{CLZ}, t_{CHZ}, t_{OHZ}, t_{OLZ}, t_{WLZ} and t_{WHZ}
2	5 pF	t_{CLZ}, t_{CHZ}, t_{OHZ}, t_{OLZ}, t_{WLZ} and t_{WHZ}

Figure 1. Output Load

** Including Probe and Jig Capacitance.



AC OPERATING CONDITIONS AND CHARACTERISTICS - READ CYCLE: Over operating ranges												
No.	Symbol	Parameter	-70		-85		-10		-12		-15		Unit
			Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
1	t_{RC}	Read Cycle Time	70		85		100		120		150		ns
2	t_{AA}	Address Access Time		70		85		100		120		150	ns
3	t_{CO1}	Chip Enable ($\overline{CE1}$) to Output Valid		70		85		100		120		150	ns
4	t_{CO2}	Chip Enable (CE2) to Output Valid		70		85		100		120		150	ns
5	t_{OE}	Output Enable to Output Valid		40		45		50		60		70	ns
6	t_{LZ1}	Chip Enable ($\overline{CE1}$) to Output in LOW-Z [4, 5]	5		5		10		10		10		ns
7	t_{LZ2}	Chip Enable (CE2) to Output in LOW-Z [4, 5]	5		5		10		10		10		ns
8	t_{OLZ}	Output Enable to Output in LOW-Z [4, 5]	0		0		0		0		0		ns
9	t_{HZ1}	Chip Enable ($\overline{CE1}$) to Output in HIGH-Z [4, 5]		30		30		35		45		50	ns
10	t_{HZ2}	Chip Enable (CE2) to Output in HIGH-Z [4, 5]		30		30		35		45		50	ns
11	t_{OHZ}	Output Enable to Output in HIGH-Z [4, 5]		30		30		35		45		50	ns
12	t_{OH}	Output Hold from Address Change	10		10		10		10		10		ns

AC OPERATING CONDITIONS AND CHARACTERISTICS - WRITE CYCLE [6,7]: Over operating ranges												
No.	Symbol	Parameter	-70		-85		-10		-12		-15		Unit
			Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
13	t_{WC}	Write Cycle Time	70		85		100		120		150		ns
14	t_{AW}	Address Valid to End of Write	65		75		90		100		120		ns
15	t_{CW}	Chip Enable to End of Write	65		75		90		100		120		ns
16	t_{AS}	Address Set-up Time***	0		0		0		0		0		ns
17	t_{WP}	Write Pulse Width	55		65		75		85		90		ns
18	t_{WR}	Write Recovery Time	10		10		10		15		15		ns
19	t_{WHZ}	Write Enable to Output in HIGH-Z [4, 5]		30		30		35		40		45	ns
20	t_{DW}	Data to Write Time Overlap	35		35		40		50		60		ns
21	t_{DH}	Data Hold from Write Time	0		0		0		0		0		ns
22	t_{OW}	Output Active from End of Write	5		5		5		5		5		ns

*** Valid for both Read and Write Cycles.

Data Retention AC Characteristics						
Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
V_{DR}	V_{DD} for Data Retention	$\overline{CE1} \geq V_{DD}$ -0.2V, CE2 $\geq V_{DD}$ -0.2V or CE2 $\leq V_{DD}$ 0.2V	2.0	-	-	V
t_{CDR}	Chip Disable to Data Retention Time	See Retention Waveform	0	-	-	ns
t_R	Operation Recovery Time	See Retention Waveform	5	-	-	ms

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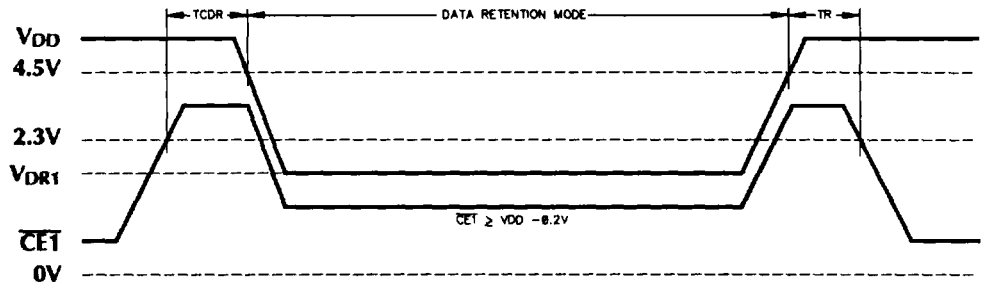
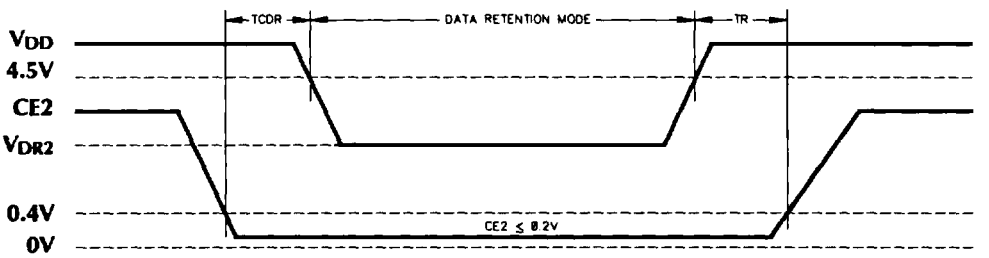
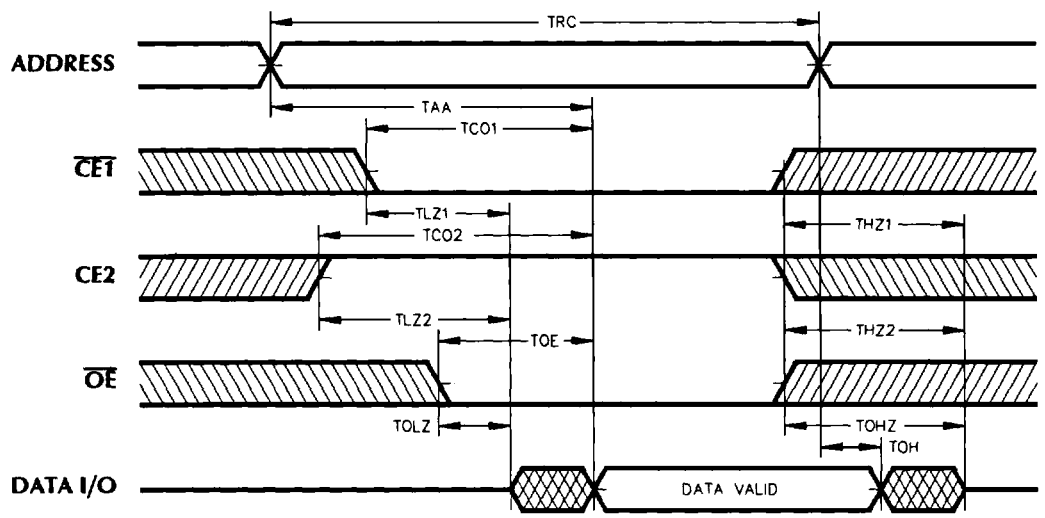
DATA RETENTION WAVEFORM: $\overline{CE1}$ Controlled.



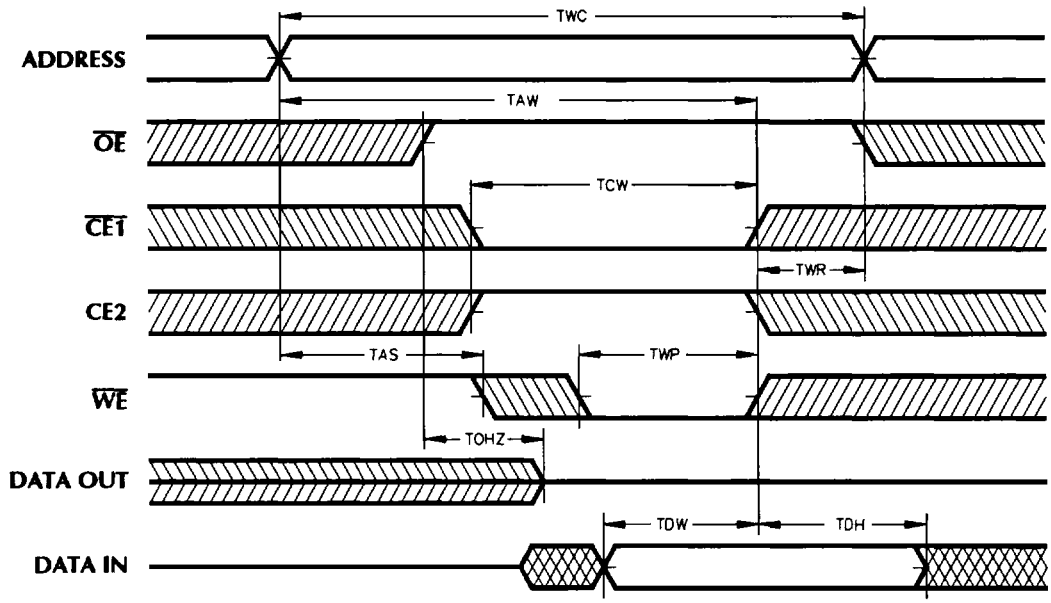
DATA RETENTION WAVEFORM: [8] CE2 Controlled.



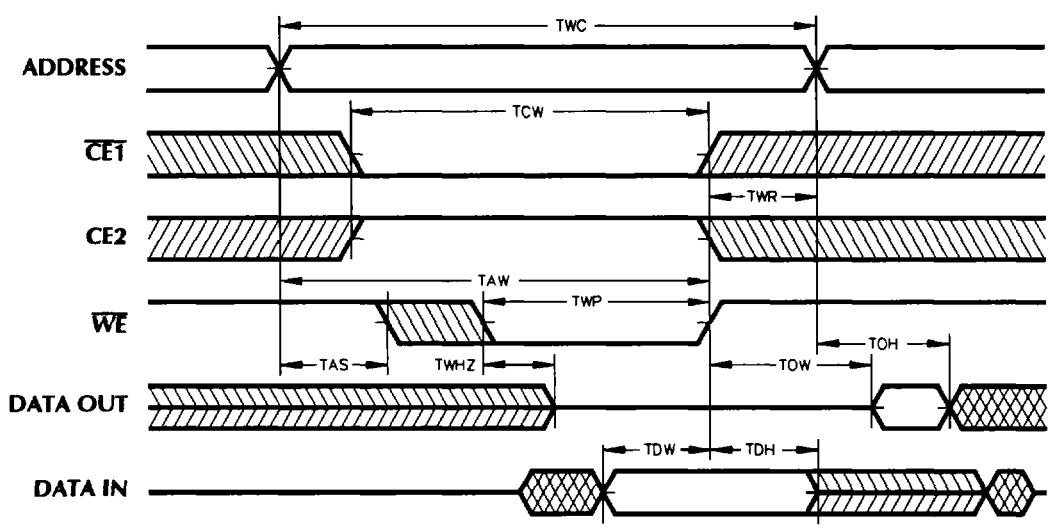
READ CYCLE



WRITE CYCLE 1: $\overline{WE}$ Controlled. $\overline{OE}$ Clocked.



WRITE CYCLE 2: $\overline{CE}$ Controlled. $\overline{OE}$ is LOW.



ORDERING INFORMATION

DP S128M8 X X – XX X

DP	PREFIX	DENSE-PAC
S128M8	DEVICE TYPE	CMOS SRAM 128KX8 MONOLITHIC
X	PACKAGE	F 32-PIN CERAMIC FLATPACK G 32-PAD CERAMIC LCC K 32-PIN CERAMIC ZIP N 32-PIN CERAMIC SIDE BRAZED DIP
X	DESIGN UNIQUENESS	BLANK TWO CHIP ENABLES S SINGLE CHIP ENABLE ("N" PACKAGE ONLY)
XX	SPEED	70 70ns (COMMERCIAL ONLY) 85 85ns 10 100ns 12 120ns 15 150ns
X	GRADE	C COMMERCIAL 0°–+70°C I INDUSTRIAL –40°–+85°C M MILITARY –55°–+125°C B MIL–PROCESSED –55°–+125°C

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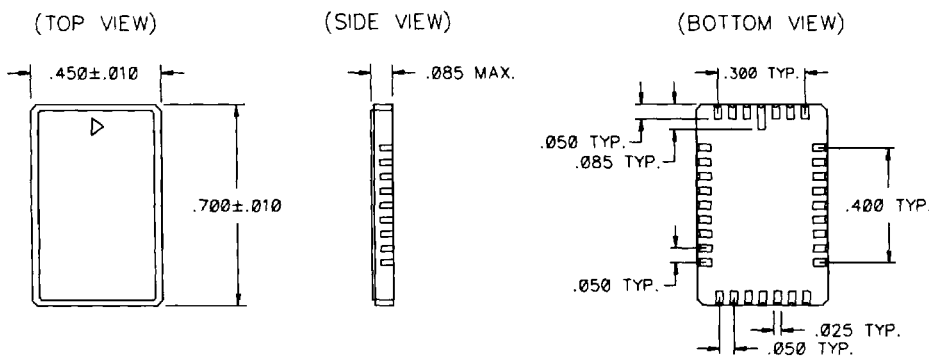
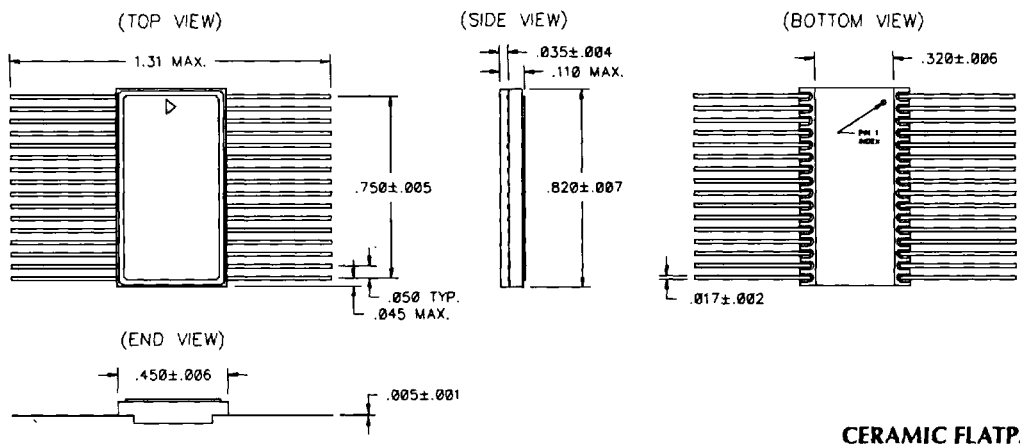
MECHANICAL DIAGRAMS

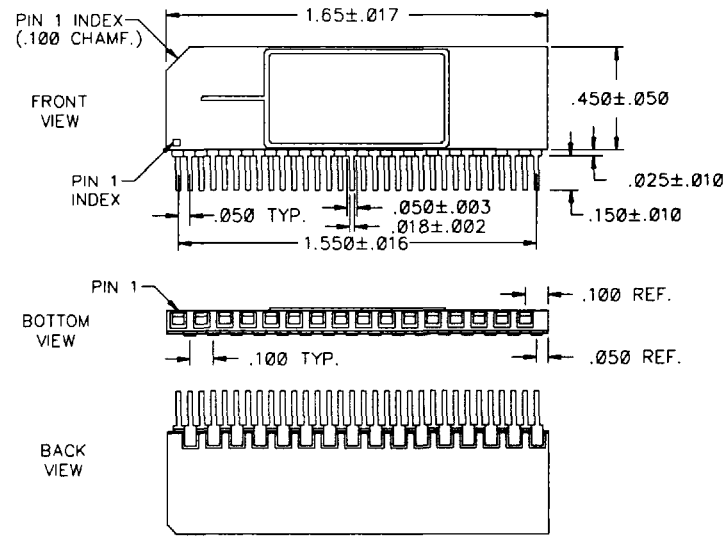


CERAMIC LCC

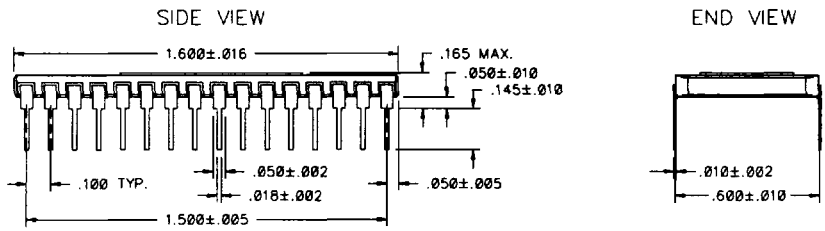


CERAMIC FLATPACK

MECHANICAL DIAGRAMS (Continued)



CERAMIC ZIP



CERAMIC SIDE BRAZED DIP

NOTES:

1. All voltages are with respect to V_{SS}.
2. -2.0V min. for pulse width less than 20ns (V_{IL} min. = -0.5V at DC level).
3. Stresses greater than those under **ABSOLUTE MAXIMUM RATINGS** may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.
4. This parameter is guaranteed and not 100% tested.
5. Transition is measured at the point of ± 500mV from steady state voltage.
6. When $\overline{OE}$ and $\overline{CE}$ are LOW and $\overline{WE}$ is HIGH, I/O pins are in the output state; and input signals of opposite phase to the outputs must not be applied.
7. The outputs are in a high impedance state when $\overline{WE}$ is LOW.
8. CE2 controls address buffer, $\overline{WE}$ buffer, $\overline{CE1}$ buffer and $\overline{OE}$ buffer and D_{IN} buffer. If CE2 controls Data Retention Mode, V_{IN} levels (Address, $\overline{WE}$, $\overline{OE}$, $\overline{CS1}$, I/O) can be in the high impedance state. If $\overline{CE1}$ controls Data Retention Mode, CE2 must be CE2 ≥ V_{DD} -0.2V or 0V ≤ CE2 ≤ 0.2V. The other input levels (Address, $\overline{WE}$, $\overline{OE}$, I/O) can be in the High Impedance State.

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