

DENSE-PAC MICROSYSTEMS

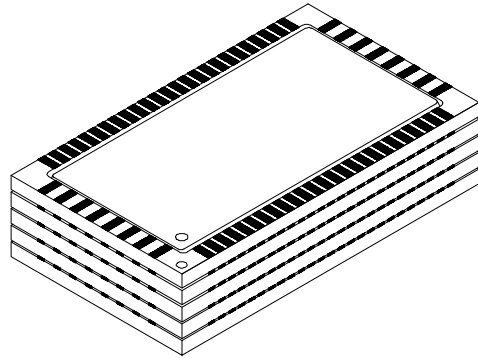
256 Megabit CMOS DRAM DPnnD8MX32RY5

PRELIMINARY

DESCRIPTION:

The DPnnD8MX32RY5 is the 8 Meg x 32 Dynamic RAM module that utilize the new and innovative space saving TSOP stacking technology. The module is constructed of four 4 Meg x 16 Dynamic RAM's that are configured as 2 banks of 4 Meg x 32.

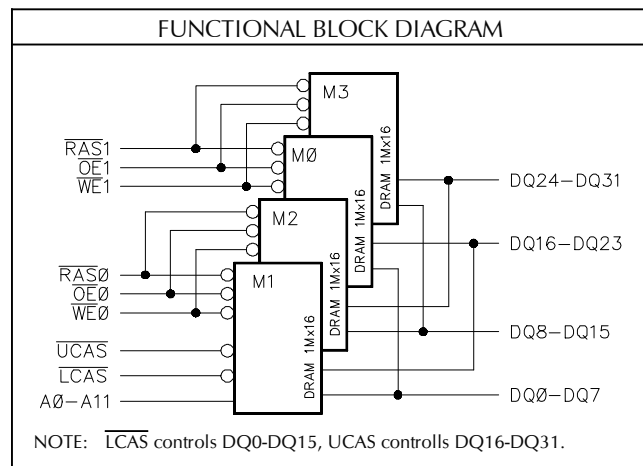
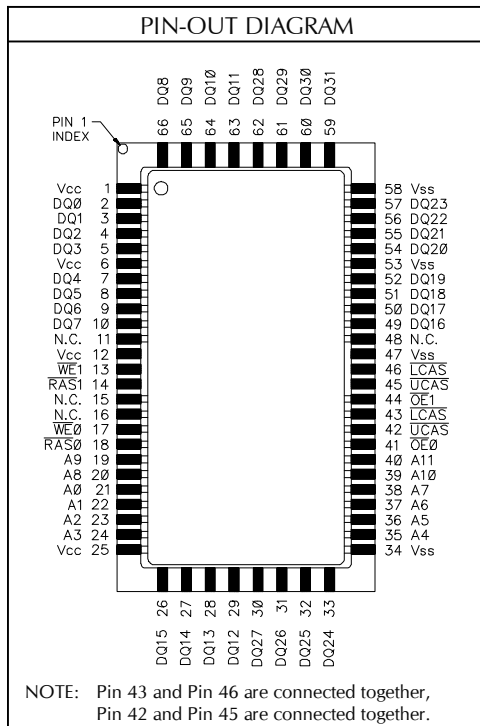
The DPnnD8MX32RY5 provides for a compatible upgrade path to lower density compatible modules. The module features high speed access times, common data inputs and outputs, and three standard refresh modes.



FEATURES:

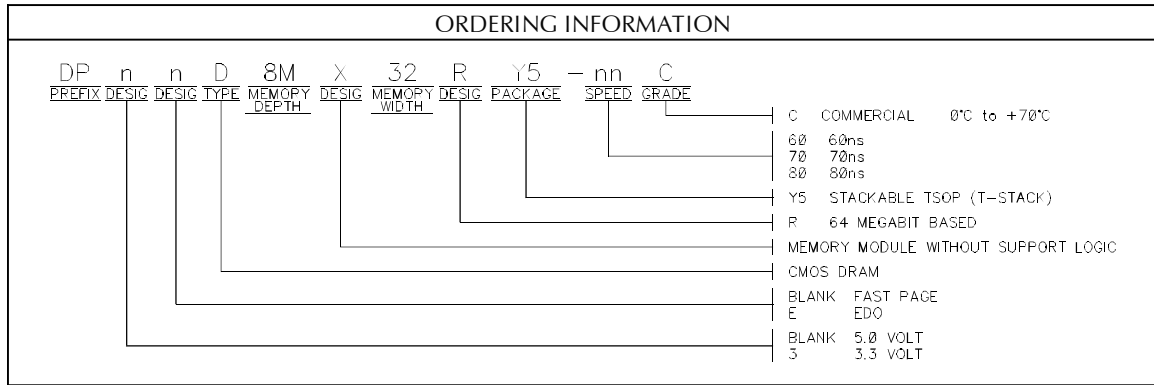
- Access Times: 60, 70, 80ns (max.)
- 5.0V or 3.3V Supply
- Common Data Inputs and Outputs
- EDO or Fast Page Mode Capability
- 4096 Cycles / 64 ms
- 3 Variations of Refresh:
 - \overline{RAS} only Refresh
 - \overline{CAS} before \overline{RAS} Refresh
 - Hidden Refresh
- Package: TSOP Leadless Stack

| PIN NAMES | |
|-------------------------------------|---|
| A0 - A11 | Row Address: A0 - A11 Column Address: A0 - A9 Refresh Address: A0 - A11 |
| DQ0 - DQ31 | Data In / Data Out |
| \overline{UCAS} | Upper Column Address Strobe |
| \overline{LCAS} | Lower Column Address Strobe |
| $\overline{RAS0} - \overline{RAS1}$ | Row Address Enables |
| $\overline{WE0} - \overline{WE1}$ | Data Write Enables |
| $\overline{OE0} - \overline{OE1}$ | Data Output Enables |
| V _{DD} | Power Supply (+5V) |
| V _{SS} | Ground |
| N.C. | No Connect |

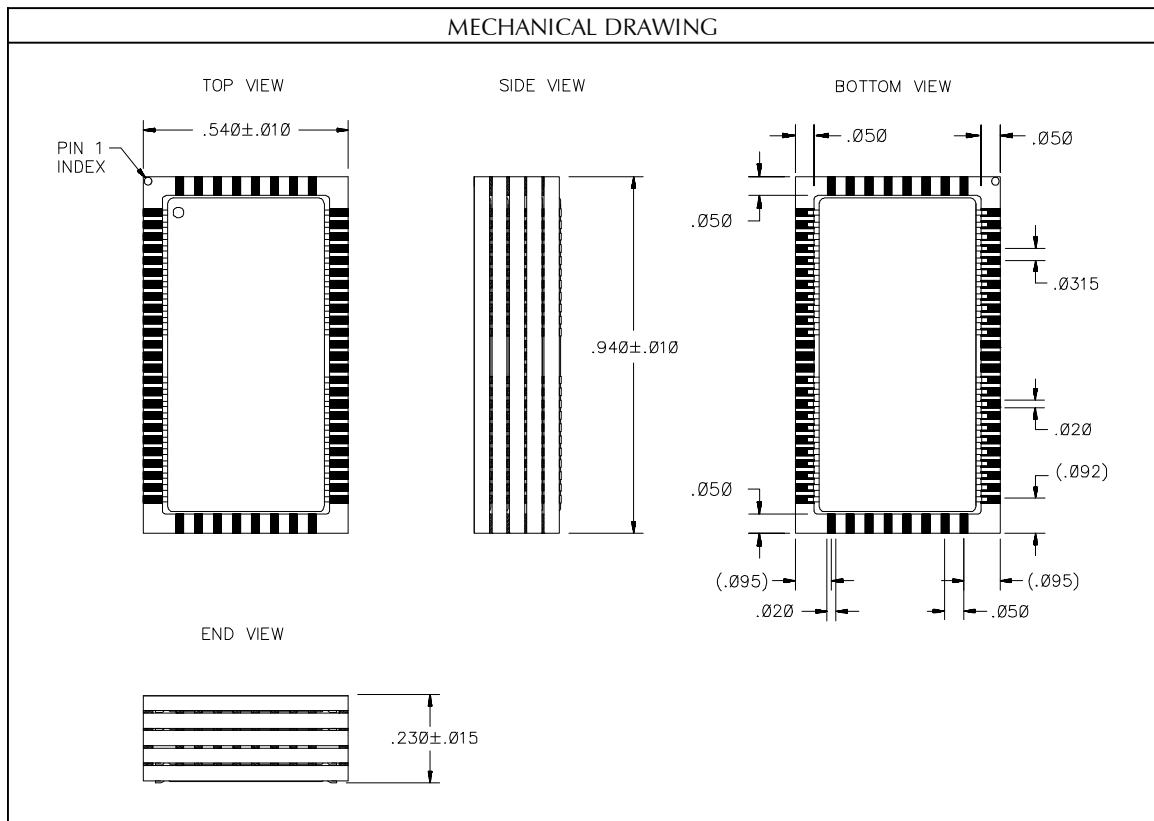


PRELIMINARY

ORDERING INFORMATION



MECHANICAL DRAWING



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