Data Sheet
January 1992

AT&T Microelectronics

ATT7C187

High-Speed CMOS SRAM 64 Kbit (64K x 1), Separate I/O

Features

- High speed — 10 ns maximum access time
- Automatic powerdown during long cycles
- Advanced CMOS technology
- Chip-select powerdown
- Data retention at 2 V for battery backup operation
- Plug-compatible with IDT7187 and CY7C187
- Low-power operation
  — Active: 500 mW typical at 25 ns
  — Standby: 500 µW typical
- Package styles available:
  — 22-pin, plastic DIP
  — 24-pin, plastic SOJ (J-lead)

Description

The ATT7C187 device is a high-performance, low-power, CMOS static RAM organized as 65,536 words by 1 bit per word. Parts are available in four speeds with worst-case access times from 10 ns to 20 ns.

All interface signals are TTL compatible, and operation is from a single 5 V power supply. Power consumption is 500 mW (typical) at 25 ns. Dissipation drops to 75 mW (typical) when the memory is deselected ($\overline{CE}$ is high).

Two standby modes are available. Automatic powerdown during long cycles reduces power consumption when the memory is deselected, or during read or write accesses that are longer than the minimum access time. In addition, data can be retained in inactive storage with a supply voltage as low as 2 V. The ATT7C187 consumes only 30 µW at 3 V (typical), thereby allowing effective battery backup operation.

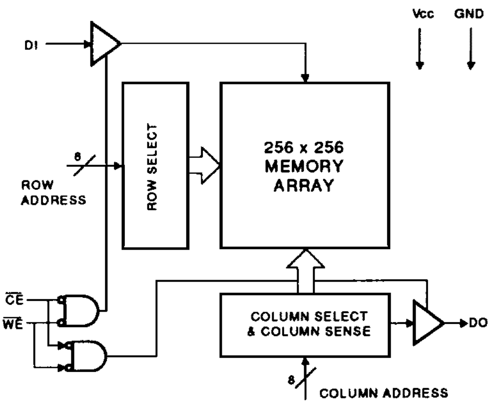


Figure 1. Block Diagram

Pin Information

Table 1. DIP Pin Descriptions

Pin	Name/Function
A0—A15	Address
DIN	Data Input
DOUT	Data Output
$\overline{CE}$	Chip Enable
$\overline{WE}$	Write Enable
GND	Ground
Vcc	Power

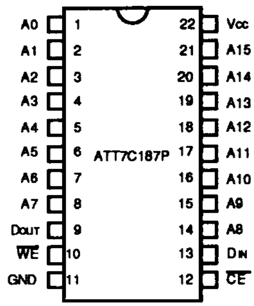


Figure 2. Pin Diagram

Table 2. SOJ Pin Descriptions

Pin	Function
A0—A15	Address
DIN	Data Input
DOUT	Data Output
$\overline{CE}$	Chip Enable
$\overline{WE}$	Write Enable
GND	Ground
Vcc	Power
NC	No Connect

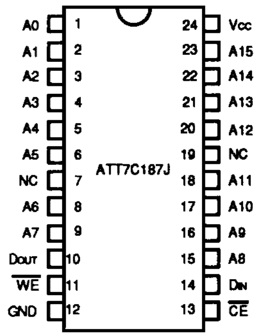


Figure 3. Pin Diagram

Functional Description

The ATT7C187 device provides asynchronous (unclocked) operation with matching access and cycle times. An active-low chip enable and a 3-state output simplify the connection of several chips for increased storage capacity.

Memory locations are specified on address pins A0 through A15. Reading from a designated location is accomplished by presenting an address and then taking $\overline{CE}$ low while $\overline{WE}$ remains high. The data in the addressed memory location then appears on the data-out pin within one access time. When $\overline{CE}$ is high or $\overline{WE}$ is low, the output pin stays in a high-impedance state.

Writing to an addressed location is accomplished when the $\overline{CE}$ and $\overline{WE}$ inputs are both low. Either signal can be used to terminate the write operation. Data-in and data-out signals have the same polarity.

Latch-up and static discharge protection are provided on-chip. The ATT7C187 can withstand an injection of up to 200 mA on any pin without damage.

Absolute Maximum Ratings

Stresses in excess of the Absolute Maximum Ratings can cause permanent damage to the device. These are absolute stress ratings only. Functional operation of the device is not implied at these or any other conditions in excess of those given in the operational sections of this data sheet. Exposure to Absolute Maximum Ratings for extended periods can adversely affect device reliability.

Parameter	Symbol	Min	Max	Unit
Storage Temperature	T_{stg}	−65	150	°C
Operating Ambient Temperature	T_A	−55	125	°C
Supply Voltage with Respect to Ground	V_{CC}	−0.5	7.0	V
Input Signal with Respect to Ground	—	−3.0	7.0	V
Signal Applied to High-impedance Output	—	−3.0	7.0	V
Output Current into Low Outputs	—	—	25	mA
Latch-up Current	—	>200	—	mA

Recommended Operating Conditions

Mode	Temperature Range (Ambient)	Supply Voltage
Active Operation	0 °C to 70 °C	$4.5\ V \le V_{CC} \le 5.5\ V$
Data Retention	0 °C to 70 °C	$2.0\ V \le V_{CC} \le 5.5\ V$

Electrical Characteristics

Over all Recommended Operating Conditions

Table 3. General Electrical Characteristics

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Output Voltage:						
High	V_{OH}	I_{OH} = –4.0 mA, V_{CC} = 4.5 V	2.4	—	—	V
Low	V_{OL}	I_{OL} = 8.0 mA	—	—	0.4	V
Input Voltage:						
High	V_{IH}	—	2.2	—	V_{CC} + 0.3	V
Low[1]	V_{IL}	—	–3.0	—	0.8	V
Input Current	I_{IX}	Ground ≤ V_I ≤ V_{CC}	–10	—	10	µA
Output Leakage Current	I_{OZ}	Ground ≤ V_O ≤ V_{CC}, $\overline{CE}$ = V_{CC}	–10	—	10	µA
Output Short Current	I_{OS}	V_O = Ground, V_{CC} = Max[2]	—	—	–350	mA
Vcc Current:						
Inactive[3]	I_{CC2}	—	—	15	30	mA
Standby[4]	I_{CC3}	—	—	100	500	µA
DR Mode	I_{CC4}	V_{CC} = 2.0 V[5]	—	10	250	µA
Capacitance:						
Input	C_I	T_A = 25 °C, V_{CC} = 5.0 V	—	—	5	pF
Output	C_O	Test frequency = 1 MHz[6]	—	—	7	pF

1. This device provides hard clamping of transient undershoot. Input levels below ground are clamped beginning at –0.6 V. A current in excess of 100 mA is required to reach –2 V. The device can withstand indefinite operation with inputs as low as –3 V subject only to power dissipation and bond-wire fusing constraints.
2. Duration of the output short-circuit should not exceed 30 s.
3. Tested with outputs open and all address and data inputs changing at the maximum write-cycle rate. The device is continuously disabled, i.e., $\overline{CE}$ ≥ V_{IH}.
4. Tested with outputs open and all address and data inputs stable. The device is continuously disabled, i.e., $\overline{CE}$ = V_{CC}. Input levels are within 0.2 V of V_{CC} or ground.
5. Data retention operation requires that V_{CC} never drops below 2.0 V. $\overline{CE}$ must be ≥ V_{CC} – 0.2 V. For all other inputs, V_{IN} ≥ V_{CC} – 0.2 V or V_{IN} < 0.2 V is required to ensure full powerdown.
6. This parameter is not 100% tested.

Table 4. Electrical Characteristics by Speed

Parameter	Symbol	Test Condition	Speed (ns)					Unit
			25	20	15	12	10	
Max Vcc Current, Active	I_{CC1}	*	100	125	160	190	205	mA

* Tested with outputs open and all address and data inputs changing at the maximum write-cycle rate. The device is continuously enabled for writing, i.e., $\overline{CE}$ and $\overline{WE}$ ≤ V_{IL}. Input pulse levels are 0 V to 3.0 V. Max I_{CC} shown applies over the active operating temperature range.

Timing Characteristics

Table 5. Read Cycle[1, 2, 3, 4]

Over all Recommended Operating Conditions; all measurements in ns. Test conditions assume input transition times of less than 3 ns, reference levels of 1.5 V, input pulse levels of 0 V to 3.0 V (see Figure 10), and output loading for specified I_{OL} and I_{OH} +30 pF (see Figure 9A).

Symbol	Parameter	Speed									
		25		20		15		12		10	
		Min	Max	Min	Max	Min	Max	Min	Max	Min	Max
tADXADX, tCELCEH	Read-cycle Time	25	—	20	—	15	—	12	—	10	—
tADXDOV	Address Change to Output Valid[5, 6]	—	25	—	20	—	15	—	12	—	10
tADXDOX	Address Change to Output Change	3	—	3	—	3	—	3	—	3	—
tCELDOV	Chip Enable Low to Output Valid[5, 7]	—	25	—	20	—	15	—	12	—	10
tCELDOZ	Chip Enable Low to Output Low-Z[8, 9]	3	—	3	—	3	—	3	—	3	—
tCEHDOZ	Chip Enable High to Output High-Z[8, 9]	—	10	—	8	—	8	—	5	—	4
tCELICH, tADXICH	Chip Enable Low or Address Change to Powerup[10, 11]	0	—	0	—	0	—	0	—	0	—
tICHICL	Powerup to Powerdown[10, 11]	—	25	—	20	—	20	—	20	—	18

1. Each parameter is shown as a minimum or maximum value. Input requirements are specified from the point of view of the external system driving the chip. For example, tADXWEH (Table 6) is specified as a minimum since the external system must supply at least that much time to meet the worst-case requirements of all parts. Responses from the internal circuitry are specified from the point of view of the device. Access time, for example, is specified as a maximum since worst-case operation of any device always provides data within that time.
2. All address timings are referenced from the last valid address line to the first transitioning address line.
3. $\overline{CE}$ or $\overline{WE}$ must be high during address transitions.
4. This product is a very high-speed device, and care must be taken during testing in order to realize valid test information. Inadequate attention to setups and procedures can cause a good part to be rejected as faulty. Long high-inductance leads that cause supply bounce must be avoided by bringing the Vcc and ground planes directly up to the contactor fingers. A 0.01 µF high-frequency capacitor is also required between Vcc and ground. To avoid signal reflections, proper terminations must be used.
5. $\overline{WE}$ is high for the read cycle.
6. The chip is continuously selected ($\overline{CE}$ low).
7. All address lines are valid prior to or coincident with the $\overline{CE}$ transition to low.
8. At any given temperature and voltage condition, output-disable time is less than output-enable time for any given device.
9. Transition is measured ±200 mV from steady-state voltage with specified loading in Figure 9B. This parameter is sampled and not 100% tested.
10. This parameter is not 100% tested.
11. Powerup from I_{CC2} to I_{CC1} occurs as a result of any of the following conditions: (1) falling edge of $\overline{CE}$, (2) falling edge of $\overline{WE}$ ($\overline{CE}$ active), (3) transition on any address line ($\overline{CE}$ active), or (4) transition on any data line ($\overline{CE}$ and $\overline{WE}$ active). The device automatically powers down from I_{CC1} to I_{CC2} after tICHICL has elapsed from any of the prior conditions. Power dissipation is dependent only on cycle rate, not on chip-select pulse width.

Timing Characteristics (continued)

Table 6. Write Cycle[1, 2, 3, 4] (See Figures 6, 7, and 8.)

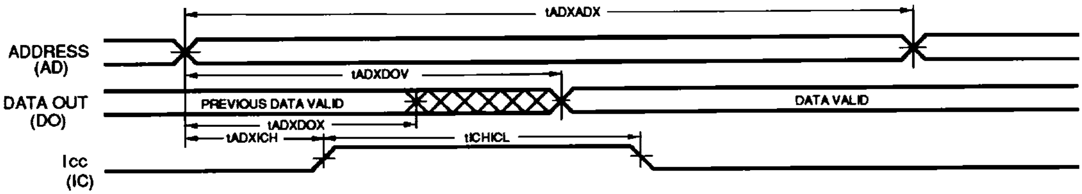
Over all Recommended Operating Conditions; all measurements in ns. Test conditions assume input transition times of less than 3 ns, reference levels of 1.5 V, input pulse levels of 0 V to 3.0 V (see Figure 10), and output loading for specified I_{OL} and I_{OH} +30 pF (see Figure 9A).

Symbol	Parameter	Speed									
		25		20		15		12		10	
		Min	Max	Min	Max	Min	Max	Min	Max	Min	Max
tADXADX	Write-cycle Time	20	—	20	—	15	—	12	—	10	—
tCELWEH	Chip Enable Low to End of Write	15	—	15	—	12	—	10	—	8	—
tADXWEX, tADXWEL	Address Change to Beginning of Write	0	—	0	—	0	—	0	—	0	—
tADXWEH	Address Change to End of Write	15	—	15	—	12	—	10	—	8	—
tWEHADX	End of Write to Address Change	0	—	0	—	0	—	0	—	0	—
tWELWEH	Write Enable Low to End of Write	15	—	15	—	12	—	10	—	8	—
tDIVWEH, tDIVCEH	Data Valid to End of Write	10	—	10	—	7	—	6	—	5	—
tWEHDIX	End of Write to Data Change	0	—	0	—	0	—	0	—	0	—
tWEHDOZ	Write Enable High to Output Low-Z[5, 6]	0	—	0	—	0	—	0	—	0	
tWELDOZ	Write Enable Low to Output High-Z[5, 6]	—	7	—	7	—	5	—	4	—	4
tCELICH	Chip Enable Low to Powerup[7, 8]	0	—	0	—	0	—	0	—	0	—
tWELICH	Write Enable Low to Powerup[7, 8]	0	—	0	—	0	—	0	—	0	—
tCEHVCL	Chip Enable High to Data Retention[7]	0	—	0	—	0	—	0	—	0	—
tICHICL	Powerup to Powerdown	—	25	—	20	—	20	—	20	—	18

1. Each parameter is shown as a minimum or maximum value. Input requirements are specified from the point of view of the external system driving the chip. For example, tADXWEH is specified as a minimum since the external system must supply at least that much time to meet the worst-case requirements of all parts. Responses from the internal circuitry are specified from the point of view of the device. Access time, for example, is specified as a maximum since worst-case operation of any device always provides data within that time.
2. All address timings are referenced from the last valid address line to the first transitioning address line.
3. $\overline{CE}$ or $\overline{WE}$ must be high during address transitions.
4. This product is a very high-speed device, and care must be taken during testing in order to realize valid test information. Inadequate attention to setups and procedures can cause a good part to be rejected as faulty. Long high-inductance leads that cause supply bounce must be avoided by bringing the Vcc and ground planes directly up to the contactor fingers. A 0.01 µF high-frequency capacitor is also required between Vcc and ground. To avoid signal reflections, proper terminations must be used.
5. At any given temperature and voltage condition, output-disable time is less than output-enable time for any given device.
6. Transition is measured ±200 mV from steady-state voltage with specified loading in Figure 9B. This parameter is sampled and not 100% tested.
7. This parameter is not 100% tested.
8. Powerup from I_{CC2} to I_{CC1} occurs as a result of any of the following conditions: (1) falling edge of $\overline{CE}$, (2) falling edge of $\overline{WE}$ ($\overline{CE}$ active), (3) transition on any address line ($\overline{CE}$ active), or (4) transition on any data line ($\overline{CE}$ and $\overline{WE}$ active). The device automatically powers down from I_{CC1} to I_{CC2} after tICHICL has elapsed from any of the prior conditions. Power dissipation is dependent only on cycle rate, not on chip-select pulse width.

Timing Characteristics (continued)

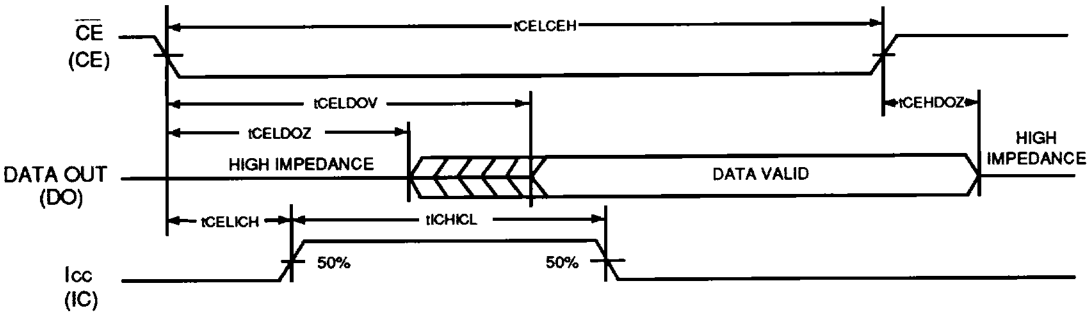
Timing Diagrams



Notes:
WE is high for the read cycle.

The chip is continuously selected (CE low).

Figure 4. Read Cycle — Address-Controlled

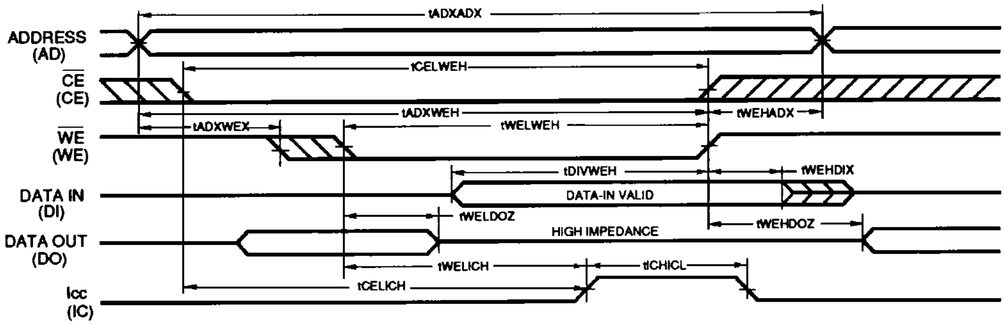


Notes:
WE is high for the read cycle.

All address lines are valid prior to or coincident with the CE transition to low.

Figure 5. Read Cycle — CE-Controlled

Timing Characteristics (continued)



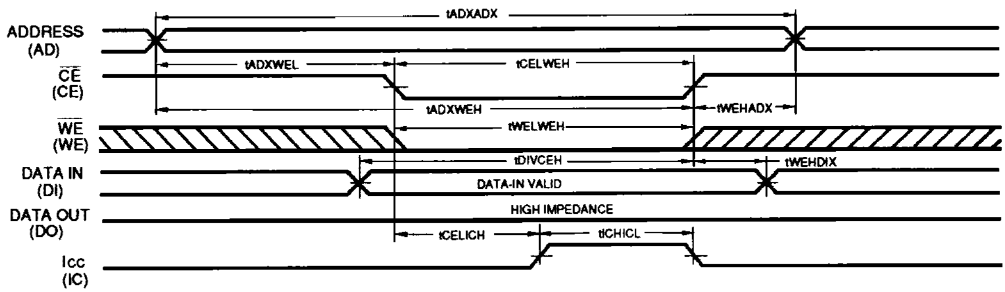
Notes:
The internal write cycle of the memory is defined by the overlap of $\overline{CE}$ low and $\overline{WE}$ low. Both signals must be low to initiate a write. Either signal can terminate a write by going high. The address, data, and control input setup and hold times should be referred to the signal that falls last or rises first.

If $\overline{WE}$ goes low before or concurrent with $\overline{CE}$ going low, the output remains in a high-impedance state.

If $\overline{CE}$ goes high before or concurrent with $\overline{WE}$ going high, the output remains in a high-impedance state.

Powerup from I_{CC2} to I_{CC1} occurs as a result of any of the following conditions: (1) falling edge of $\overline{CE}$, (2) falling edge of $\overline{WE}$ ($\overline{CE}$ active), (3) transition on any address line ($\overline{CE}$ active), or (4) transition on any data line ($\overline{CE}$ and $\overline{WE}$ active). The device automatically powers down from I_{CC1} to I_{CC2} after tICHICL has elapsed from any of the prior conditions. Power dissipation is dependent only on cycle rate, not on chip-select pulse width.

Figure 6. Write Cycle — $\overline{WE}$-Controlled



Notes:
The internal write cycle of the memory is defined by the overlap of $\overline{CE}$ low and $\overline{WE}$ low. Both signals must be low to initiate a write. Either signal can terminate a write by going high. The address, data, and control input setup and hold times should be referred to the signal that falls last or rises first.

If $\overline{WE}$ goes low before or concurrent with $\overline{CE}$ going low, the output remains in a high-impedance state.

If $\overline{CE}$ goes high before or concurrent with $\overline{WE}$ going high, the output remains in a high-impedance state.

Powerup from I_{CC2} to I_{CC1} occurs as a result of any of the following conditions: (1) falling edge of $\overline{CE}$, (2) falling edge of $\overline{WE}$ ($\overline{CE}$ active), (3) transition on any address line ($\overline{CE}$ active), or (4) transition on any data line ($\overline{CE}$ and $\overline{WE}$ active). The device automatically powers down from I_{CC1} to I_{CC2} after tICHICL has elapsed from any of the prior conditions. Power dissipation is dependent only on cycle rate, not on chip-select pulse width.

Figure 7. Write Cycle — $\overline{CE}$-Controlled

Timing Characteristics (continued)

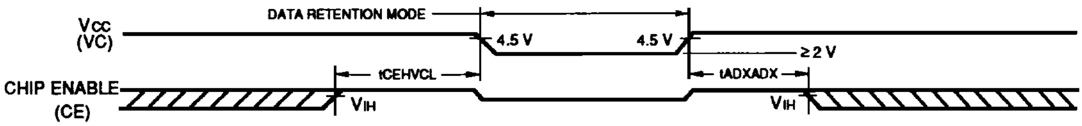


Figure 8. Data Retention

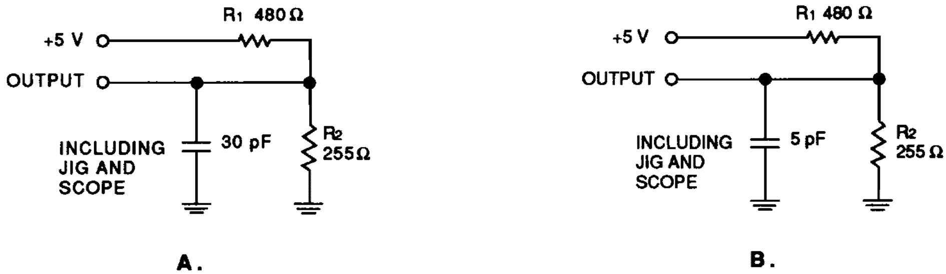


Figure 9. Test Loads

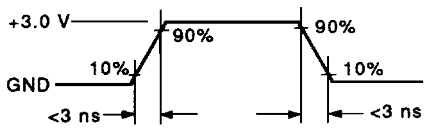
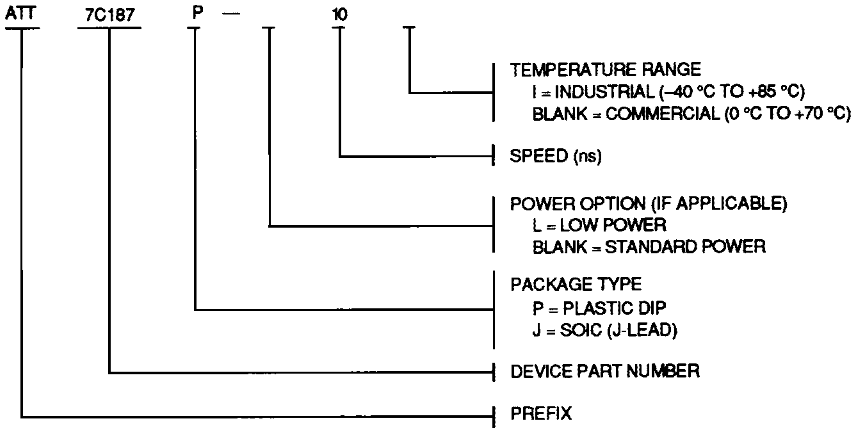


Figure 10. Transition Times

Ordering Information



Operating Range 0 °C to 70 °C

Package Style	Performance Speed				
	25 ns	20 ns	15 ns	12 ns	10 ns
22-Pin, Plastic DIP	ATT7C187P-25	ATT7C187P-20	ATT7C187P-15	ATT7C187P-12	ATT7C187P-10
24-Pin, Plastic SOJ	ATT7C187J-25	ATT7C187J-20	ATT7C187J-15	ATT7C187J-12	ATT7C187J-10