POWER
MANAGEMENT

88PL810/88PL815/88PL830

High Current, Adjustable 8 Level LDO Regulator

Advance Datasheet, Patent Pending

Doc. No. MV-S102944-00, Rev. D
October 31, 2007
Approved by Document Control

MOVING FORWARD FASTER®

MARVELL®

Document Status	
Advance Information	This document contains design specifications for initial product development. Specifications may change without notice. Contact Marvell Field Application Engineers for more information.
Preliminary Information	This document contains preliminary data, and a revision of this document will be published at a later date. Specifications may change without notice. Contact Marvell Field Application Engineers for more information.
Final Information	This document contains specifications on a product that is final release. Specifications may change without notice. Contact Marvell Field Application Engineers for more information.
Revision Code: Rev. D	
Advance	Technical Publication: 1.1

Description

The 88PL810/88PL815/88PL830 devices are high current ultra-low-dropout linear (LDO) regulators, featuring up to 235 mV @ 3A dropout voltage and very low ground current. Quiescent current is typically 1.5 mA and drops to 0.1 µA in shutdown. The 88PL810/88PL815/88PL830 incorporate several features not commonly found in other LDO's. The devices protect themselves from short circuit conditions by turning OFF and ON ("hiccup"), thereby limiting temperature rise. In "Hot-Swap" applications, no additional circuitry is required since the 88PL810/88PL815/88PL830 devices have an integrated "Soft Start" mode. Additionally, a unique output voltage programming technique is used requiring a single resistor (R_{VSET}) to provide eight output voltage options.

The 88PL830 device's output voltage can be adjusted to 8 different levels between 2.4V and 2.75V (2% or 50 mV per step), for an input voltage range of 2.7V to 3.6V. This voltage is defined by the user with a single external resistor. The 88PL810 device is adjustable in 30 mV steps and the 88PL815 device is adjustable in 36 mV steps.

The 88PL810/88PL815/88PL830 devices are stable with a 10 µF ceramic output capacitor. However, any other type of capacitor up to 1000 µF can be placed in parallel with it as long as the 10 µF ceramic output capacitor is placed next to the 88PL810/88PL815/88PL830.

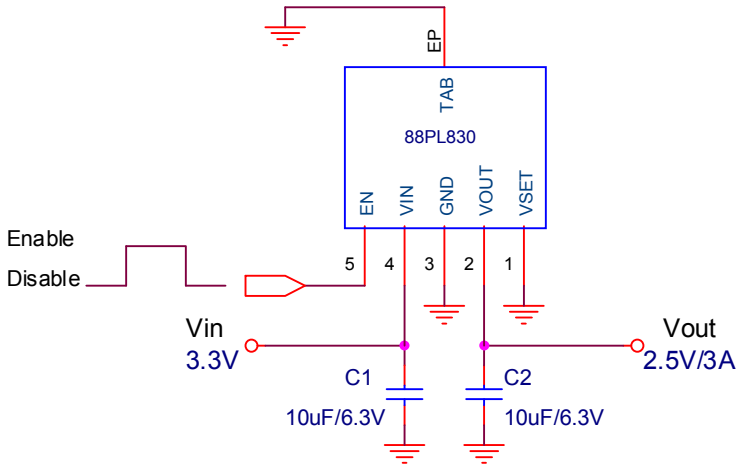
The "Hiccup" short-circuit protection is a feature that is not common among other LDO's. When the 88PL810/88PL815/88PL830 senses a prolong over-current condition, it shuts off for about 6 ms and then tries to start up again. This minimizes the thermal stress on the 88PL810/88PL815/88PL830 devices and reduces the current draw from the input supply in over-current situations.

Features

- 88PL810: 1.5V/1.0A
- 88PL815: 1.8V/1.5A
- 88PL830: 2.5V/3.0A
- Ultra-low dropout (235 mV @ 3A typ.)
- Input voltage range 2.7V to 3.6V
- One resistor sets the output voltage level
- Fixed Soft start ramp with any output capacitor up to 1000 µF
- "Hiccup" short circuit protection
- Stable with ceramic output capacitors
- Adjustable 8 level, programmable output voltage in 2% steps
- Logic controlled shutdown
- 0.1 µA supply current in shutdown
- Stable with 0A load current
- Lead-free packages
- Low profile DPAK (T0-252) and QFN-5L packages
- -40°C to +125°C junction temperature range

Applications

- Adjustable linear regulator for low-voltage digital IC
- PC add-in cards
- High efficiency linear power supplies
- Portable communication devices
- Backup power supplies
- 3.3V PCI Express Bus



Typical LDO Regulator

Section 1. Signal Description

1.1 Pin Configuration

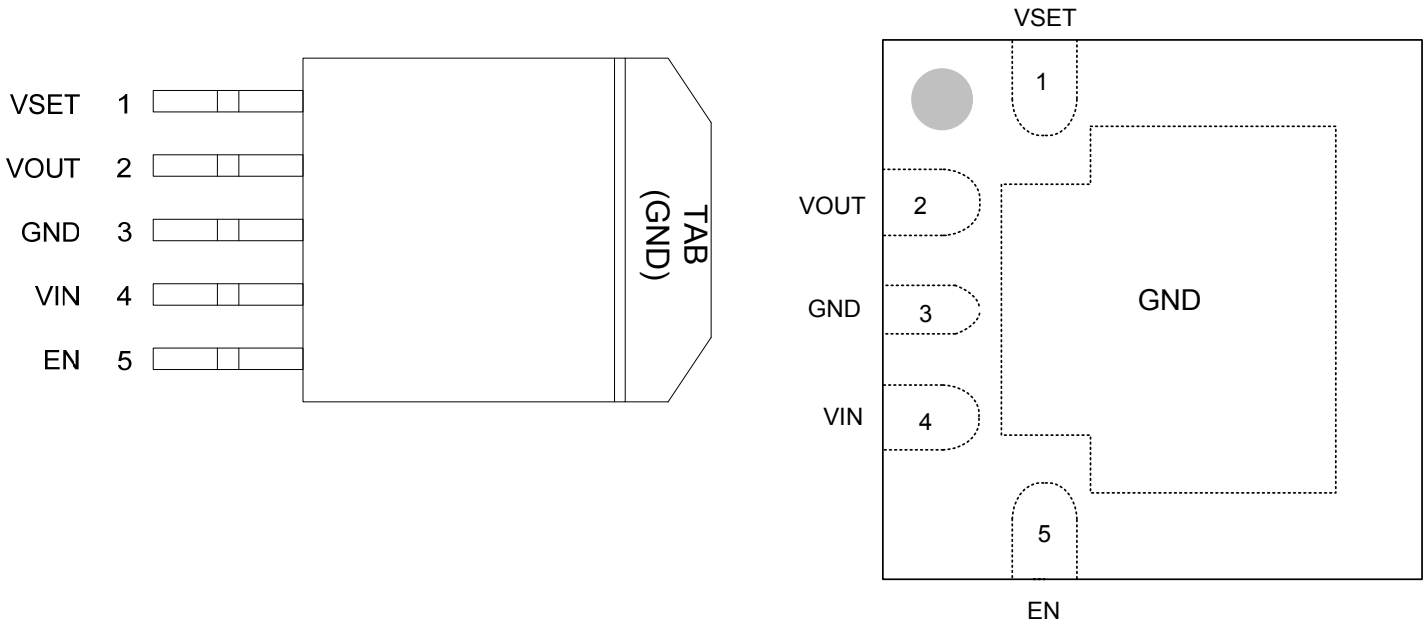


Figure 1: DPAK (left) and 5 x 5 mm QFN-5L – Top View

Table 1: Product Table		
Part Number	**Output Voltage**	**Output Current**
88PL830	2.40, 2.45, **2.50**[1], 2.55, 2.60, 2.65, 2.70, 2.75	3.0A
88PL815	1.728, 1.764, **1.80**, 1.836, 1.872, 1.908, 1.944, 1.980	1.5A
88PL810	1.44, 1.47, **1.50**, 1.53, 1.56, 1.59, 1.62, 1.65	1.0A

[1] Bold = If Vset is tied to ground then the Bold indicates the output voltage.

1.2 Pin Description

1.2.1 Pin Types

This section provides the pin description of the 88PL810/88PL815/88PL830 devices. Table 2 shows the pin types used in Table 3.

Table 2: Pin Type Definitions

Pin Type	Definition
I	Input only
O	Output only
S	Supply
NC	Not Connected
GND	Ground

Table 3: Pin Description

Pin #	Pin Name	Pin Type	Pin Function
1	VSET	I	Connect to an external resistor that is connected to ground to set the output voltage of the regulator. See the "Electrical Characteristics" table for resistor values and Output Voltage Setting section. The total capacitance across this pin and GND should be equal to 25pF or less. Use a resistor with tolerance better than 2%. If this pin is connected to GND, the output voltage will be set to 2.5V (88PL830), 1.8V (88PL815), or 1.5V (88PL810). Do not float this pin.
2	VOUT	0	Output Voltage: Adjustable regulator output. A 10uF capacitor is connected between this pin and the GND pin.
3	GND	GND	Ground: Tab is connected to GND.
4	VIN	S	Input Voltage: Input voltage supplies current to output. Connect a 10 μF decouple capacitor (C_{IN}) between this pin and GND pin.
5	EN	I	Enable: CMOS compatible input. Logic low = Disable, Logic high = Enable.

Section 2. Electrical Specifications

2.1 Absolute Maximum Ratings[1]

Parameter	Symbol	Range	Units
Input Voltage to GND	V_{IN}	-0.6 to 4.2	V
Enable voltage (V_{EN}) to GND	V_{EN}	-0.6 to max (V_{IN} + 0.6, 4.2)	V
Voltage Set to GND	V_{SET}	-0.6 to max (V_{IN} + 0.6, 4.2)	V
Output Voltage to GND	V_{OUT}	-0.6 to max (V_{IN} + 0.6, 4.2)	V
Operating Temperature Range[2]	T_{OP}	-40 to 85	°C
Storage Temperature Range	T_{STOR}	-65 to 150	°C
Maximum Junction Temperature	T_{JMAX}	125	°C
ESD Rating[3]		2	kV

1. Exceeding the absolute the maximum rating may damage the device.
2. Specifications over the –40°C to 85°C operating temperature ranges are assured by design, characterization and correlation with statistical process controls.
3. Devices are ESD sensitive. Handling precautions recommended. Human Body model, 1.5 kΩ, in series with 100 pF.

2.2 Recommended Operating Conditions[1]

Parameter	Symbol	Range	Units
Input Voltage	V_{IN}	2.7 to 3.6	V
DPAK Package Thermal Resistance	θ_{JA}	See section 5	°C/W
5 X 5 mm QFN-5L Package Thermal Resistance	θ_{JA}	See section 5	°C/W

1. This device is not guaranteed to function outside the specified operating range

2.3 Electrical Characteristics

The following table applies unless otherwise noted: C_{IN} = 10 uF; C_{OUT} = 10 uF (Ceramic); I_{OUT} = 10 mA; T_A = 25°C; V_{IN}=3.3V. **Bold values indicate -40°C ≤ T_A ≤ 85°C.**

Parameter	Symbol	Conditions	Min	Typ	Max	Units
Input Voltage Range	V_{IN}		2.7		3.6	V
Output Voltage Accuracy	V_{OUT}	1mA ≤ I_{OUT} ≤ 3A (88PL830)	-2		2	%
		1mA ≤ I_{OUT} ≤ 1.5A (88PL815)				
		1mA ≤ I_{OUT} ≤ 1A (88PL810)				
Output Voltage Load Regulation	$\Delta V_{OUT}/V_{OUT}$	10mA ≤ I_{OUT} ≤ 3A (88PL830)		0.1		%
		10mA ≤ I_{OUT} ≤ 1.5A (88PL815)				
		10mA ≤ I_{OUT} ≤ 1A (88PL810)				
Output Voltage Line Regulation	$\Delta V_{OUT}/V_{OUT}$	V_{IN} = 3.0V-3.6V, I_{OUT} = 10 mA		0.01		%
Dropout Voltage (88PL830 only)	V_{IN}-V_{OUT}	I_{OUT} = 1A, Output voltage variation=1%		75		mV
		I_{OUT} = 2A, Output voltage variation=1%		156		mV
		I_{OUT} = 3A, Output voltage variation=1%		235		mV
Quiescent Current (88PL810)	I_Q	I_{OUT} = 0mA		1.0		mA
Quiescent Current (88PL815)				1.2		
Quiescent Current (88PL830)				1.5		
Shutdown Input Current	I_{SHDN}	V_{EN} = GND		0.1	50	µA
Output Current Limit (88PL810)	$I_{OUT(LIM)}$	V_{OUT} = 1.5V		3.0		A
Output Current Limit (88PL815)		V_{OUT} = 1.8V		3.0		A
Output Current Limit (88PL830)		V_{OUT} = 2.5V		7.0		A
Enable Input						
Enable Input Logic low	V_{EN}	LDO Shutdown			1.1	V
Enable Input Logic high		LDO Enabled	2.2			V
Enable Pin Input Current	I_{EN}	V_{EL} = 1.1V		1	10	µA
		V_{EH} = 2.2V		1	10	µA

Parameter	Symbol	Conditions	Min	Typ	Max	Units
Under Voltage Lockout						
Under Voltage Lockout	V_{UVLO}	High threshold (UTH), V_{IN} increasing		2.60	2.70	V
		Low threshold (LTH), V_{IN} decreasing		2.45		V
Under Voltage Lockout Hysteresis				150		mV
LDO Output Voltage						
Output Voltage (88PL830)		R_{SET} = 11 KΩ	2.352	2.40	2.448	V
		R_{SET} = 18.7 KΩ	2.401	2.45	2.499	V
		R_{SET} = 31.6 KΩ or 0Ω	2.450	2.50	2.550	V
		R_{SET} = 53.6 kΩ	2.499	2.55	2.601	V
		R_{SET} = 97.6 kΩ	2.548	2.60	2.652	V
		R_{SET} = 165 kΩ	2.597	2.65	2.703	V
		R_{SET} = 280 kΩ	2.646	2.70	2.754	V
		R_{SET} = 475 kΩ	2.695	2.75	2.805	V
Output Voltage (88PL815)		R_{SET} = 11 kΩ	1.693	1.728	1.763	V
		R_{SET} = 18.7 kΩ	1.729	1.764	1.799	V
		R_{SET} = 31.6 kΩ or 0Ω	1.764	1.800	1.836	V
		R_{SET} = 53.6 kΩ	1.799	1.836	1.873	V
		R_{SET} = 97.6 kΩ	1.835	1.872	1.909	V
		R_{SET} = 165 kΩ	1.870	1.908	1.946	V
		R_{SET} = 280 kΩ	1.905	1.944	1.983	V
		R_{SET} = 475 kΩ	1.940	1.980	2.020	V
Output Voltage (88PL810)		R_{SET} = 11 kΩ	1.411	1.44	1.469	V
		R_{SET} = 18.7 kΩ	1.441	1.47	1.499	V
		R_{SET} = 31.6 kΩ or 0Ω	1.470	1.50	1.530	V
		R_{SET} = 53.6 kΩ	1.499	1.53	1.561	V
		R_{SET} = 97.6 kΩ	1.529	1.56	1.591	V
		R_{SET} = 165 kΩ	1.558	1.59	1.622	V
		R_{SET} = 280 kΩ	1.588	1.62	1.652	V
		R_{SET} = 475 kΩ	1.617	1.65	1.683	V

Parameter	Symbol	Conditions	Min	Typ	Max	Units
Soft Start						
Start-up Time (88PL830)	t_{SS}	V_{OUT} = 2.5V		3	5	ms
Start-up Time (88PL815)		V_{OUT} = 1.8V		2.2		
Start-up Time (88PL810)		V_{OUT} = 1.5V		2.1		
Low Drop Out Auto-restart						
LDO Auto-restart		Time to restart after current limit shut down		6	30	ms
Over Temperature Protection						
Over-temperature Protection	T_{OT}	T_J increasing (Disable IC)		150		°C
		T_J decreasing (Enable IC)		120		°C

Section 3. Functional Description

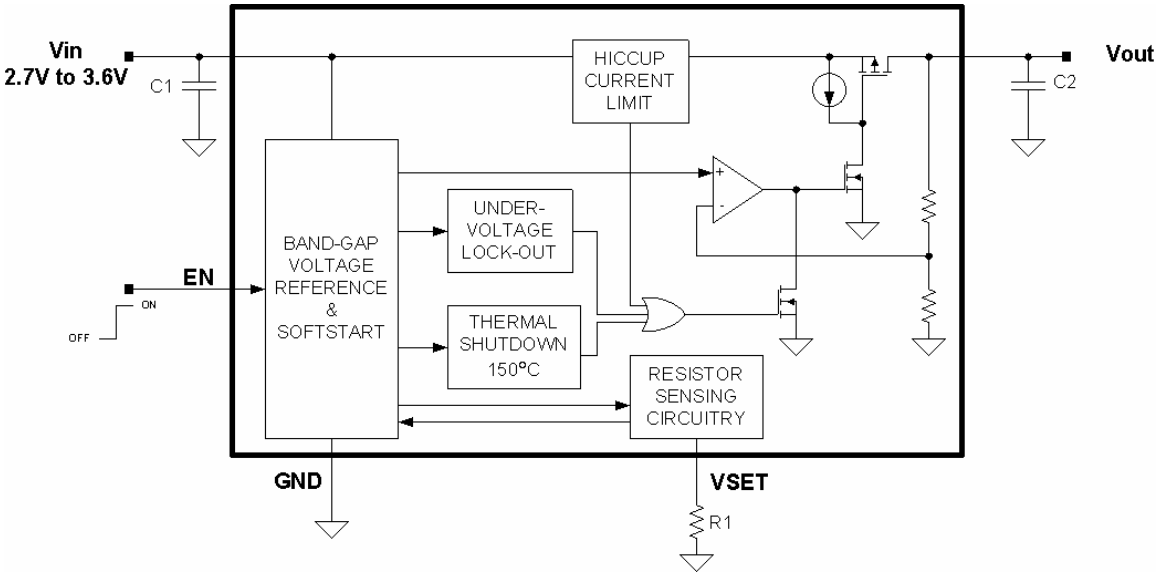


Figure 2: 88PL810/88PL815/88PL830 Simplified Block Diagram

Output Voltage – AnyVoltage ™ Technology

For 88PL830, the output voltage is set by using a single resistor (R_{VSET}) to provide eight output voltage options from 2.40V to 2.75V in 50 mV steps (See Table 4). The R_{SET} resistor is only read once during start-up before the output voltage is turned on; therefore, the output voltage cannot be changed on-the-fly. To configure the output to a different voltage either power has to recycle or the enable input has to turn OFF and back ON.

Table 4

Step	V_{OUT} 88PL830 (V)	V_{OUT} 88PL815 (V)	V_{OUT} 88PL810 (V)	R_{VSET} (kΩ)
1	2.50	1.80	1.50	0
2	2.75	1.980	1.65	475
3	2.70	1.944	1.62	280
4	2.65	1.908	1.59	165
5	2.60	1.872	1.56	97.6
6	2.55	1.836	1.53	53.6
7	2.50	1.80	1.50	31.6
8	2.45	1.764	1.47	18.8
9	2.40	1.728	1.44	11

Figure 3 shows the startup sequence of the 88PL830. Once the input voltage (Vin) is above the under voltage lockout (UVLO) upper threshold (UTH) of 2.65V, the V_{SET} pin becomes active. Current is sourced out of this pin in exponentially increasing steps. After each step there is a blanking time before the V_{SET} voltage is compared to an internal 1.2V reference. If the V_{SET} voltage is below this reference voltage, the current source proceeds to the next set. Once the V_{SET} voltage is above the reference voltage the sequence stops and the output voltage (Vout) is allowed to turn-on. Figure 4 shows the V_{SET} waveform for a 2.5V output. The 88PL830 keeps track of how many steps were required to determine the appropriate output voltage. Table 4 provides the number of steps necessary for each output voltage option. Using a 31.6 kΩ resistor requires the current source to step 7 times, see Figure 4.

Figure 3: Start-Up Sequence

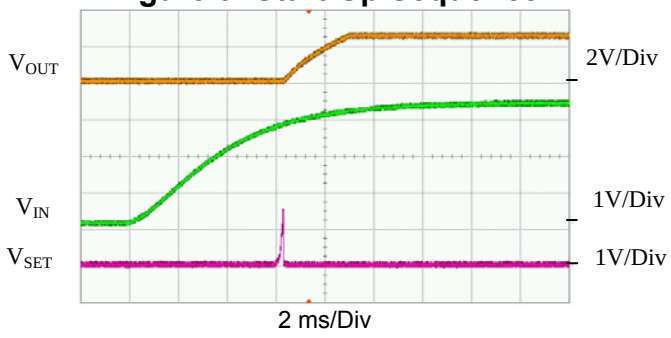
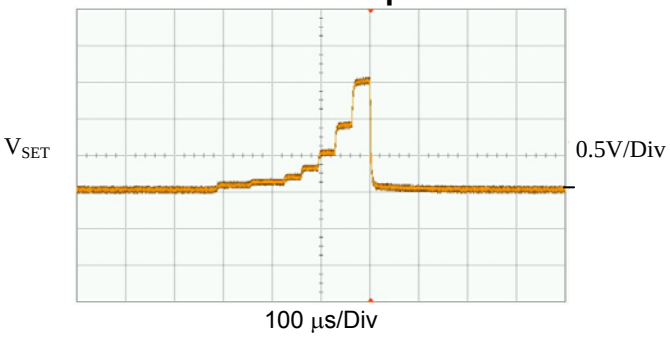


Figure 4: V_{SET} Voltage Steps for 2.5V Output



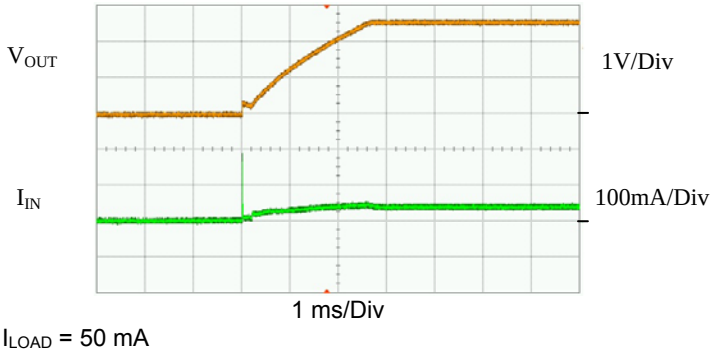
The 88PL810/88PL815/88PL830 devices provide an innovative technique to set the output voltage. The output voltage is determined during startup by the device reading the value of an external resistor that is located outside the regulator's feedback loop. By placing the output voltage-programming resistor outside the regulator's feedback loop, its tolerance does not affect the accuracy of the output voltage. Normally, adjustable regulators use 1% resistors to set the output voltage. However, these resistors are located inside the feedback loop, introducing as much as 2% of initial accuracy error to the output voltage, resulting in an overall initial accuracy of 3%. The 88PL810/88PL815/88PL830 initial accuracy is 2% for any of the eight output voltages.

The V_{SET} pin is sensitive to excessive leakage currents and stray capacitance. The output voltage can potentially be programmed to the lower output voltage if there is contamination that introduces excessive leakage current on the VSET pin, especially for a R_{VSET} of 475kΩ. The parasitic resistance on the node must be greater than 3MΩ and the stray capacitance must be equal to 25pF or less.

Soft Start

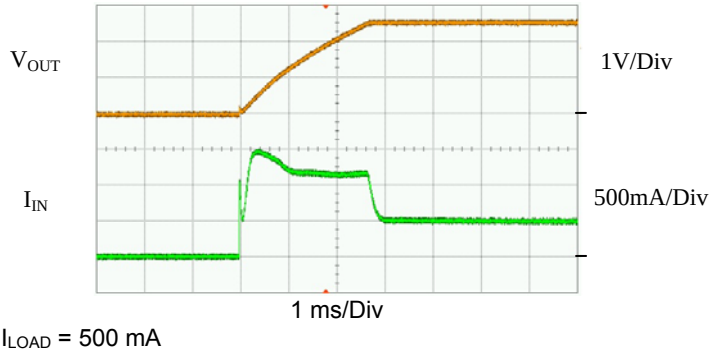
Soft start is a highly desirable property in "Hot-Swap" applications. Most LDOs start-up within 100 us, producing large inrush currents on the input power supply. The 88PL810/88PL815/88PL830 device controls the rise time of the output voltage, thereby dramatically reducing the inrush current. The 88PL830 device rise time is typically 3ms and it is independent of output capacitance and load current. Figure 5 shows the rise time with a 10 uF output capacitor at 50 mA load and Figure 6 shows the rise time with a 1000 uF output capacitor at 500 mA load. Even with these extreme loading conditions and different inrush current, the output voltage rise time difference is less than 0.1 ms. Also note that the output voltage starts at near 0V while other LDO soft start techniques typically start at 1.25V.

Figure 5: Rise Time with C_{OUT} = 10 uF



I_{LOAD} = 50 mA

Figure 6: Rise Time with C_{OUT} = 1000 uF



I_{LOAD} = 500 mA

Hiccup Current Limit

The “Hiccup” short-circuit protection is a feature that is not common among other LDOs. When the current-sense circuit sees an over-current condition, the 88PL810/88PL815/88PL830 device shuts off for about 6 ms and then tries to start up again, see Figure 7. If the over-load condition is removed, the 88PL810/88PL815/88PL830 devices will start-up normally; otherwise, the 88PL810/88PL815/88PL830 device will see another over-current event and shut off again, repeating the previous cycle.

Figure 7: Hiccup Period

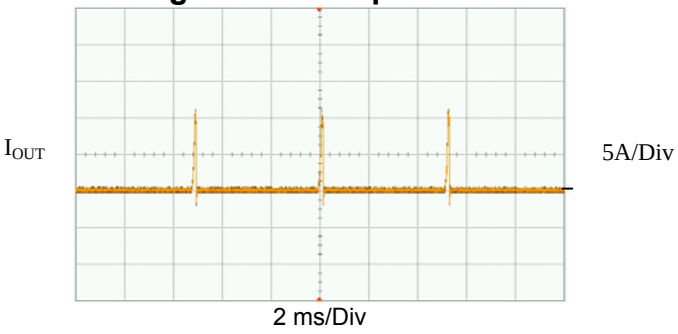


Figure 7

Figure 8: Current Limit Response Time

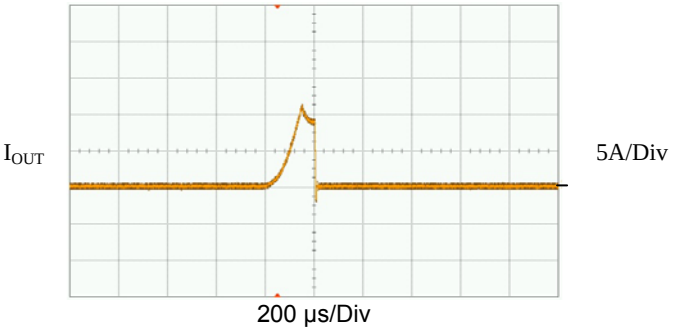


Figure 8

Hiccup mode protection offers protection against over current situations, since it limits the average current to the load at a low level, reducing power dissipation and case temperature of the IC. The 88PL810/88PL815/88PL830 device case temperature will only rise about 20°C and have a case temperature of around 45°C at room, reducing the thermal stress on the device.

Figure 8 shows the response time of the current limit circuitry. The response time of the protection circuit must be quick enough to prevent damage from overloads, yet allow enough time to response to transient loads without prematurely tripping the protection circuit.

Output Capacitor (C_{OUT}) selection

The 88PL810/88PL815/88PL830 device requires a 10 uF ceramic output capacitor as part of the frequency compensation. However, any other type of capacitor up to 1000 uF can be placed in parallel with it as long as the 10uF ceramic output capacitor is placed next to the 88PL810/88PL815/88PL830 device. Additional output capacitance further improves load-transient response and power supply rejection.

X7R and X5R type ceramic capacitors are recommended because of their performance over temperature. Capacitance of the X7R type capacitors changes only 15% over their operating temperature range. Y5V and Z5U type ceramic capacitors change value by as much as 60% and 50%, respectively, over their operating temperature range. If Y5V type ceramic capacitors are used, then higher value capacitor in comparison with X7R and X5R capacitors must be used to ensure a

sufficient capacitance value over the operating temperature range. The following capacitors are some of the capacitors recommended to be used with the 88PL810/88PL815/88PL830.

Table 5: Recommended Capacitors

Manufacturer	Part Number	Dielectric	Capacitance (µF)	Voltage (V)	Case Size (inch)	Max Height (mm)
Murata	GRM188R60G106M	X5R	10	4.0	0603	0.9
Murata	GRM219R60J106K	X5R	10	6.3	0805	0.95
Murata	GRM21BR60J106K	X5R	10	6.3	0805	1.35
Taiyo-Yuden	CE JMK212BJ106MG-T	X5R	10	6.3	0805	1.40
TDK	C2012X5R0J106MT	X5R	10	6.3	0805	1.55

Input Capacitor

An input capacitor of 1 uF or greater is required between the 88PL810/88PL815/88PL830 device's V_{IN} pin and ground. It must be placed as close as possible to the 88PL810/88PL815/88PL830 device for stable operation. While 1 uF will provide adequate bypassing of the V_{IN} supply, larger value input capacitors (10 uF) can improve bypassing to handle fast transient response requirements.

Enable

The 88PL810/88PL815/88PL830 devices feature an active high enable (EN) input that allows ON/OFF control of the device. Near "zero" current drain is achieved when the device is disabled, with only microamperes of leakage current flow. The EN input includes TTL/CMOS compatible thresholds for simple interfacing with logic, or that may be directly tied to V_{IN} for a constant ON state. The enable input must not be left floating; it must be tied either high or low.

Minimum Load Current

The 88PL810/88PL815/88PL830 device, unlike most other high current regulators, does not require a minimum load to maintain output voltage regulation.

Undervoltage Lockout (UVLO)

The 88PL810/88PL815/88PL830 incorporates undervoltage-lockout circuitry to disable the LDO when the input voltage is below 2.45V (typical). The LDO is enabled when the input voltage is above 2.60V (typical).

Thermal Shutdown

When the junction temperature of the 88PL810/88PL815/88PL830 device exceeds 150°C (typical), the thermal shutdown circuitry disables the LDO. The LDO is enabled when the junction temperature is decreased to 120°C (typical).

Thermal Considerations

The power handling capability of the device is limited by the maximum rated junction temperature (125°C). The power dissipated by the device is made up of two components:

1. Output current multiplied by the differential of input and output voltage: (I_{OUT}) (V_{IN}-V_{OUT}).
2. Input current into the device (used by internal circuitry in mA) multiplied by the input voltage: (I_Q)(V_{IN})

The actual power dissipation (P_D) will be the sum of the two components listed above:

$$P_D = (I_{OUT}) (V_{IN}-V_{OUT}) + (I_Q) (V_{IN})$$

To determine the maximum power dissipation ($P_{D\,(max)}$) of the package, use the junction-to-ambient thermal resistance (θ_{JA}) of the device and the following equation:

$$P_{D\,(max)} = (T_{J\,(max)}-T_{A\,(max)})/ (\theta_{JA})$$

Where $T_{J\,(max)}$ is the maximum junction temperature of the die (125°C) and $T_{A\,(max)}$ is the ambient operating temperature. Note that θ_{JA} is layout dependent.

A heat sink effectively increases the surface area of the package to improve the flow of heat away from the IC and into the air. Each material in the heat flow between the IC and the outside environment has a thermal resistance. Starting from the die, we have θ_{JC} (junction to case), θ_{CS} (case to heat sink), and θ_{SA} (heat sink to ambient). These thermal resistances are added together to determine the total thermal resistance between the die and the air, θ_{JA}.

$$\theta_{JA} = \theta_{JC} + \theta_{CS} + \theta_{SA}$$

The value for θ_{SA} is dependent on the heat sink, where the θ_{CS} is dependent on the package type and contact between heat sink and package. The proper heat sink can be selected based on the following equation:

$$\theta_{SA} = \frac{T_{J\,(max)} - T_{A\,(max)}}{P_{D\,(max)}} - (\theta_{JC} + \theta_{CS})$$

The θ_{JA} can be calculated after the proper heat sink is selected.

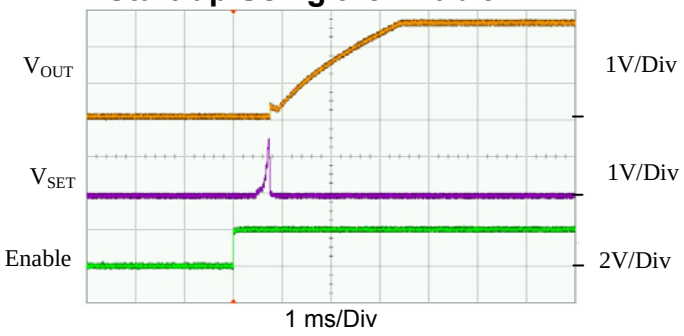
To prevent the device from entering Thermal Shutdown, the actual power dissipation needs to be equal or less than the maximum power dissipation:

$$\frac{T_{J\,(max)} - T_{A\,(max)}}{\theta_{JA}} \geq (I_{OUT})\,(V_{IN} - V_{OUT})$$

Section 4. Functional Characteristics

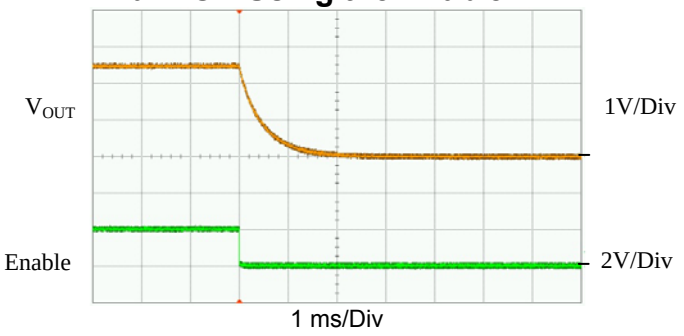
The following is used C_{IN} = 10 uF; C_{OUT} = 10 uF (Ceramic); V_{IN}=3.3V; V_{OUT}=2.5V; unless otherwise noted.

Start-up Using the Enable Pin



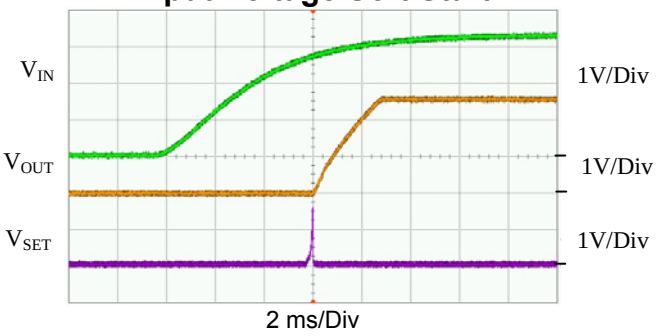
I_{LOAD} = 50Ω

Turn Off Using the Enable Pin



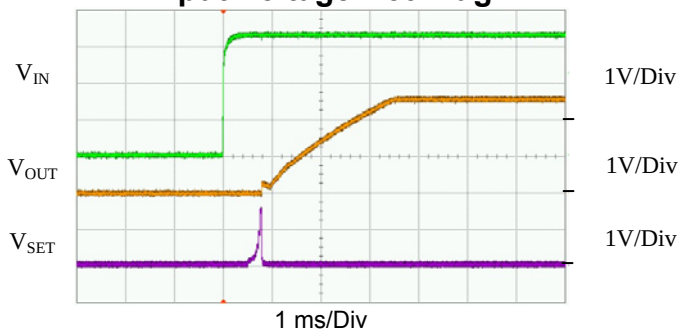
I_{LOAD} = 50Ω

Input Voltage Soft Start



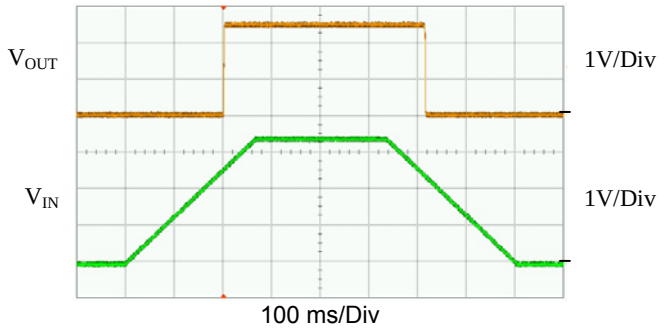
I_{LOAD} = No Load

Input Voltage Hot Plug



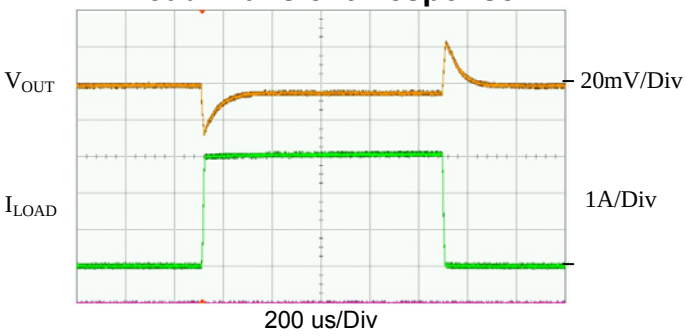
I_{LOAD} = No Load

UVLO Thresholds



V_{HTH} = 2.60V
V_{LTH} = 2.45V

Load Transient Response



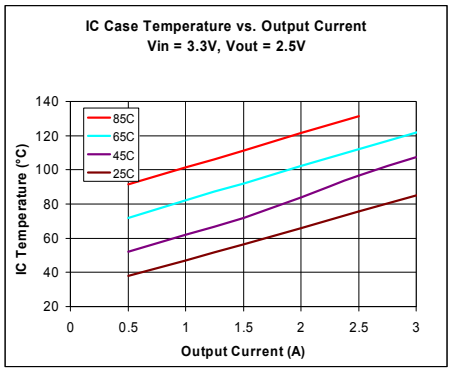
I_{LOAD} = 0.01A to 3.0A C_{OUT} = 10 µF

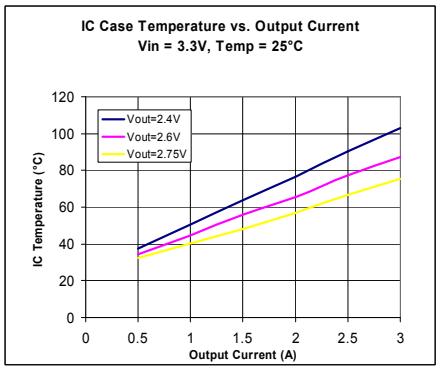
Section 5. Typical Characteristics

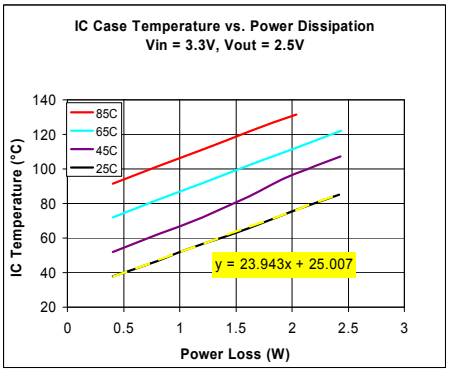
5.1 IC Case and Board Temperature

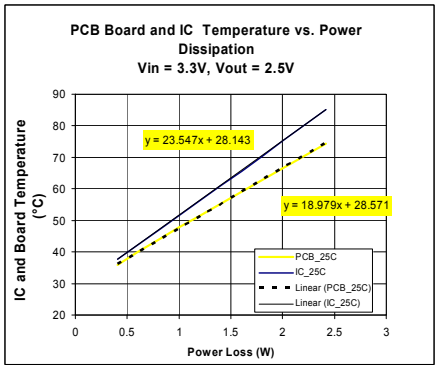
Actual results depend upon the size of the PCB and proximity to other heat emitting components. The following test data used a ¾ in^2 PCB, 1 oz copper, and 88PL830 part.

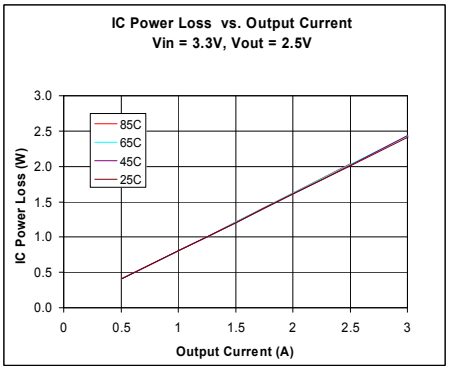
5.1.1 DPAK package

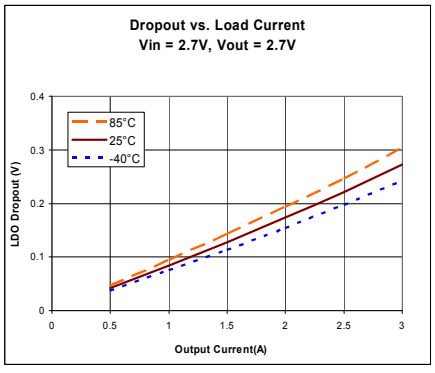






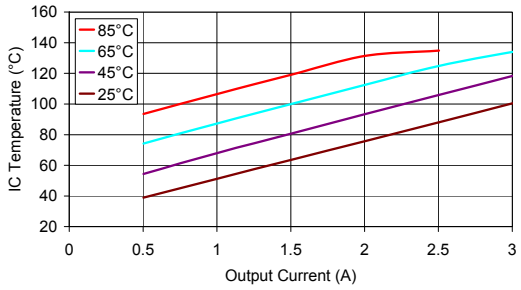




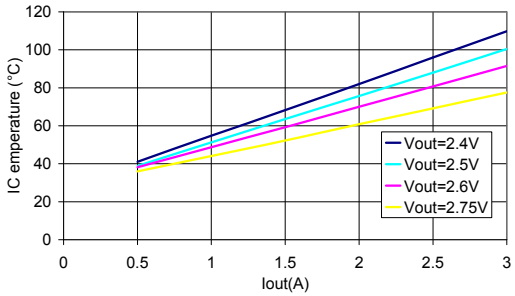


5.1.2 5x5 mm QFN-5L package

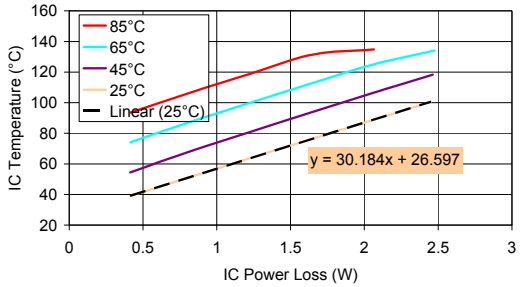
IC Case Temperature vs. Output Current
Vin = 3.3V, Vout = 2.5V



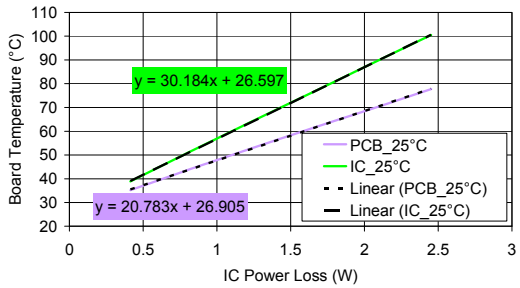
IC Temperature vs. Output Current
Vin = 3.3V, @25C



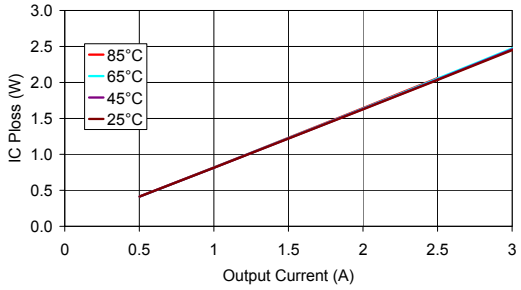
IC Case Temperature vs. Power Dissipation
Vin = 3.3V, Vout = 2.5V



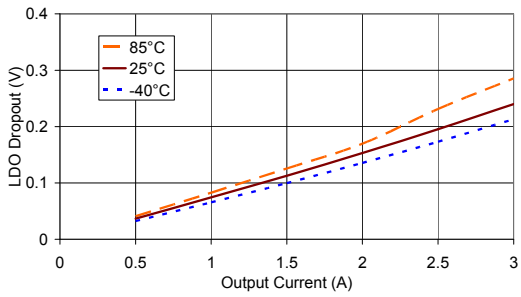
PCB Board and IC Temperature vs. Power Dissipation
Vin = 3.3V, Vout = 2.5V, @ 25°C



IC Power Loss vs. Output Current
Vin = 3.3V, Vout = 2.5V



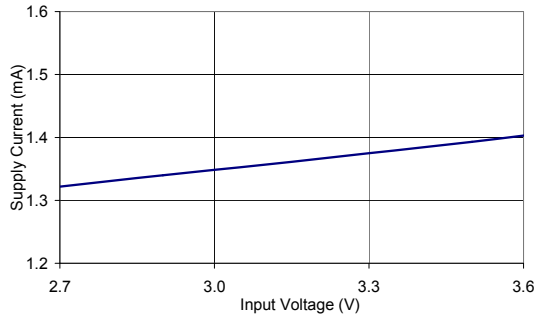
Dropout vs. Load Current
Vin = 2.7, Vout = 2.7V



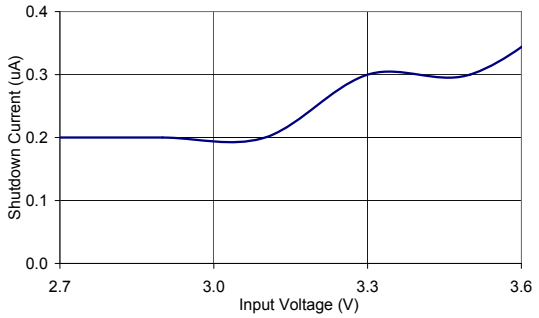
5.2 Input Voltage Graphs

The following data applies to 88PL830; C_{IN} = 10 uF; C_{OUT} = 10 uF (Ceramic); unless otherwise noted.

Supply Current vs. Input Voltage

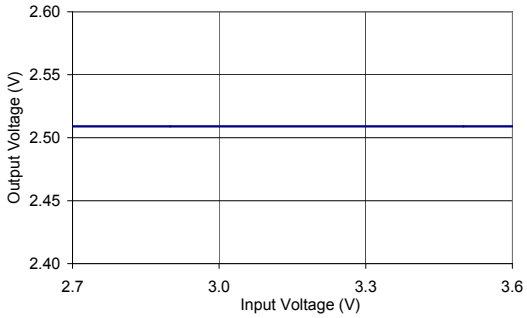


Shutdown Current vs. Input Voltage



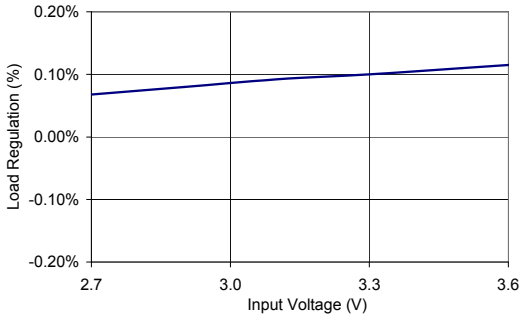
Load = No Load

Output Voltage vs. Input Voltage



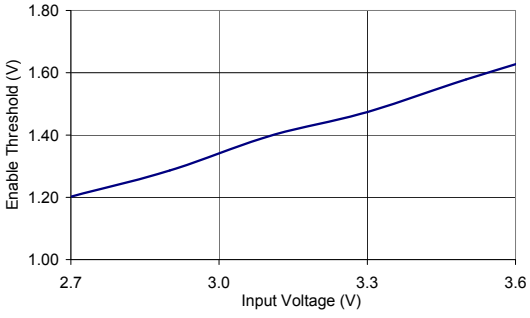
$I_{OUT\ (LDO)}$ = 10 mA

Load Regulation vs. Input Voltage

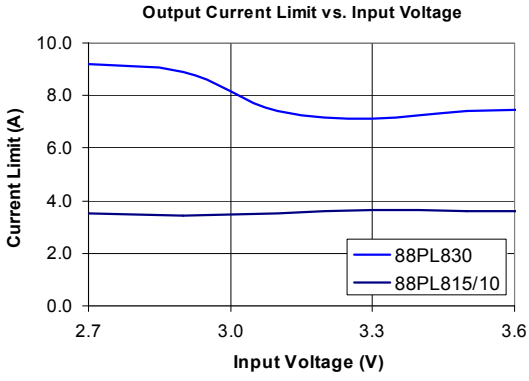


$V_{OUT\ (LDO)}$ = 2.5V
$I_{OUT\ (LDO)}$ = 10 mA – 3.0A

Enable Threshold vs. Input Voltage



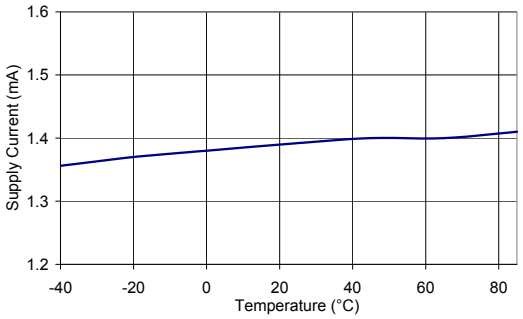
Output Current Limit vs. Input Voltage



5.3 Temperature Graphs

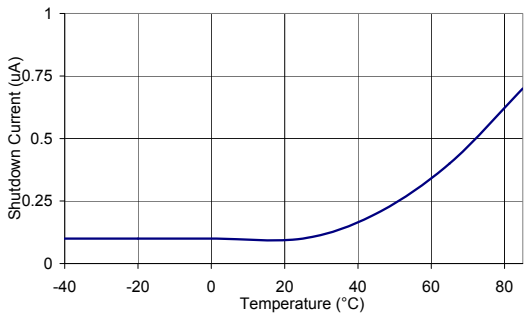
The following data applies to 88PL830; C_{IN} = 10 uF; C_{OUT} = 10 uF (Ceramic); V_{IN}=3.3V; V_{OUT}=2.5V; unless otherwise noted.

Supply Current vs. Temperature



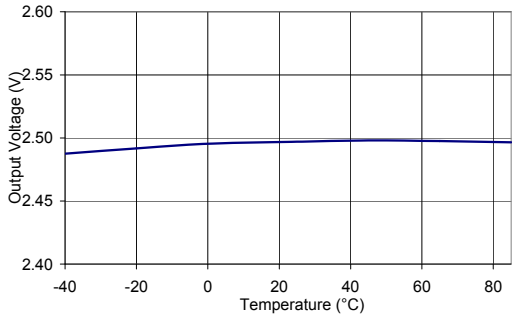
$I_{OUT\ (LDO)}$ = No Load

Shutdown Current vs. Temperature



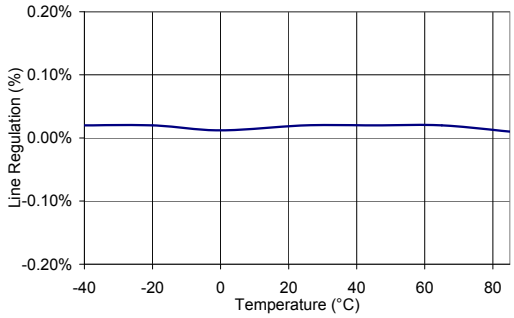
$I_{OUT\ (LDO)}$ = 10mA

Output Voltage vs. Temperature



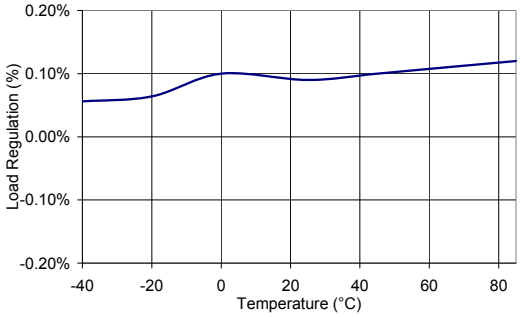
$I_{OUT\ (LDO)}$ = 10 mA

Line Regulation vs. Temperature



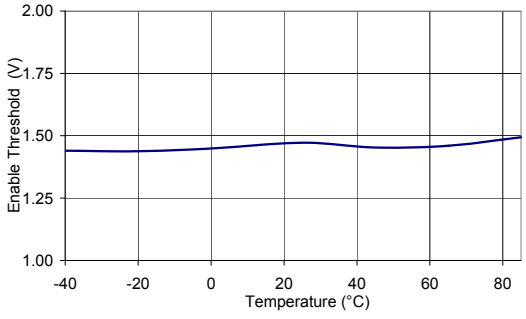
V_{IN} = 3.0V – 3.6V $I_{OUT\ (LDO)}$ = 10 mA

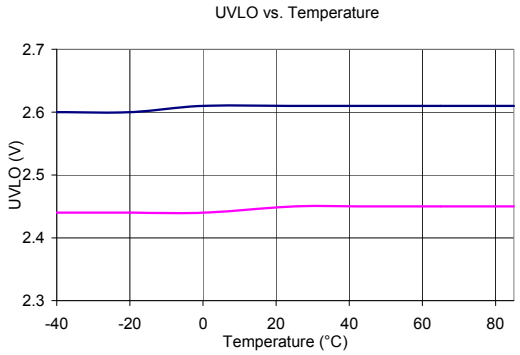
Load Regulation vs. Temperature

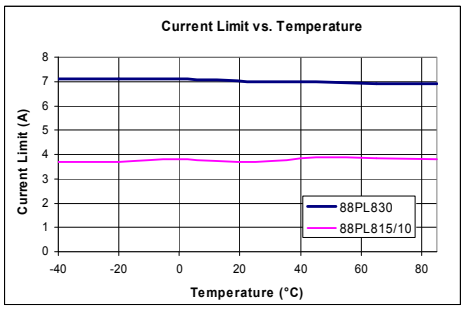


$I_{OUT\ (LDO)}$ = 10 mA – 3A

Enable Threshold vs. Temperature







$I_{OUT\ (LDO)}$ = 10 mA

Section 6. Mechanical Drawings

6.1 Mechanical Dimensions

6.1.1 DPAK Package

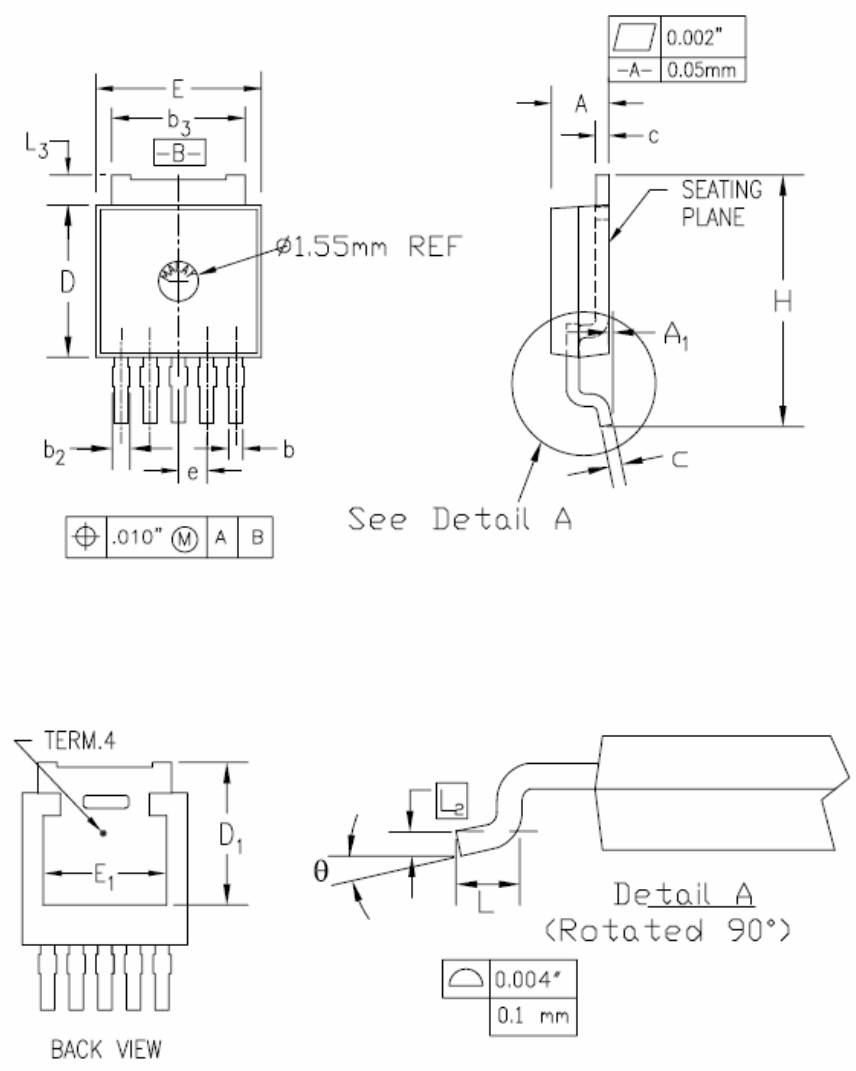


Figure 9: 88PL810/88PL815/88PL830 DPAK mechanical Dimensions

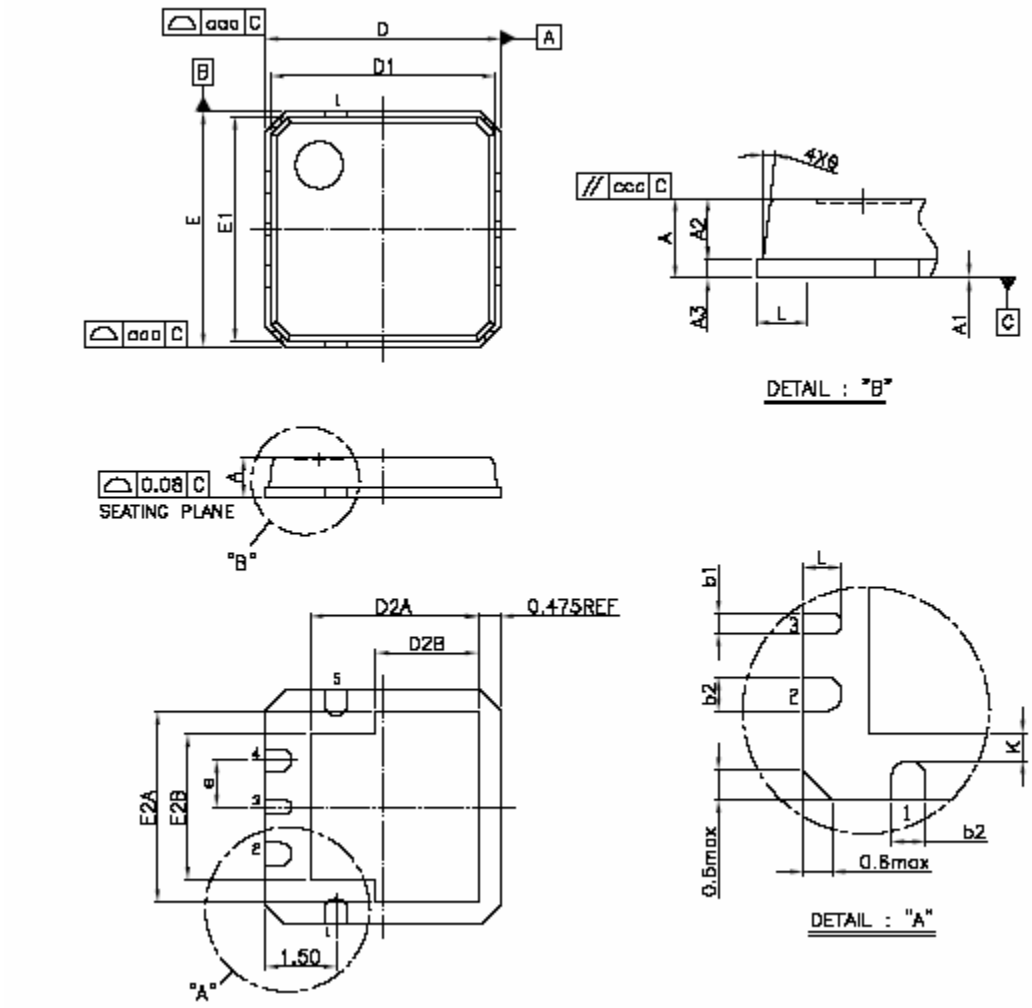
Table 6: DPAK Dimensions

SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN.	MAX.	MIN.	MAX.	
A	0.086	0.094	2.19	2.38	
A_1	–	0.005	–	0.13	
b	0.017	0.027	0.43	0.69	
b_2	0.022	0.032	0.56	0.81	
b_3	0.205	0.215	5.21	5.46	
c	0.018	0.024	0.46	0.61	
D	0.235	0.245	5.97	6.22	
D_1	0.205	–	5.21	–	2
E	0.250	0.265	6.35	6.73	
E_1	0.190	–	4.83	–	2
e	0.045 BSC		1.14 BSC		
H	0.380	0.410	9.65	10.41	
L	0.055	0.070	1.40	1.78	4
L_2	0.020 BSC		0.51 BSC		
L_3	0.035	0.050	0.89	1.27	
θ	0°	8°	0°	8°	

NOTES:

1. No current JEDEC outline, all dimensions stated above are identical to Chippac's 3L TO252AA except the lead dimensions.
2. D_1 and E_1 dimensions establish a minimum mounting surface for terminal 4.
3. L is the terminal length for soldering.
4. Controlling dimension: Inch.

6.1.2 5 X 5 mm QFN-5L Package



Note:

1. Controlling Dimension: Millimeter
2. Reference Document: JEDEC MO-229

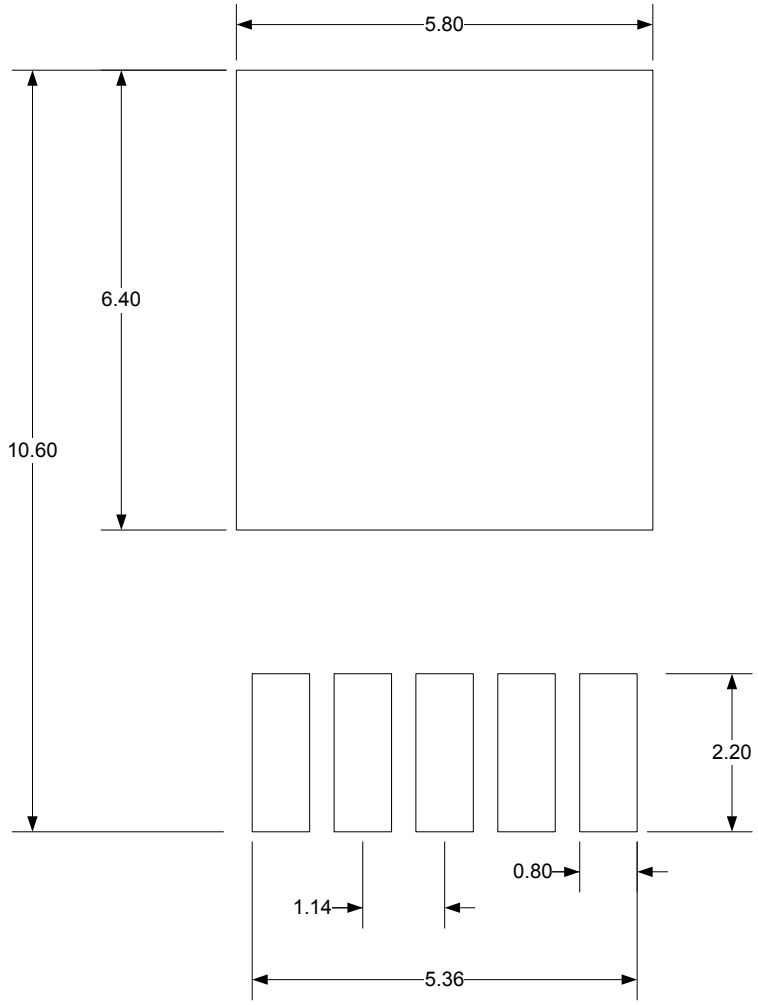
Figure 10: 88PL810/88PL815/88PL830 5X5 mm QFN-5L mechanical Dimensions

Table 7: 5 X 5 mm QFN-5L Dimensions

Symbol	Dimension in mm			Dimension in inch		
	MIN	NOM	MAX	MIN	NOM	MAX
A	0.80	0.85	1.00	0.031	0.033	0.039
A1	0.00	0.02	0.05	0.00	0.001	0.002
A2	0.60	0.65	0.50	0.024	0.026	0.031
A3	0.020 REF			0.008 REF		
b1	0.25	0.30	0.35	0.010	0.012	0.014
B2	0.45	0.50	0.55	0.018	0.020	0.022
D/E	5.00 BSC			0.197 BSC		
D1/E1	4.95 BSC			0.187BSC		
D2A	3.43	3.58	3.73	0.135	0.141	0.147
D2B	2.03	2.18	2.33	0.080	0.086	0.092
E2A	3.90	4.05	4.20	0.154	0.159	0.165
E2B	2.95	3.10	3.25	0.116	0.122	0.128
e	1.00 BSC			0.039 BSC		
L	0.35	0.55	0.75	0.014	0.022	0.030
K	0.20	---	---	0.008	---	---
ϴ	0°	---	12°	0°	---	12°
aaa	---	---	0.15	---	---	0.006
bbb	---	---	0.10	---	---	0.004
ccc	---	---	0.10	---	---	0.004
ddd	---	---	0.05	---	---	0.002

6.2 Typical Pad Layout Dimensions

6.2.1 Recommended Solder Pad Layout for DPAK-5 (T0-252)

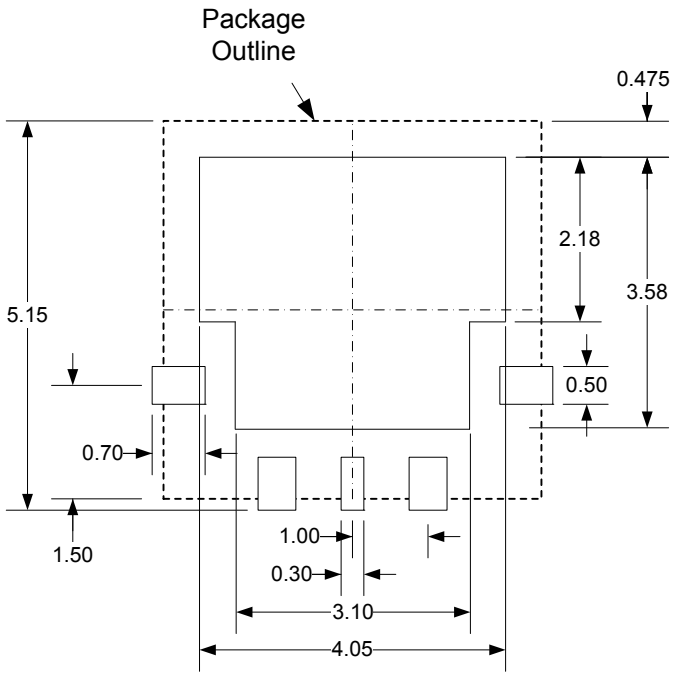


DPAK-5L
Land Pattern (mm)

Notes:

1. Top View
2. Drawing Not to Scale
3. Dimensions are in millimeters
4. Tolerance ± 0.05 mm

6.2.2 Recommended Solder Pad Layout for QFN-5



5X5 QFN-5L
Land Pattern (mm)

Notes:

1. Top View
2. Drawing Not to Scale
3. Dimensions are in millimeters
4. Tolerance ± 0.05 mm

Section 7. Ordering Information

7.1 Ordering Part Numbers and Package Markings

Figure 11 shows the ordering part numbering scheme of the 88PL810/88PL815/88PL830. For complete information, contact Marvell FAE or sales representative.

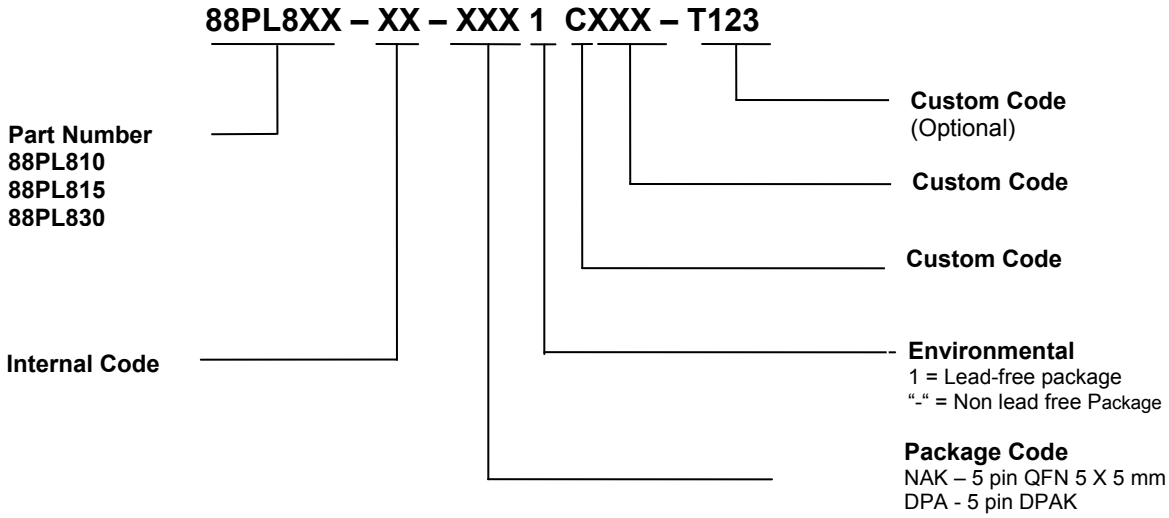


Figure 11: Ordering Part Numbers and Package Markings

7.2 Sample Ordering Part Number

The standard ordering part numbers for the respective solutions are as follows:

Marketing Part Number	Marking	LDO Output Voltage	LDO Output Current	Ambient Temperature Range1	Package2
88PL810-NAK1	L10	1.5V	1.0A	-40°C to 85°C	5 x 5 QFN-5
88PL815-NAK1	L15	1.8V	1.5A	-40°C to 85°C	5 x 5 QFN-5
88PL830-NAK1	L30	2.5V	3.0A	-40°C to 85°C	5 x 5 QFN-5
88PL810-DPA1	L10	1.5V	1.0A	-40°C to 85°C	DPAK-5
88PL815-DPA1	L15	1.8V	1.5A	-40°C to 85°C	DPAK-5
88PL830-DPA1	L30	2.5V	3.0A	-40°C to 85°C	DPAK-5

1. Specifications over the –40°C to 85°C operating temperature range are assured by design, characterization and correlation with statistical process controls.
2. Package dimensions are in mm.

7.3 Package Marking

Figures 12 and 13 show a typical package marking and pin 1 location for the 88PL810/88PL815/88PL830 part in 5 X 5 mm QFN-5 and DPAK-5.

7.3.1 5 X 5 QFN-5 Package Marking

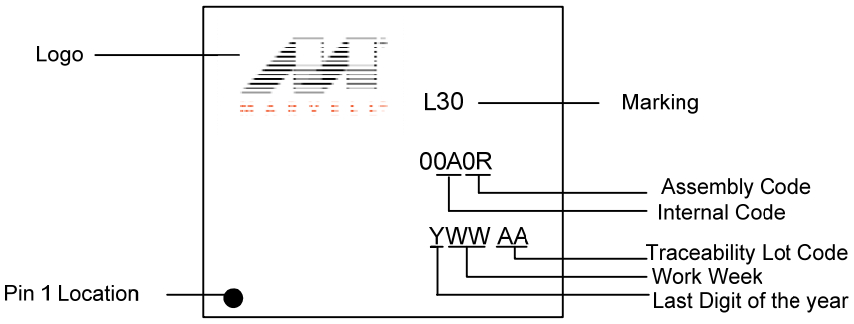


Figure 12: 88PL810/88PL815/88PL830 Package Marking and Pin 1 Location for 5 X 5 mm QFN-5

7.3.2 DPAK-5 Package Marking

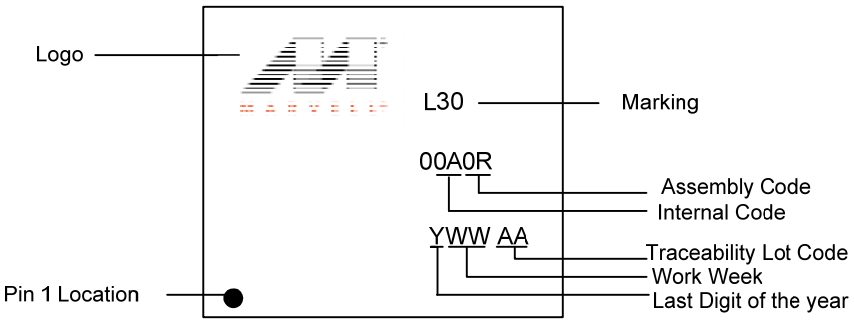


Figure 13: 88PL810/88PL815/88PL830 Package Marking and Pin 1 Location for DPAK-5

MARVELL

MOVING FORWARD FASTER®

Marvell Semiconductor, Inc.

5488 Marvell Lane
Santa Clara, CA 95054, USA

Tel: 1.408.222.2500
Fax: 1.408.752.9028

www.marvell.com

Worldwide Corporate Offices

Marvell Semiconductor, Inc.
5488 Marvell Lane
Santa Clara, CA 95054, USA
Tel: 1.408.222.2500

Marvell Asia Pte, Ltd.
151 Lorong Chuan, #02-05
New Tech Park, Singapore 555741
Tel: 65.6756.1600
Fax: 65.6756.7600

Marvell Japan K.K.
Shinjuku Center Bldg. 44F
1-25-1, Nishi-Shinjuku, Shinjuku-ku
Tokyo 163-0644, Japan
Tel: 81.(0).3.5324.0355
Fax: 81.(0).3.5324.0354

Marvell Semiconductor Israel, Ltd.
6 Hamada Street
Mordot HaCarmel Industrial Park
Yokneam 20692, Israel
Tel: 972.(0).4.909.1500
Fax: 972.(0).4.909.1501

Marvell Semiconductor Korea, Ltd.
Rm. 603, Trade Center
159-2 Samsung-Dong, Kangnam-Ku
Seoul 135-731, Korea
Tel: 82.(0).2.551-6070/6079
Fax: 82.(0).2.551.6080

Radlan Computer Communications, Ltd.
Atidim Technological Park, Bldg. #4
Tel Aviv 61131, Israel
Tel: 972.(0).3.645.8555
Fax: 972.(0).3.645.8544

Worldwide Sales Offices

Western US
Marvell
5488 Marvell Lane
Santa Clara, CA 95054, USA
Tel: 1.408.222.2500
Fax: 1.408.752.9028
Sales Fax: 1.408.752.9029

Central US
Marvell
9600 North MoPac Drive, Suite #215
Austin, TX 78759, USA
Tel: 1.512.343.0593
Fax: 1.512.340.9970

Eastern US/Canada
Marvell
Parlee Office Park
1 Meeting House Road, Suite 1
Chelmsford, MA 01824 , USA
Tel: 1.978.250.0588
Fax: 1.978.250.0589

Europe
Marvell
5 Marchmont Gate
Boundary Way
Hemel Hempstead
Hertfordshire, HP2 7SF
United Kingdom
Tel: 44.(0).1442.211588
Fax: 44.(0).1442.211543

Israel
Marvell
6 Hamada Street
Mordot HaCarmel Industrial Park
Yokneam 20692, Israel
Tel: 972.(0).4.909.1500
Fax: 972.(0).4.909.1501

China
Marvell
5J1, 1800 Zhongshan West Road
Shanghai, PRC 200233
Tel: 86.21.6440.1350
Fax: 86.21.6440.0799

Marvell
Rm. 1102/1103, Jinbin Fudi Mansion
49 An Ning Zhuang West Rd.
Qing He, Haidian District
Beijing, PRC 100085
Tel: 86.10.8274.3831
Fax: 86.10.8274.3830

Japan
Marvell
Shinjuku Center Bldg. 44F
1-25-1, Nishi-Shinjuku, Shinjuku-ku
Tokyo 163-0644, Japan
Tel: 81.(0).3.5324.0355
Fax: 81.(0).3.5324.0354

Taiwan
Marvell
2Fl., No.1, Alley 20, Lane 407, Sec. 2
Ti-Ding Blvd., Nei Hu District
Taipei, Taiwan, 114, R.O.C
Tel: 886.(0).2.6177.7071
Fax: 886.(0).2.8752.5707

Korea
Marvell
Rm. 603, Trade Center
159-2 Samsung-Dong, Kangnam-Ku
Seoul 135-731, Korea
Tel: 82.(0).2.551-6070/6079
Fax: 82.(0).2.551.6080

For more information, visit our website at: www.marvell.com