# **EURO**QUARTZ

## 8 pin Dual-in-Line

- Frequency range 0.625MHz to 50.0MHz
- **CMOS/TTL Output**
- Supply Voltage 5.0 V or 3.3 VDC .
- **Integrated Phase Jitter 1ps typical**





**G8 VCXO** 

625.0kHz ~ 50.0MHz

#### DESCRIPTION

G8 VCXOs, are packaged in an industry-standard, 8 pin Dual in Line package. Typical phase jitter for G series VCXOs is <1ps, output CMOS/TTL. G series VCXOs use fundamental mode crystal osccillators. Applications include phase lock loop, SONET/ATM, settop boxes, MPEG , audio/video modulation, video game consoles and HDTV.

#### SPECIFICATION

Frequency Range		
Vdd = +3.3VDC:	0.625MHz to 50.0MHz	
Vdd = +5.0VDC:	1.0MHz to 50.0MHz	
Supply Voltage:	+3.3 VDC ±5% or +5.0VDC±5%	
Output Logic:	TTL/HCMOS	
Integrated Phase Jitter:	1.0ps maximum 12kHz to 20MHz	
Period Jitter RMS:	2.0ps typical	
Period Jitter Peak to Peak:	14ps maximum	
Phase Noise:	See table below	
Initial Frequency Accuracy		
Tune to the nominal frequency with:		
+3.3VDC:	$Vc = 1.65V \pm 0.2V$	
+5.0 VDC:	$Vc = 2.5V \pm 0.2V$	
Output Voltage HIGH (1):	90% Vdd minimum	
Output Voltage LOW (0):	10% Vdd maximum	
Control Voltage Centre		
+3.3VDC:	1.65V	
+5.0VDC:	2.5V	
Control Voltage Range		
+3.3VDC:	0.3V to 3.0V	
+5.0VDC:	0.5V to 4.5V	
Dulling Danage		
Pulling Range		
+3.3VDC	±80ppm to ±120ppm (standard)	
	±80ppm to ±150ppm	
+3.3VDC +5.0VDC:	±80ppm to ±150ppm (±200ppm available)	
+3.3VDC +5.0VDC: Temperature Stability:	±80ppm to ±150ppm (±200ppm available) See table	
+3.3VDC +5.0VDC: Temperature Stability: Output Load:	±80ppm to ±150ppm (±200ppm available) See table CMOS = 15pF, TTL = 2 gates	
+3.3VDC +5.0VDC: Temperature Stability: Output Load: Start-up Time:	±80ppm to ±150ppm (±200ppm available) See table CMOS = 15pF, TTL = 2 gates 10ms maximum, 5ms typical	
+3.3VDC +5.0VDC: Temperature Stability: Output Load: Start-up Time: Duty Cycle:	±80ppm to ±150ppm (±200ppm available) See table CMOS = 15pF, TTL = 2 gates 10ms maximum, 5ms typical 50% ±5% measured at 50% Vdd	
+3.3VDC +5.0VDC: Temperature Stability: Output Load: Start-up Time: Duty Cycle: Rise/Fall Times:	±80ppm to ±150ppm (±200ppm available) See table CMOS = 15pF, TTL = 2 gates 10ms maximum, 5ms typical 50% ±5% measured at 50% Vdd 0.7ns typical (15pF load)	
+3.3VDC +5.0VDC: Temperature Stability: Output Load: Start-up Time: Duty Cycle:	±80ppm to ±150ppm (±200ppm available) See table CMOS = 15pF, TTL = 2 gates 10ms maximum, 5ms typical 50% ±5% measured at 50% Vdd 0.7ns typical (15pF load) 10 to 45mA, frequency	
+3.3VDC +5.0VDC: Temperature Stability: Output Load: Start-up Time: Duty Cycle: Rise/Fall Times: Current Consumption:	±80ppm to ±150ppm (±200ppm available) See table CMOS = 15pF, TTL = 2 gates 10ms maximum, 5ms typical 50% ±5% measured at 50% Vdd 0.7ns typical (15pF load) 10 to 45mA, frequency dependent	
+3.3VDC +5.0VDC: Temperature Stability: Output Load: Start-up Time: Duty Cycle: Rise/Fall Times: Current Consumption: Linearity:	±80ppm to ±150ppm (±200ppm available) See table CMOS = 15pF, TTL = 2 gates 10ms maximum, 5ms typical 50% ±5% measured at 50% Vdd 0.7ns typical (15pF load) 10 to 45mA, frequency dependent 10% maximum, 6% typical	
+3.3VDC +5.0VDC: Temperature Stability: Output Load: Start-up Time: Duty Cycle: Rise/Fall Times: Current Consumption: Linearity: Modulation Bandwidth:	±80ppm to ±150ppm (±200ppm available) See table CMOS = 15pF, TTL = 2 gates 10ms maximum, 5ms typical 50% ±5% measured at 50% Vdd 0.7ns typical (15pF load) 10 to 45mA, frequency dependent 10% maximum, 6% typical 10kHz minimum	
+3.3VDC +5.0VDC: Temperature Stability: Output Load: Start-up Time: Duty Cycle: Rise/Fall Times: Current Consumption: Linearity: Modulation Bandwidth: Input Impedance:	±80ppm to ±150ppm (±200ppm available) See table CMOS = 15pF, TTL = 2 gates 10ms maximum, 5ms typical 50% ±5% measured at 50% Vdd 0.7ns typical (15pF load) 10 to 45mA, frequency dependent 10% maximum, 6% typical 10kHz minimum 1 MΩ minimum	
+3.3VDC +5.0VDC: Temperature Stability: Output Load: Start-up Time: Duty Cycle: Rise/Fall Times: Current Consumption: Linearity: Modulation Bandwidth: Input Impedance: Slope Polarity:	±80ppm to ±150ppm (±200ppm available) See table CMOS = 15pF, TTL = 2 gates 10ms maximum, 5ms typical 50% ±5% measured at 50% Vdd 0.7ns typical (15pF load) 10 to 45mA, frequency dependent 10% maximum, 6% typical 10kHz minimum 1 MΩ minimum Monotonic and Positive. (An	
+3.3VDC +5.0VDC: Temperature Stability: Output Load: Start-up Time: Duty Cycle: Rise/Fall Times: Current Consumption: Linearity: Modulation Bandwidth: Input Impedance:	±80ppm to ±150ppm (±200ppm available) See table CMOS = 15pF, TTL = 2 gates 10ms maximum, 5ms typical 50% ±5% measured at 50% Vdd 0.7ns typical (15pF load) 10 to 45mA, frequency dependent 10% maximum, 6% typical 10kHz minimum 1 MΩ minimum Monotonic and Positive. (An increase of control voltage	
+3.3VDC +5.0VDC: Temperature Stability: Output Load: Start-up Time: Duty Cycle: Rise/Fall Times: Current Consumption: Linearity: Modulation Bandwidth: Input Impedance: Slope Polarity:	±80ppm to ±150ppm (±200ppm available) See table CMOS = 15pF, TTL = 2 gates 10ms maximum, 5ms typical 50% ±5% measured at 50% Vdd 0.7ns typical (15pF load) 10 to 45mA, frequency dependent 10% maximum, 6% typical 10kHz minimum 1 MΩ minimum Monotonic and Positive. (An increase of control voltage always increases output	
+3.3VDC +5.0VDC: Temperature Stability: Output Load: Start-up Time: Duty Cycle: Rise/Fall Times: Current Consumption: Linearity: Modulation Bandwidth: Input Impedance: Slope Polarity: (Transfer function)	$\pm$ 80ppm to $\pm$ 150ppm ( $\pm$ 200ppm available) See table CMOS = 15pF, TTL = 2 gates 10ms maximum, 5ms typical 50% $\pm$ 5% measured at 50% Vdd 0.7ns typical (15pF load) 10 to 45mA, frequency dependent 10% maximum, 6% typical 10kHz minimum 1 MΩ minimum 1 MΩ minimum Monotonic and Positive. (An increase of control voltage always increases output frequency.)	
+3.3VDC +5.0VDC: Temperature Stability: Output Load: Start-up Time: Duty Cycle: Rise/Fall Times: Current Consumption: Linearity: Modulation Bandwidth: Input Impedance: Slope Polarity: (Transfer function) Storage Temperature:	±80ppm to ±150ppm (±200ppm available) See table CMOS = 15pF, TTL = 2 gates 10ms maximum, 5ms typical 50% ±5% measured at 50% Vdd 0.7ns typical (15pF load) 10 to 45mA, frequency dependent 10% maximum, 6% typical 10kHz minimum 1 MΩ minimum 1 MΩ minimum Monotonic and Positive. (An increase of control voltage always increases output frequency.) -50° to +100°C	
+3.3VDC +5.0VDC: Temperature Stability: Output Load: Start-up Time: Duty Cycle: Rise/Fall Times: Current Consumption: Linearity: Modulation Bandwidth: Input Impedance: Slope Polarity: (Transfer function)	$\pm$ 80ppm to $\pm$ 150ppm ( $\pm$ 200ppm available) See table CMOS = 15pF, TTL = 2 gates 10ms maximum, 5ms typical 50% $\pm$ 5% measured at 50% Vdd 0.7ns typical (15pF load) 10 to 45mA, frequency dependent 10% maximum, 6% typical 10kHz minimum 1 MΩ minimum 1 MΩ minimum Monotonic and Positive. (An increase of control voltage always increases output frequency.)	

### **FREQUENCY STABILITY**

Stability Code	Stability ±ppm	Temp. Range
А	25	0°~+70°C
В	50	0°~+70°C
С	100	0°~+70°C
D	25	-40°~+85°C
E	50	-40°~+85°C
F	100	-40°~+85°C
If non-standard frequency stability is required		

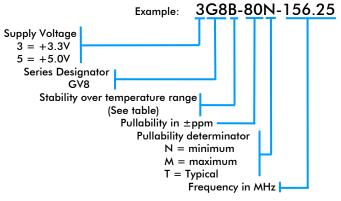
Use 'I' followed by stability, i.e. I20 for ±20ppm

12.8 8 2 ω 2 35 Pin 1 Indicators Ø0.45 leads 4 1 o 3x glass standoffs Ο Pin Connections 62 1 Voltage Control 0 4 Ground, case 8 5 Output 5 7.62 8 Supply Voltage

#### PHASE NOISE

Offset	Frequency 155.25MHz
10Hz	-70dBc/Hz
100Hz	-105dBc/Hz
1kHz	-132dBc/Hz
10kHz	-142dBc/Hz
1MHz	-150dBc/Hz

#### PART NUMBERING



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