Advance Information

256K X28TC256 32K x 8 Bit

Turbo Access E²PROM

FEATURES

- 25ns Access Time
  - —Within 64-Byte Page Boundaries
  - —Page Crossing Status Output—$\overline{WAIT}$
- 5 Volt Byte and Page Alterable
  - —Write From One to Sixty-Four Bytes
  - —Write Time—5ms Max.
  - —Complete Memory Rewrite: 1.3 Sec. Max.
- Early End of Write Detection
  - —DATA Polling
  - —Toggle Bit Polling
  - —Minimize Memory Rewrite: 0.8 Sec. Typical
- Software Data Protection
- Highly Reliable Direct Write™ Cell
  - —Endurance: 10,000 Cycles Per Byte
  - —Data Retention: 100 years

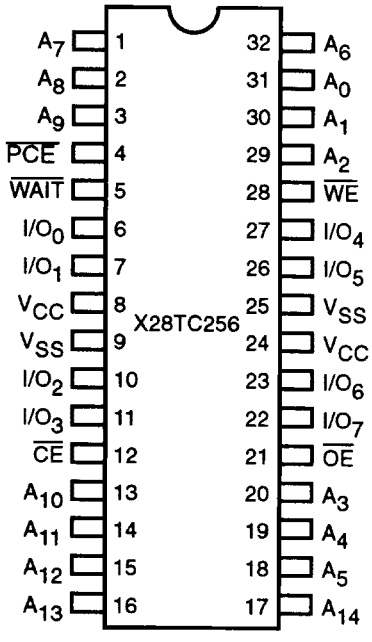
DESCRIPTION

The X28TC256 is a high speed 32K x 8, 5 volt byte alterable nonvolatile memory. It is specially designed to support high speed microprocessors by providing a fast column access time of 25ns for each byte on a 64-byte page. The access time when changing pages will be 150ns maximum. The X28TC256 automatically generates a $\overline{WAIT}$ signal when page boundaries are crossed.

The X28TC256 also features $\overline{DATA}$ Polling and toggle bit polling methods for detecting early end of write. Using either of these polling features, the entire memory can typically be rewritten in 0.8 seconds.

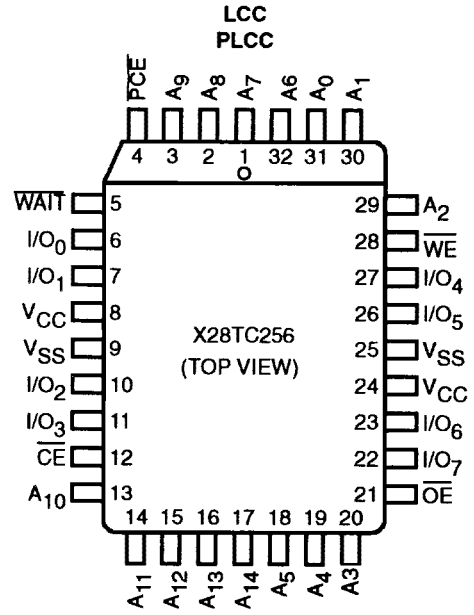
PIN CONFIGURATION

PLASTIC DIP
CERDIP



3860 FHD F02

LCC
PLCC



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PIN DESCRIPTIONS

Addresses (A_0–A_{14})

The Address inputs select an 8-bit memory location during a read or write operation.

Chip Enable ($\overline{CE}$)

The Chip Enable input must be LOW to enable all read/write operations. When $\overline{CE}$ is HIGH, power consumption is reduced.

Output Enable ($\overline{OE}$)

The Output Enable input controls the data output buffers and is used to initiate read operations.

Data In/Data Out (I/O_0–I/O_7)

Data is written to or read from the X28TC256 through the I/O pins.

Write Enable ($\overline{WE}$)

The Write Enable input controls the writing of data to the X28TC256.

Wait For Page Change ($\overline{WAIT}$)

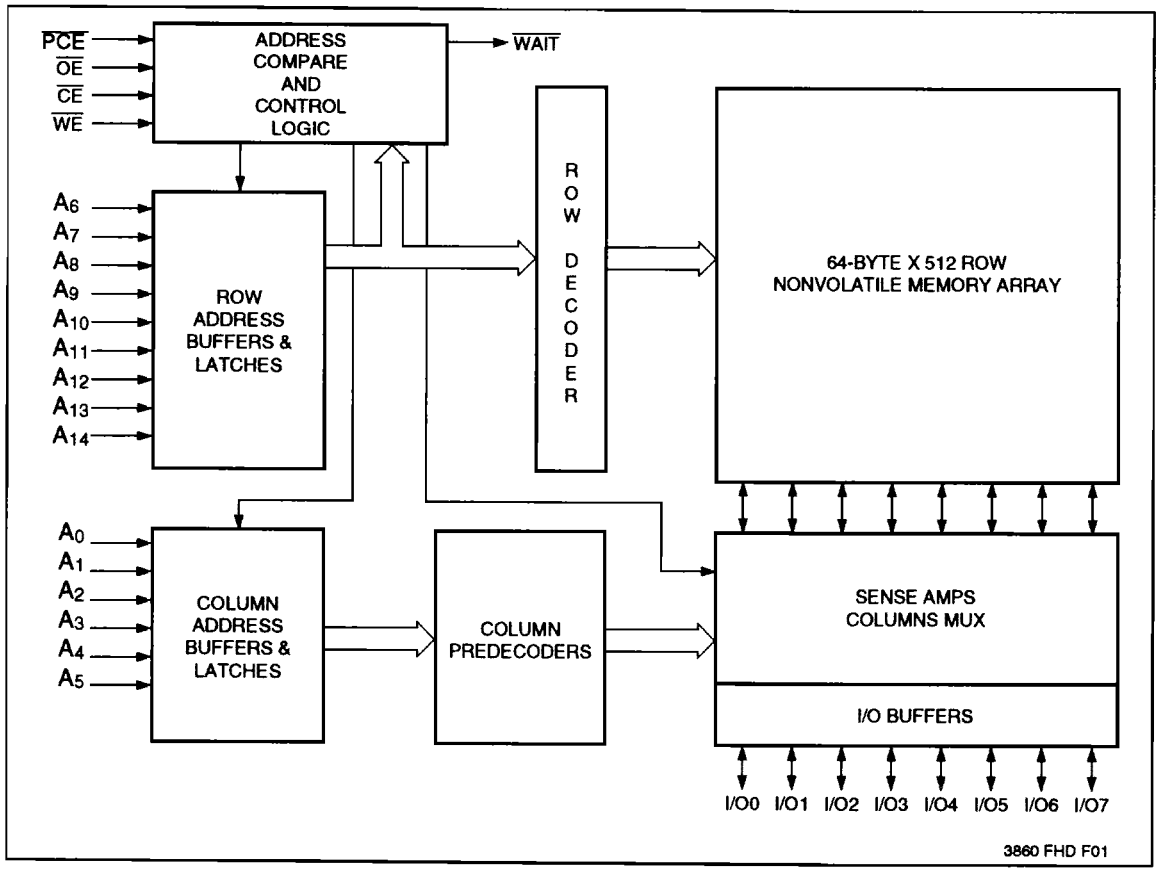
The Wait output notifies the user of a page change.

PIN NAMES

Symbol	Description
A_0–A_{14}	Address Inputs
I/O_0–I/O_7	Data Input/Output
$\overline{WE}$	Write Enable
$\overline{CE}$	Chip Enable
$\overline{OE}$	Output Enable
V_{CC}	+5V
V_{SS}	Ground
NC	No Connect
$\overline{PCE}$	Page Change Enable
$\overline{WAIT}$	Wait for page change

3869 PGM T01

FUNCTIONAL DIAGRAM



DEVICE OPERATION

Read

There are two different read operations in the X28TC256. Page read is when the page address (A_6-A_{14}) is different from the previous page address, and is initiated by $\overline{CE}$ LOW and $\overline{PCE}$ going from HIGH to LOW. The $\overline{OE}$ could go LOW at either the beginning of the read or after $\overline{WAIT}$ goes HIGH. Turbo read is when the page address remains the same and the byte address (A_0-A_5) changes, and it is initiated by both $\overline{OE}$ and $\overline{CE}$ going LOW. Turbo read could be terminated by either $\overline{OE}$ or $\overline{CE}$ going HIGH. The condition of $\overline{PCE}$ input is don't care during turbo read operation; The two-line control architecture ($\overline{CE}$ and $\overline{OE}$) eliminates bus contention in a system environment. The data bus will be in a high impedance state when either $\overline{CE}$ or $\overline{OE}$ is HIGH.

Write

To perform a write to the X28TC256 in byte or page mode, the three byte SDP command sequence must precede any write operation. The command sequence and any data write operation must conform to the write timing requirements. Write operations are initiated when both $\overline{CE}$ and $\overline{WE}$ are LOW *and* $\overline{OE}$ is HIGH. The address is latched by the falling edge of $\overline{WE}$. Similarly, the data is latched internally by the rising edge of $\overline{WE}$. A byte write operation, once initiated, will automatically continue to completion, typically within 3 ms.

Page Write Operation

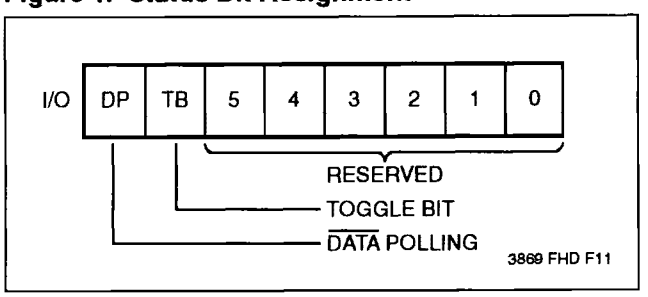
The page write feature of the X28TC256 allows the entire memory to be written in typically 0.8 seconds. Page write allows up to sixty-four bytes of data to be consecutively written to the X28TC256 prior to the commencement of the internal programming cycle. The host can fetch data from another location within the system during a page write operation (change the source address), but the page address (A_6 through A_{14}) for each subsequent valid write cycle to the part during this operation must be the same as the initial page address.

The page write mode can be initiated during any write operation. Following the command sequence and the initial byte write cycle, the host can write an additional sixty-three bytes. Each successive byte load cycle, started by the $\overline{WE}$ HIGH to LOW transition, must begin within 100 µs of the falling edge of the preceding $\overline{WE}$. If a subsequent $\overline{WE}$ HIGH to LOW transition is not detected within 100 µs, the internal automatic programming cycle will commence. There is no page write window limitation. Effectively the page write window is infinitely wide, so long as the host continues to access the device within the byte load cycle time of 100 µs.

Write Operation Status Bits

The X28TC256 provides the user two write operation status bits. These can be used to optimize a system write cycle time. The status bits are mapped onto the I/O bus as shown in Figure 1.

Figure 1. Status Bit Assignment



$\overline{DATA}$ Polling (I/O_7)

The X28TC256 features $\overline{DATA}$ Polling as a method to indicate to the host system that the byte write or page write cycle has been completed. $\overline{DATA}$ Polling allows a simple bit test operation to determine the status of the X28TC256, eliminating additional interrupt inputs or external hardware. During the internal programming cycle, any attempt to read the last byte written will produce the complement of that data on I/O_7 (i.e., write data = 0xxx xxxx, read data = 1xxx xxxx). Once the programming cycle is complete, I/O_7 will reflect true data.

Toggle Bit (I/O_6)

The X28TC256 also provides another method for determining when the internal write cycle is completed. During the internal programming cycle I/O_6 will toggle from one to zero and zero to one on subsequent attempts to read the device. When the internal cycle is complete, the toggling will cease and the device will be accessible for additional read or write operations.

$\overline{DATA}$ POLLING I/O_7

Figure 2. $\overline{DATA}$ Polling Bus Sequence

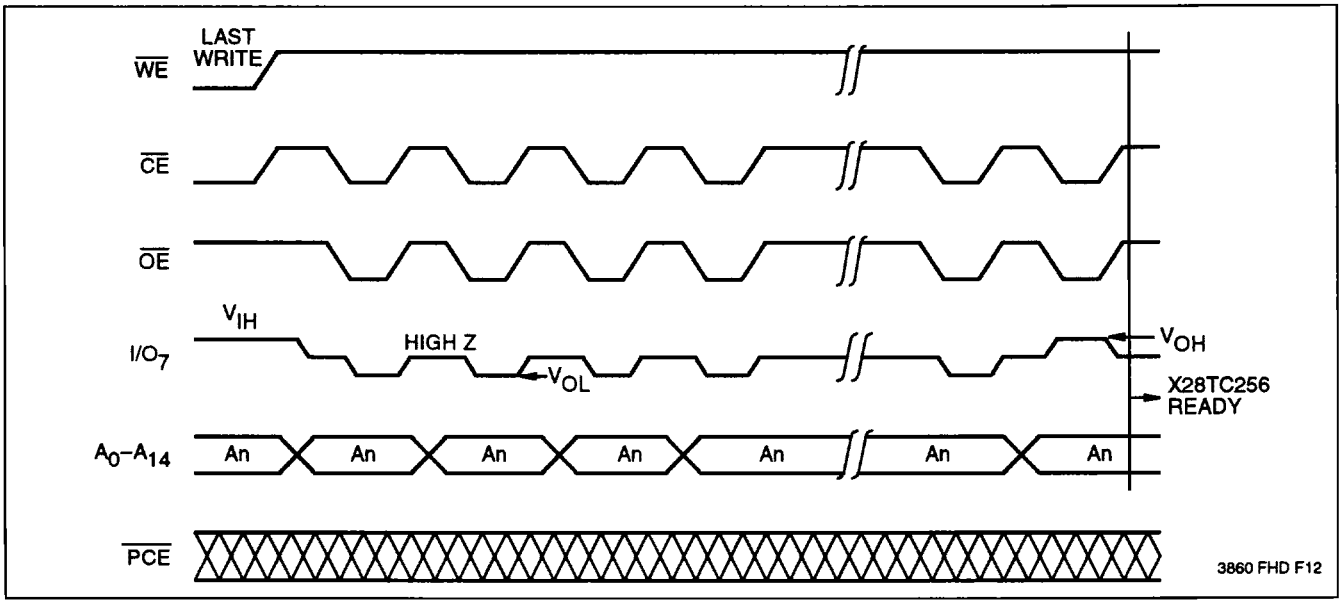
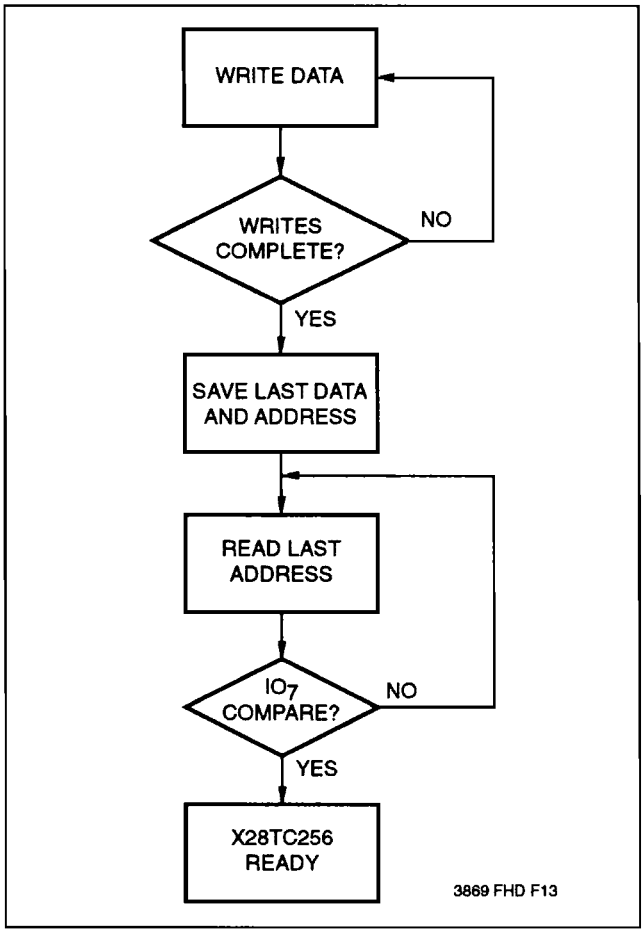


Figure 3. $\overline{DATA}$ Polling Software Flow



$\overline{DATA}$ Polling can effectively reduce the time for writing to the X28TC256. The timing diagram in Figure 2 illustrates the sequence of events on the bus. $\overline{DATA}$ polling is a page read operation. The software flow diagram in Figure 3 illustrates one method of implementing the routine.

THE TOGGLE BIT I/O_6

Figure 4. Toggle Bit Bus Sequence

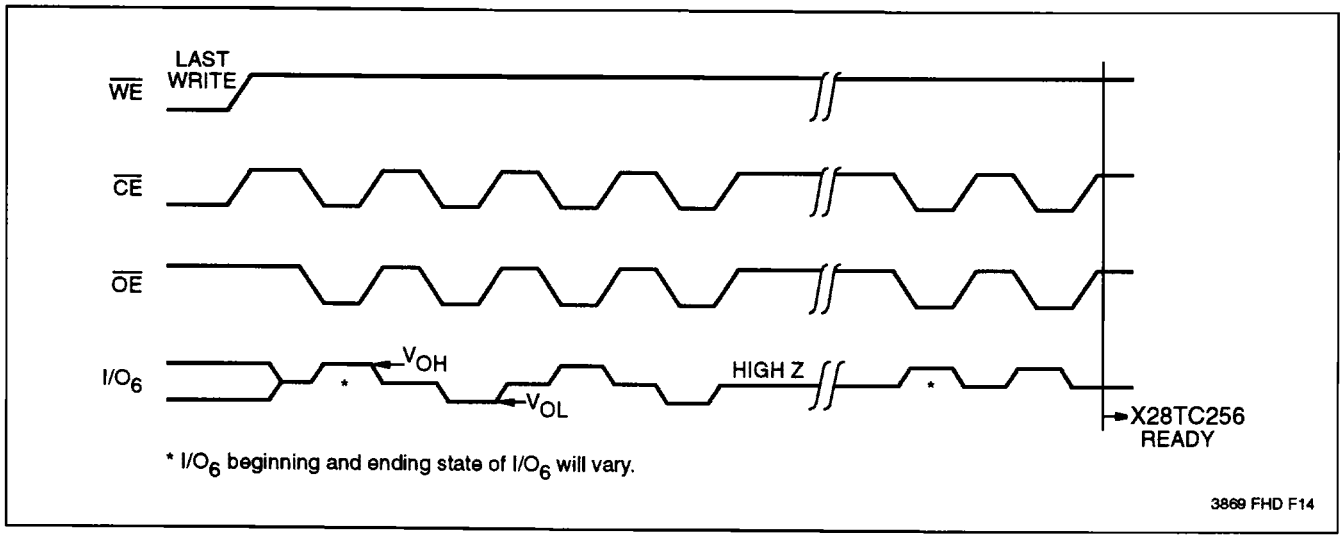
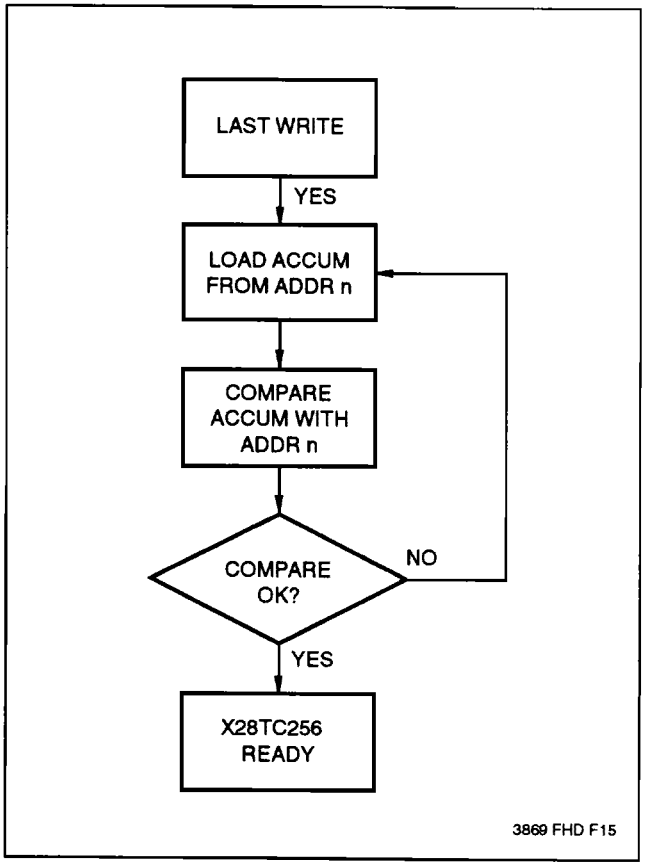


Figure 5. Toggle Bit Software Flow



The Toggle Bit can eliminate the software housekeeping chore of saving and fetching the last address and data written to a device in order to implement $\overline{DATA}$ Polling. This can be especially helpful in an array comprised of multiple X28TC256 memories that is frequently updated. The timing diagram in Figure 4 illustrates the sequence of events on the bus. Toggle bit can be either a Turbo or a page read operation. The software flow diagram in Figure 5 illustrates a method for testing the Toggle Bit.

HARDWARE DATA PROTECTION

The X28TC256 provides two hardware features that protect nonvolatile data from inadvertent writes.

- Default V_{CC} Sense—All write functions are inhibited when V_{CC} is ≤ 3.0V typically.
- Write Inhibit—Holding either $\overline{OE}$ LOW, $\overline{WE}$ HIGH, or $\overline{CE}$ HIGH will prevent an inadvertent write cycle during power-on and power-off, maintaining data integrity.

SOFTWARE DATA PROTECTION

The X28TC256 offers a software controlled data protection feature. The X28TC256 is shipped from Xicor with the software data protection ENABLED. In this mode, data is protected during power-up/down operations.

The X28TC256 is automatically protected during power-up and power-down without the need for external circuits by employing the software data protection feature. This circuit is nonvolatile and will remain set for the life of the device.

With the software protection enabled, the X28TC256 is also protected from inadvertent and accidental writes in the powered-on state. That is, the software algorithm must be issued prior to writing additional data to the device.

SOFTWARE ALGORITHM

The software data protection requires the host system to precede data write operations by a series of three write operations to three specific addresses. Refer to Figure 6 and 7 for the sequence. The three byte sequence opens the page write window enabling the host to write from one to sixty-four bytes of data. Once the page load cycle has been completed, the device will automatically be returned to the data protected state.

SOFTWARE DATA PROTECTION

Figure 6. Timing Sequence—Byte or Page Write

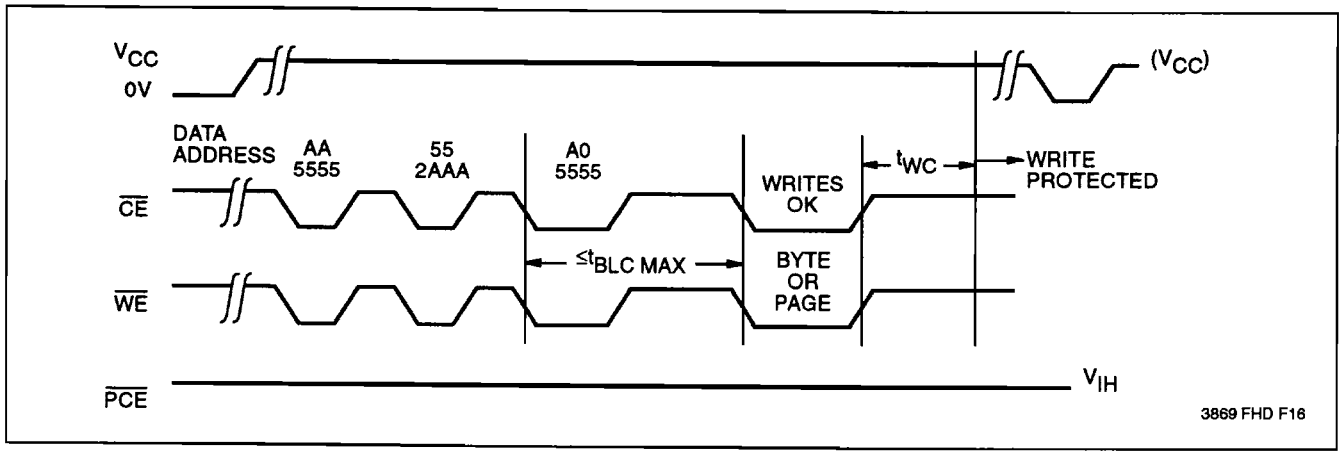
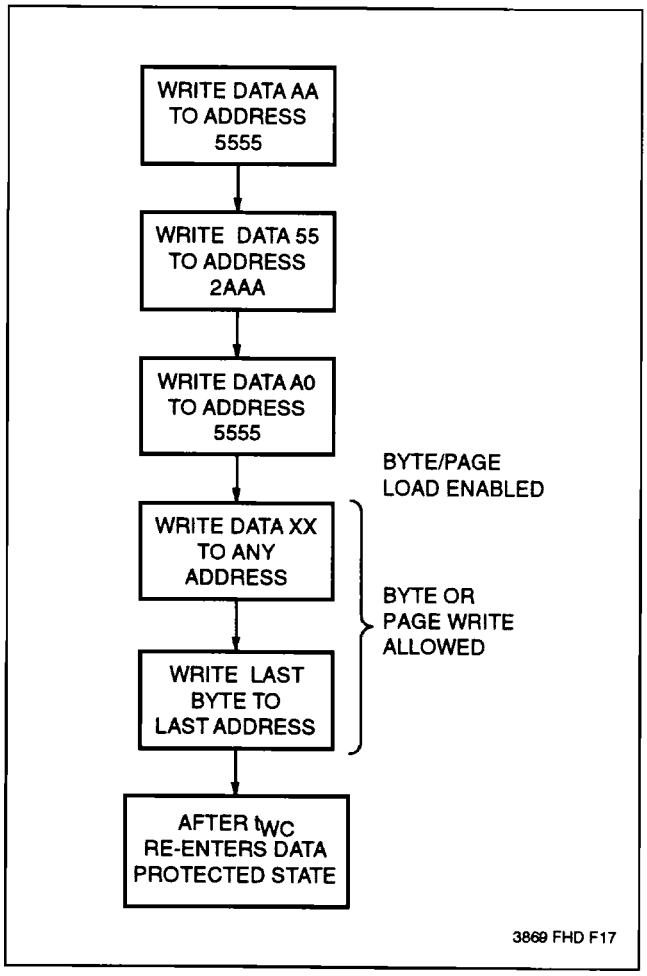


Figure 7. Write Sequence –Byte or Page Write



The software Data Protection Sequence must conform to the Write Cycle Timing Specification.

SYSTEM CONSIDERATIONS

Because the X28TC256 is frequently used in large memory arrays it is provided with a two line control architecture for both read and write operations. Proper usage can provide the lowest possible power dissipation and eliminate the possibility of contention where multiple I/O pins share the same bus.

To gain the most benefit it is recommended that $\overline{CE}$ be decoded from the address bus and be used as the primary device selection input. Both $\overline{OE}$ and $\overline{WE}$ would then be common among all devices in the array. For a read operation this assures that all deselected devices are in their standby mode and that only the selected device(s) is outputting data on the bus.

Because the X28TC256 has two power modes, standby and active, proper decoupling of the memory array is of prime concern. Enabling $\overline{CE}$ will cause transient current spikes. The magnitude of these spikes is dependent on the output capacitive loading of the I/Os. Therefore, the larger the array sharing a common bus, the larger the transient spikes. The voltage peaks associated with the current transients can be suppressed by the proper selection and placement of decoupling capacitors. As a minimum, it is recommended that a 0.1 µF high frequency ceramic capacitor be used between V_{CC} and GND at each device. Depending on the size of the array, the value of the capacitor may have to be larger.

In addition, it is recommended that a 4.7 µF electrolytic bulk capacitor be placed between V_{CC} and GND for each eight devices employed in the array. This bulk capacitor is employed to overcome the voltage droop caused by the inductive effects of the PC board traces.

The $\overline{WAIT}$ output signal is an open drain configuration and can be shared with other wait signals.

SYMBOL TABLE

WAVEFORM	INPUTS	OUTPUTS
———	Must be steady	Will be steady
	May change from Low to High	Will change from Low to High
	May change from High to Low	Will change from High to Low
	Don't Care: Changes Allowed	Changing: State Not Known
	N/A	Center Line is High Impedance

ABSOLUTE MAXIMUM RATINGS*

Temperature Under Bias.....–65°C to +135°C
Storage Temperature ..... .–65°C to +150°C
Voltage on any Pin with
Respect to V_{SS} ..... –1.0V to +7V
D.C. Output Current ..... 10 mA
Lead Temperature (Soldering, 10 Seconds) .....300°C

***COMMENT**

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and the functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

RECOMMENDED OPERATING CONDITIONS

Temperature	Min.	Max.
Commercial	0°C	70°C
Industrial	–40°C	+85°C
Military	–55°C	+125°C

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Supply Voltage	Limits
X28TC256	5V ± 10%

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D.C. OPERATING CHARACTERISTICS (Over recommended operating conditions unless otherwise specified.)

Symbol	Parameter	Limits			Units	Test Conditions
		Min.	Typ.(1)	Max.		
I_{CC1}	V_{CC} Active Current (Page Read)		20	50	mA	$\overline{CE} = \overline{OE} = V_{IL}$, $\overline{WE} = V_{IH}$, All I/O's = Open, Address Inputs= $\overline{PCE}$ =0.4V/2.4V Levels @ f =6.6 MHz
I_{CC2}	V_{CC} Active Current (Byte/Turbo Read)		15	40	mA	$\overline{CE} = \overline{OE} = V_{IL}$, $\overline{PCE} = \overline{WE} = V_{IH}$, All I/O's = Open, Address Inputs = 0.4V/2.4V Levels @ f = 33 MHz
I_{SB1}	V_{CC} Standby Current (TTL Inputs)		2	3	mA	$\overline{CE} = V_{IH}$, $\overline{OE} = V_{IL}$, All I/O's = Open, Other Inputs = V_{IH}
I_{SB2}	V_{CC} Standby Current (CMOS Inputs)		200	500	µA	$\overline{CE} = V_{CC} - 0.3V$, $\overline{OE}$ = GND, All I/O's = Open Other Inputs = $V_{CC} - 0.3V$
I_{LI}	Input Leakage Current			10	µA	V_{IN} = GND to V_{CC}
I_{LO}	Output Leakage Current			10	µA	V_{OUT} = GND to V_{CC}, $\overline{CE} = V_{IH}$
V_{IL}(2)	Input Low Voltage	–1.0		0.8	V	
V_{IH}(2)	Input High Voltage	2.0		V_{CC} + 1.0	V	
V_{OL}	Output Low Voltage			0.4	V	I_{OL} = 5mA
V_{OH}	Output High Voltage	2.4			V	I_{OH} = –5mA

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Notes: (1) Typical values are for T_A = 25°C and nominal supply voltage.
(2) V_{IL} min. and V_{IH} max. are for reference only and are not tested.

POWER-UP TIMING

Symbol	Parameter	Max.	Units
t_{PUR}(3)	Power-Up to Read	100	µs
t_{PUW}(3)	Power-Up to Write	5	ms

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CAPACITANCE T_A = 25°C, F = 1.0MHz, V_{CC} = 5V.

Symbol	Test	Max.	Units	Conditions
$C_{I/O}$(3)	Input/Output Capacitance	10	pF	$V_{I/O}$ = 0V
C_{IN}(3)	Input Capacitance	6	pF	V_{IN} = 0V

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ENDURANCE AND DATA RETENTION

Parameter	Min.	Max.	Units
Endurance	10,000		Cycles per Byte
Data Retention	100		Years

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MODE SELECTION

$\overline{CE}$	$\overline{OE}$	$\overline{WE}$	PCE	Mode	I/O	Power
L	L	H	⌐	Page Read	D_{OUT}	Active
L	L	H	X	Byte Read	D_{OUT}	Active
L	H	L	X	Write	D_{IN}	Active
H	X	X	X	Standby and Write Inhibit	High Z	Standby
X	L	X	X	Write Inhibit	—	—
X	X	H	X	Write Inhibit	—	—

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A.C. CONDITIONS OF TEST

Input Pulse Levels	0V to 3.0V
Input Rise and Fall Times	5ns
Input and Output Timing Levels	1.5V

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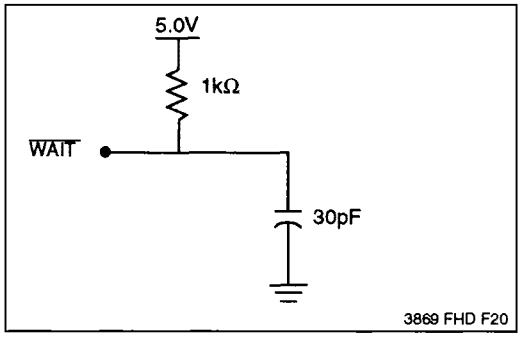
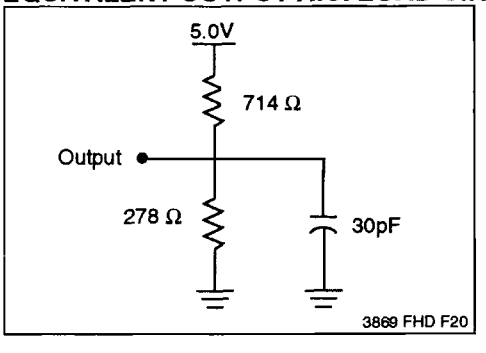
EQUIVALENT $\overline{WAIT}$ A.C. LOAD CIRCUIT



EQUIVALENT OUTPUT A.C. LOAD CIRCUIT



Note: (3) This parameter is periodically sampled and not 100% tested.

A.C. CHARACTERISTICS (Over the recommended operating conditions, unless otherwise specified.)

PAGE READ CYCLE LIMITS

Symbol	Parameter	X28TC256-25 -40°C to +85°C		X28TC256-35 -55°C to +125°C		X28TC256-45 -55°C to +125°C		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	
t_{RCP}	Page Read Cycle Time		150		150		150	ns
t_{PA}	Page Read AcessTime		150		150		150	ns
t_{WAIT}	Wait Signal Access Time		15		20		20	ns
t_{RAS}	Address Setup Time	5		5		5		ns
t_{RAH}	Address Hold Time	10		10		10		ns
t_{PCH} (4)	$\overline{PCE}$ High Time	10		10		10		ns
t_{PCL} (4)	$\overline{PCE}$ Low Time	10		10		10		ns
t_{RCS}	Chip Enable Setup Time	5		5		5		ns
t_{POH}	Output Hold From Page Change	0		0		0		ns

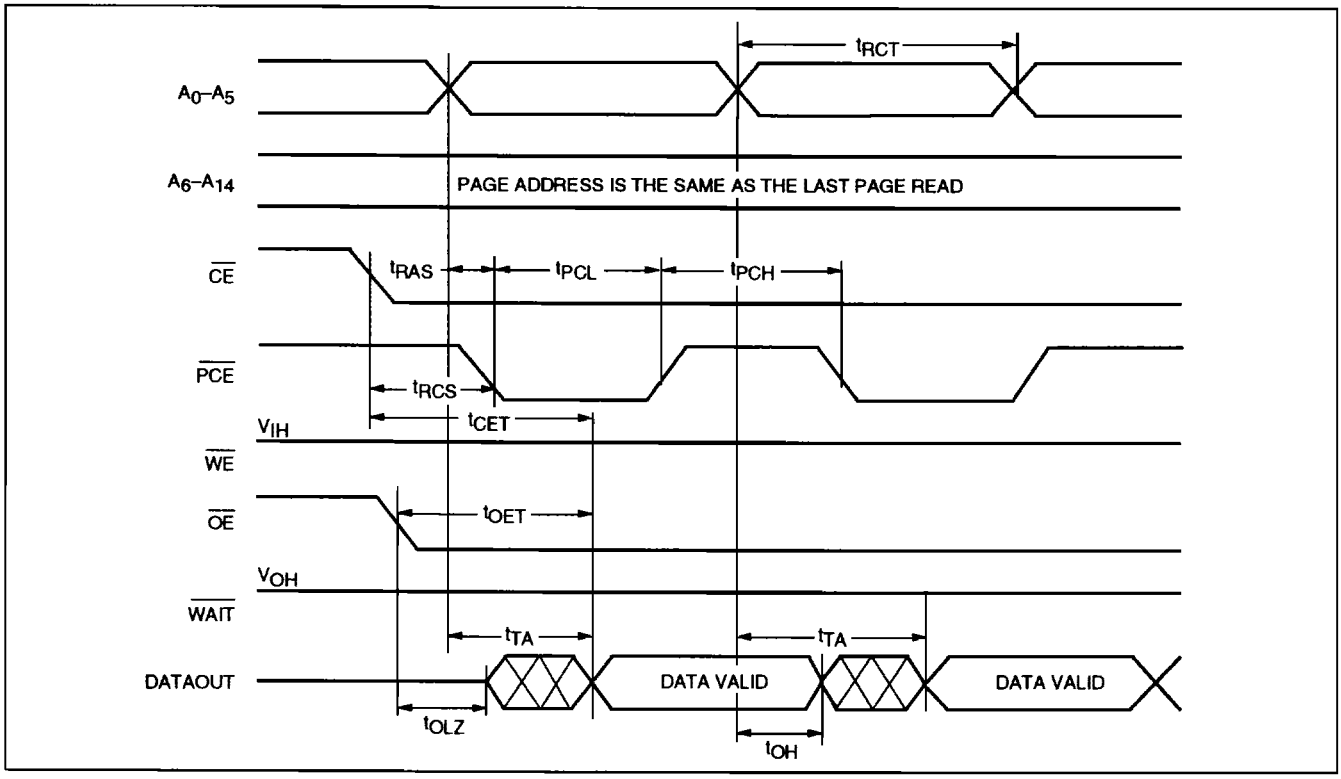
BYTE (Turbo) READ CYCLE LIMITS

Symbol	Parameter	X28TC256-25 -40°C to +85°C		X28TC256-35 -55°C to +125°C		X28TC256-45 -55°C to +125°C		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	
t_{TA}	Byte (Turbo) Acess Time		25		35		45	ns
t_{CET}	Chip Enable Acess Time		25		35		45	ns
t_{OET}	Output Enable Access Time		20		20		20	ns
t_{RCT}	Turbo Read Cycle Time		25		35		45	ns
t_{LZ} (5)	Chip Enable to Output in Low Z	0		0		0		ns
t_{HZ} (5)	Chip Enable to Output in High Z	0		0		0		ns
t_{OLZ} (5)	Output Enable to Output in Low Z	0		0		0		ns
t_{OHZ} (5)	Output Enable to Output in High Z	0		0		0		ns
t_{OH}	Output hold from address change	0		0		0		ns

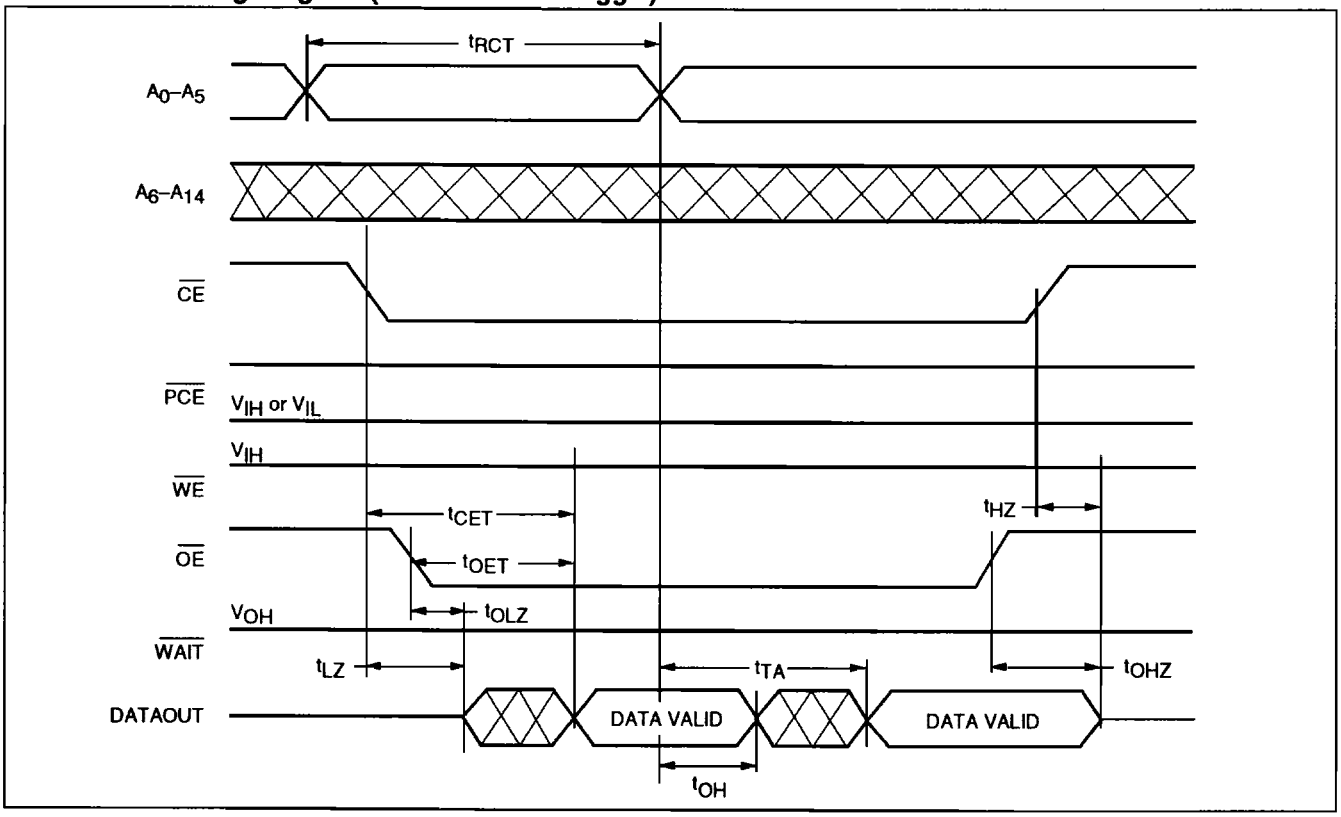
Notes: (4) t_{PCH} and t_{PCL} are periodically sampled and not 100% tested.

(5) t_{LZ} min., t_{HZ}, t_{OHZ}, t_{OLZ} min. are periodically sampled and not 100% tested. t_{HZ} and t_{OHZ} are measured with CL=5pF from the point when $\overline{CE}$, $\overline{OE}$ return high (whichever occurs first) to the time when the outputs are no longer driven.

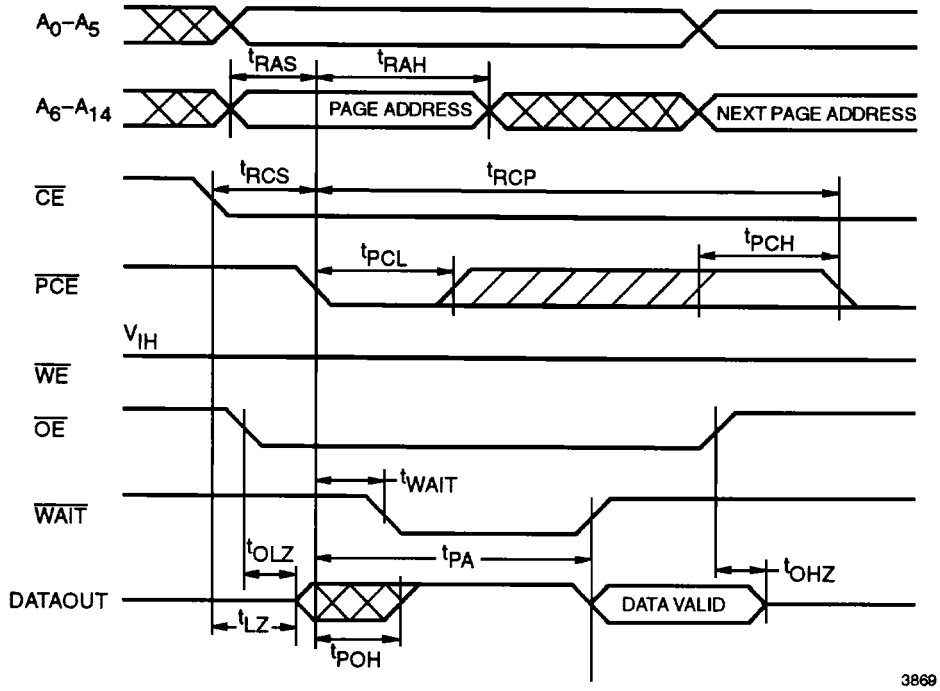
Turbo Read Timing Diagram ($\overline{PCE}$ Toggles)



Turbo Read Timing Diagram ($\overline{PCE}$ Does Not Toggle)



Page Read Timing Diagram (The Chip Remains Selected During t_{PA})



Write Cycle Limits

Symbol	Parameter	Min.	Typ.(5)	Max.	Units
t_{WC}(5)	Write Cycle Time		3	5	ms
t_{AS}	Address Setup Time	0			ns
t_{AH}	Address Hold Time	50			ns
t_{CS}	Write Setup Time	0			ns
t_{CH}	Write Hold Time	0			ns
t_{CW}	$\overline{CE}$ Pulse Width	50			ns
t_{OES}	$\overline{OE}$ High Setup Time	0			ns
t_{OEH}	$\overline{OE}$ High Hold Time	0			ns
t_{WP}	$\overline{WE}$ Pulse Width	50			ns
t_{WPH}(6)	$\overline{WE}$ High Recovery (page write only)	50			ns
t_{DS}	Data Setup	50			ns
t_{DH}	Data Hold	0			ns
t_{DW}(6)	Delay to Next Write after polling is true	10			µs
t_{BLC}	Byte Load Cycle	0.150		100	µs

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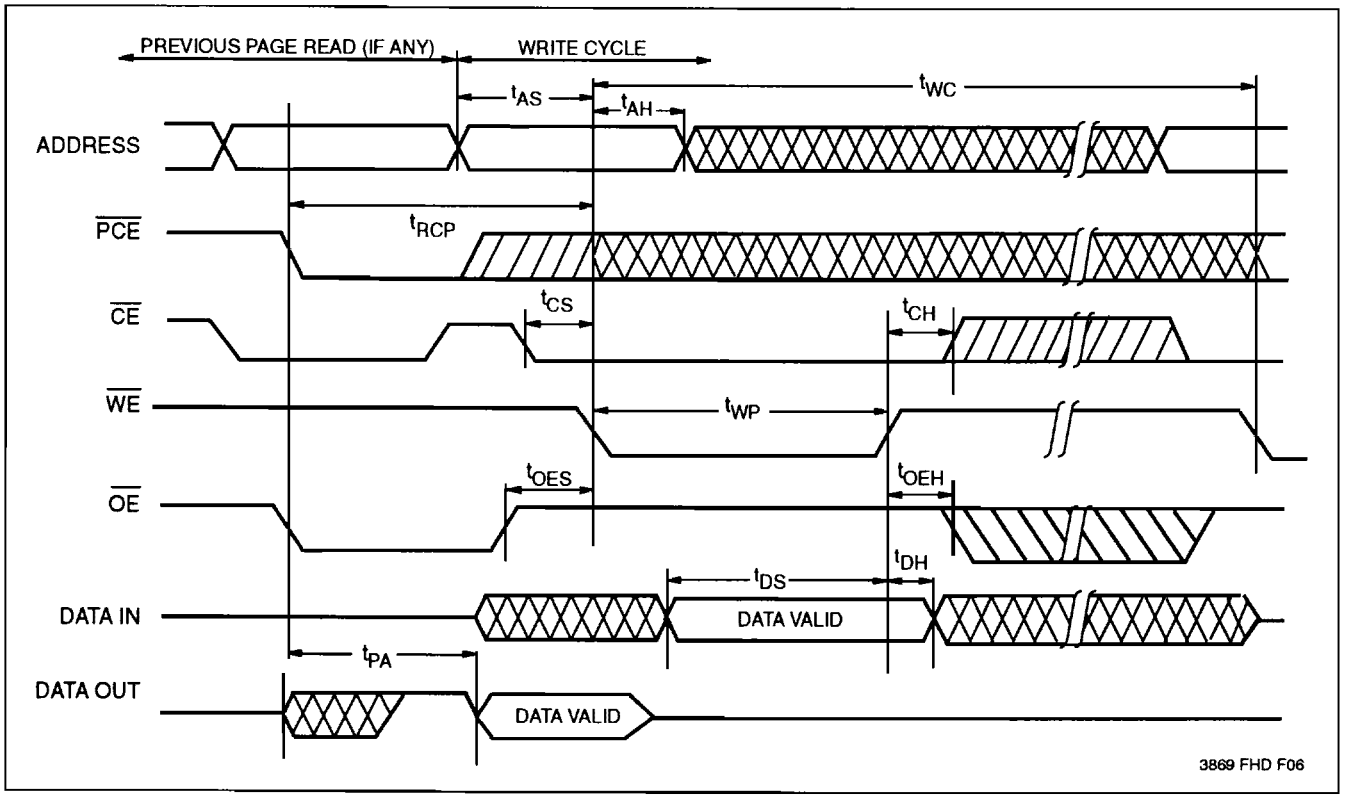
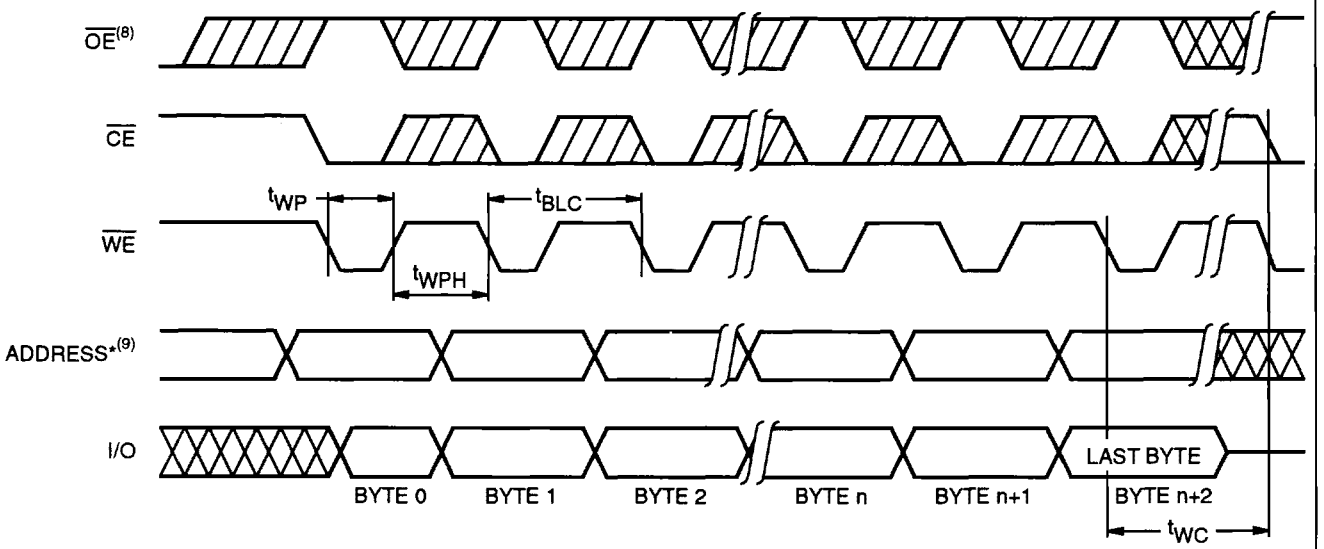
Write Cycle



Notes: (6) t_{WC} is the minimum cycle time to be allowed from the system perspective unless polling techniques are used. It is the maximum time the device requires to automatically complete the internal write operation.

(7) t_{WPH} and t_{DW} are periodically sampled and not 100% tested.

Page Write Cycle

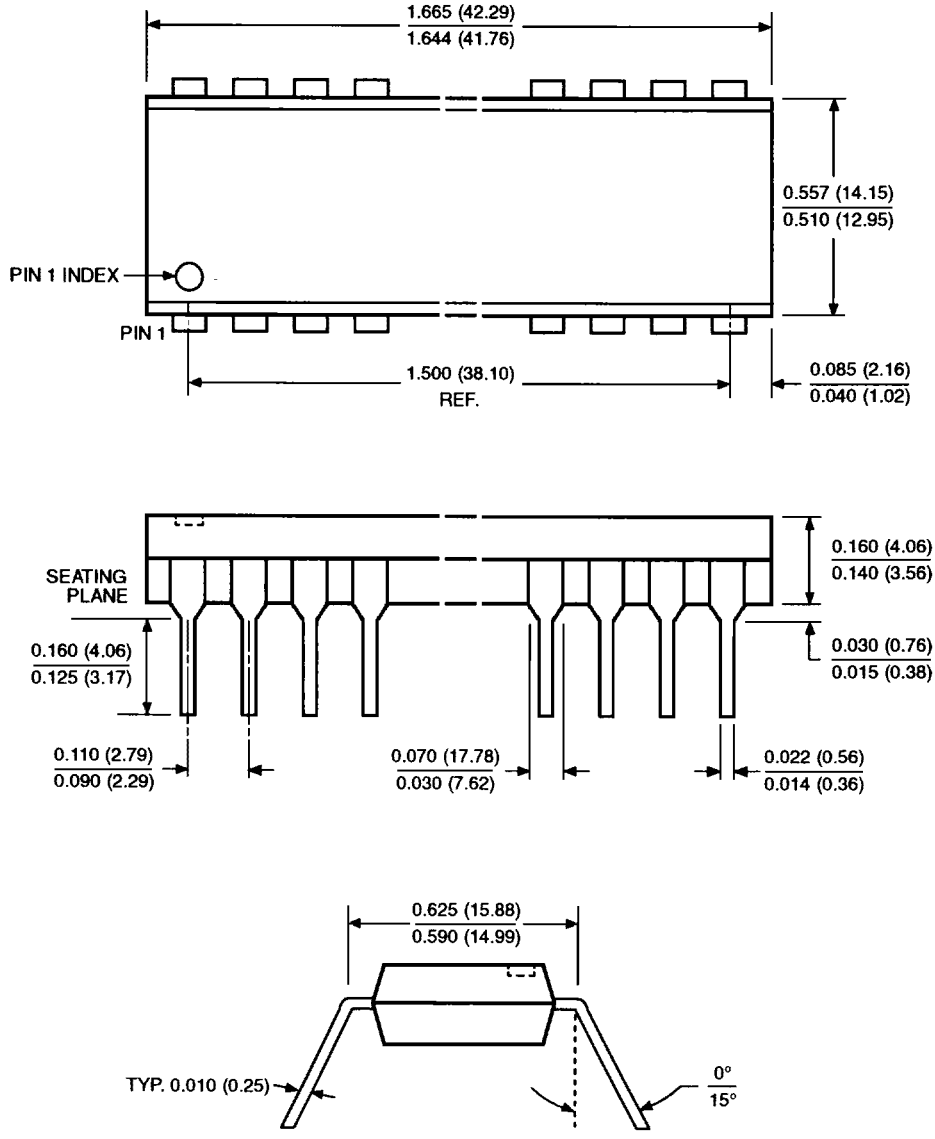


Notes: (8) Between successive byte writes within a page write operation, $\overline{OE}$ can be strobed LOW: e.g. this can be done with $\overline{CE}$ and $\overline{WE}$ HIGH to fetch data from another memory device within the system for the next write; or with $\overline{WE}$ HIGH and $\overline{CE}$ LOW effectively performing a polling operation.

(9) The timings shown above are unique to page write operations. Individual byte load operations within the page write must conform to the write cycle timing.

PACKAGING INFORMATION

32-LEAD PLASTIC DUAL IN-LINE PACKAGE TYPE P



NOTE:
1. ALL DIMENSIONS IN INCHES (IN PARENTHESES IN MILLIMETERS)
2. PACKAGE DIMENSIONS EXCLUDE MOLDING FLASH

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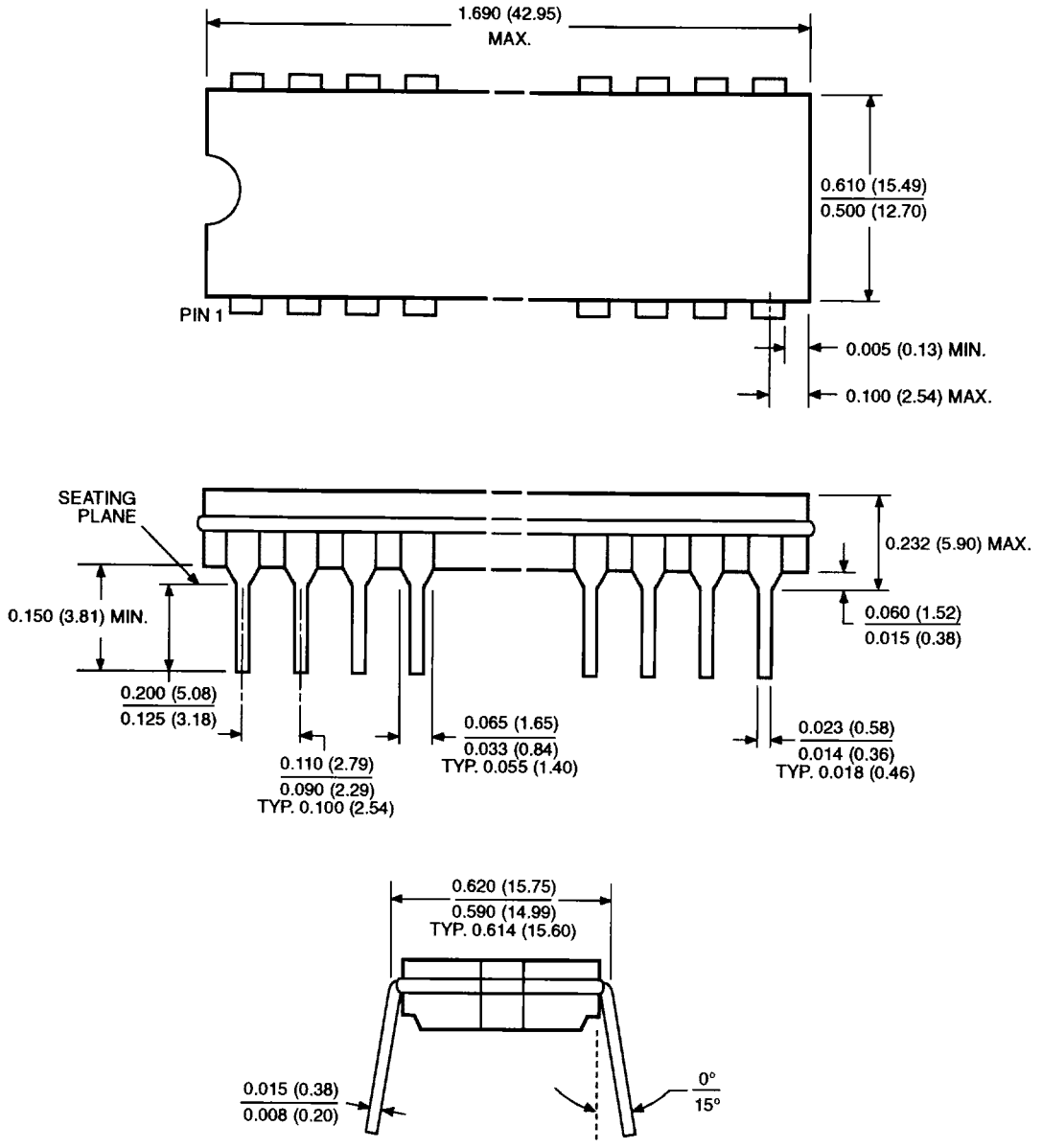
PACKAGING INFORMATION

32-LEAD HERMETIC DUAL IN-LINE PACKAGE TYPE D

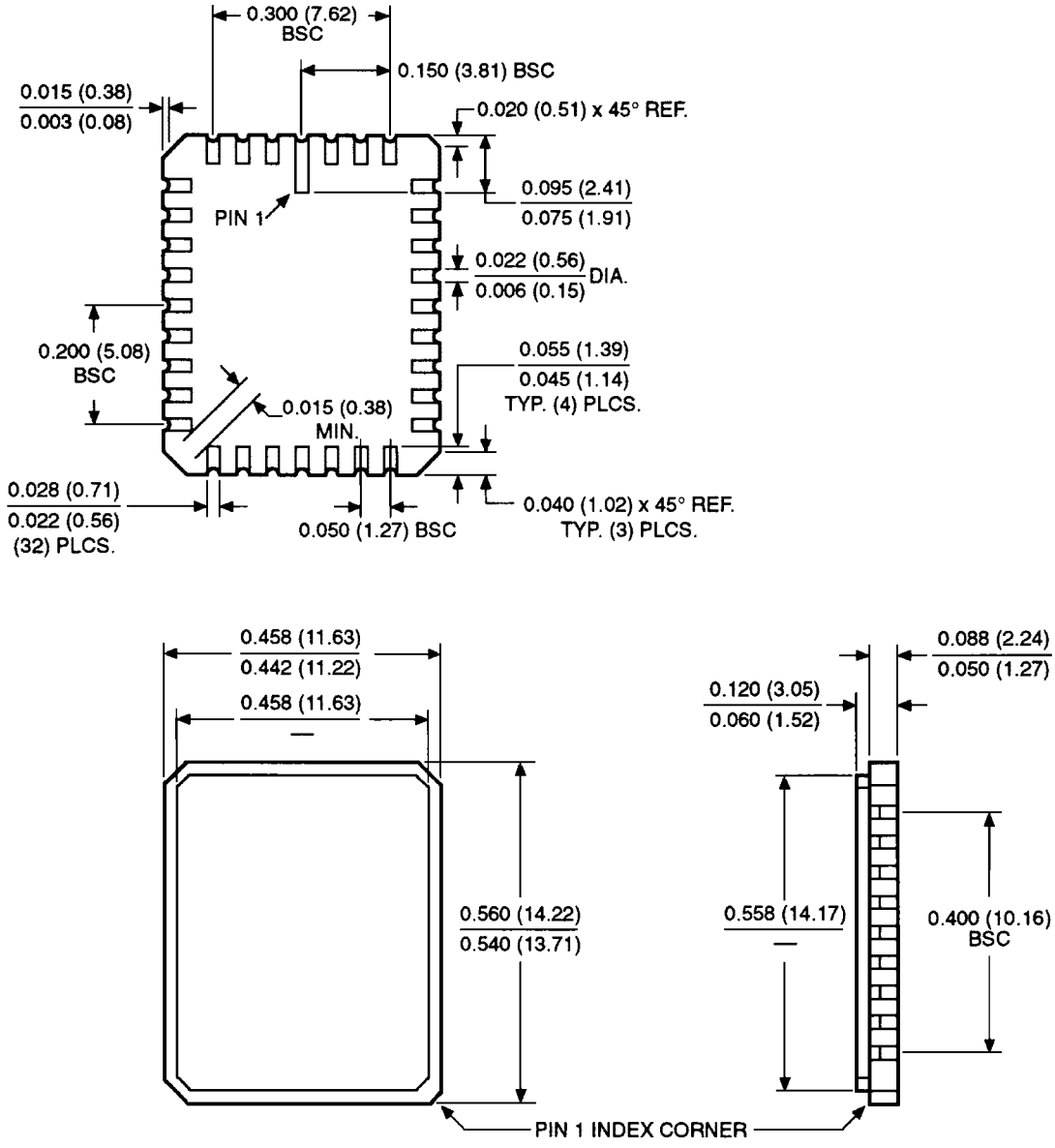


NOTE: ALL DIMENSIONS IN INCHES (IN PARENTHESES IN MILLIMETERS)

3926 FHD F09

PACKAGING INFORMATION

32-PAD CERAMIC LEADLESS CHIP CARRIER PACKAGE TYPE E



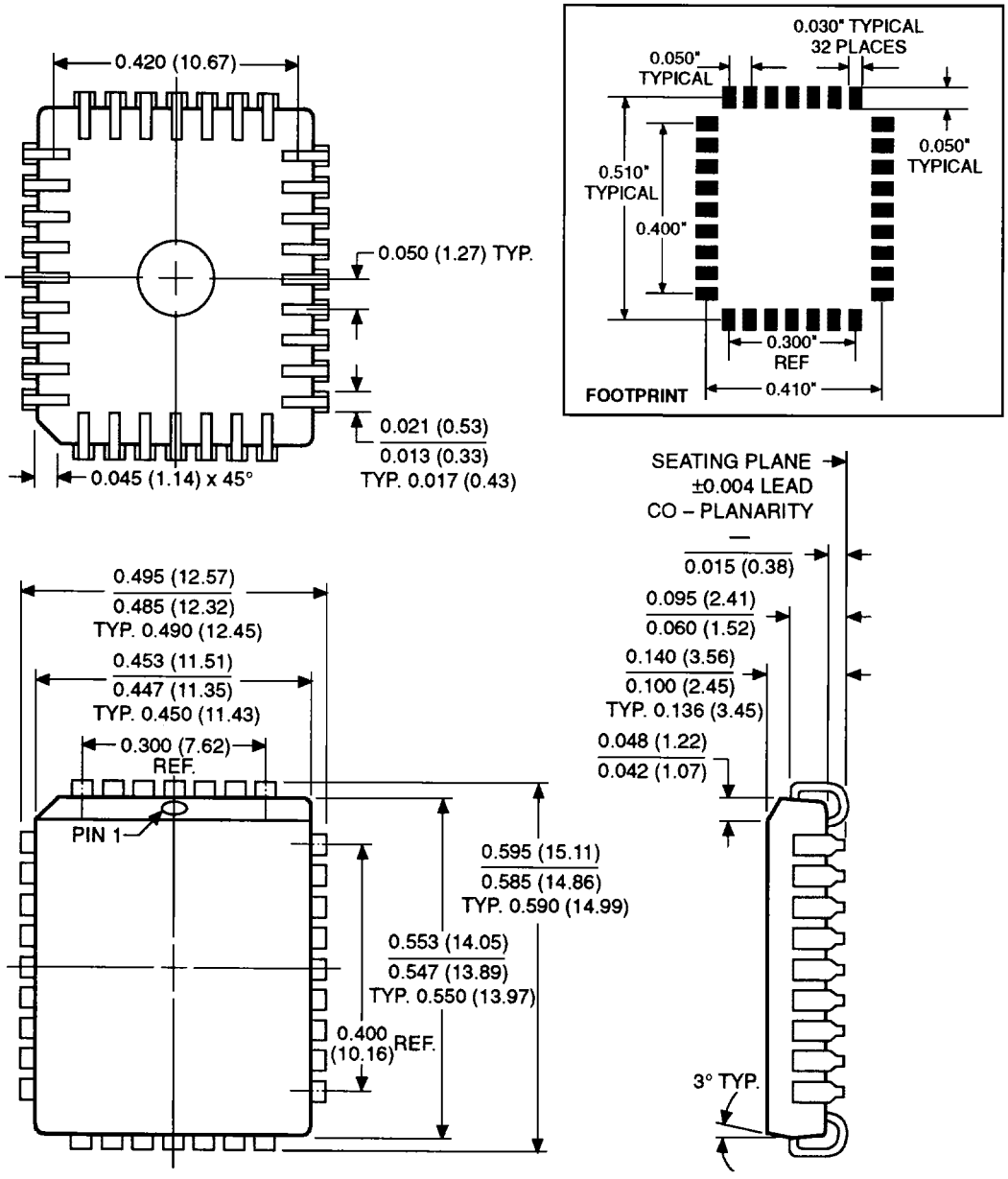
NOTE:

1. **ALL DIMENSIONS IN INCHES (IN PARENTHESES IN MILLIMETERS)**
2. **TOLERANCE: ±1% NLT ±0.005 (0.127)**

3926 FHD F14

PACKAGING INFORMATION

32-LEAD PLASTIC LEADED CHIP CARRIER PACKAGE TYPE J



NOTES:
1. ALL DIMENSIONS IN INCHES (IN PARENTHESES IN MILLIMETERS)
2. DIMENSIONS WITH NO TOLERANCE FOR REFERENCE ONLY

3926 FHD F13

ORDERING INFORMATION