16M BYTE (4M x32) FLASH (5VSupply; 5V Program) SIMM MODULE

*PRELIMINARY**

FEATURES

- Access Time of 100ns
- Packaging:
  - 80 pin SIMM
- TTL compatible inputs and outputs
- 5V V_{CC}/ 5V V_{PP}
- Three power on reset options
  - No power on reset: $\overline{RST}$ tied to Vcc (Option "V")
  - Power on reset: $\overline{RST}$ tied to power supervisor circuit (Option "P")
  - System control of power on reset: $\overline{RST}$ tied to pin 7 (Option "R"; this option is not JEDEC standard)
- Tin or Gold edge connectors
- Intel Part Number E28F160S5 Flash Memory Component

GENERAL DESCRIPTION

The White Microelectronics WPF29162-100X8XI is a 4M x 32 bits Flash Memory Module (SIMM). The WPF29162-100X8XI consists of eight 1M x 16 bits CMOS Flash memory in 56-pin TSOP packages mounted on an 80-pin glass epoxy substrate. Decoupling capacitors of 0.1µF are mounted for the Flash memory.

The WPF29162-100X8XI is intended for mounting into 80-pin edge connector sockets. The WPF29162-100X8XI uses the standard programming algorithms for Intel E28F160S5 Flash memory component and is backward compatible to the 28F160S5 Flash memory component.

* *This data sheet describes a product under development, not fully characterized, and is subject to change without notice.*

PIN CONFIGURATION

Pin Symbols

Pin	Symbol	Pin	Symbol	Pin	Symbol
1	V_{SS}	28	DQ_{31}	55	DQ_{15}
2	V_{CC}	29	$\overline{WE}_1$	56	DQ_{14}
3	V_{PP}	30	NC	57	DQ_{13}
4	$\overline{OE}$	31	NC	58	DQ_{12}
5	$\overline{WE}_0$	32	NC	59	DQ_{11}
6	NC	33	A_{19}	60	DQ_{10}
7	NC/$\overline{RST}$	34	A_{18}	61	DQ_9
8	DQ_{16}	35	A_{17}	62	DQ_8
9	DQ_{17}	36	A_{16}	63	DQ_7
10	DQ_{18}	37	A_{15}	64	DQ_6
11	DQ_{19}	38	A_{14}	65	DQ_5
12	DQ_{20}	39	A_{13}	66	DQ_4
13	DQ_{21}	40	A_{12}	67	DQ_3
14	DQ_{22}	41	A_{11}	68	DQ_2
15	DQ_{23}	42	A_{10}	69	DQ_1
16	DQ_{24}	43	A_9	70	DQ_0
17	DQ_{25}	44	A_8	71	V_{PP}
18	DQ_{26}	45	A_7	72	V_{CC}
19	DQ_{27}	46	A_6	73	PD_1
20	DQ_{28}	47	A_5	74	PD_2
21	$\overline{CE}_3$	48	A_4	75	PD_3
22	$\overline{CE}_2$	49	A_3	76	PD_4
23	$\overline{CE}_1$	50	A_2	77	PD_5
24	$\overline{CE}_0$	51	A_1	78	PD_6
25	V_{SS}	52	A_0	79	PD_7
26	DQ_{29}	53	NC	80	V_{SS}
27	DQ_{30}	54	V_{SS}		

Pin Functions

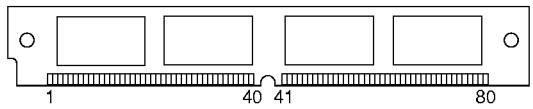
Pin Symbol	Pin Function
A_0-A_{19}	Address Inputs
DQ_0-DQ_{31}	Data In/Out
$\overline{CE}_0$-$\overline{CE}_3$	Chip Enable
$\overline{WE}_0$-$\overline{WE}_1$	Write Enable
$\overline{OE}$	Output Enable
PD_1-PD_7	Presence Detect
$\overline{RST}$	Reset
V_{CC}	Power (+5V)
V_{PP}	Programming Voltage (+5V)
V_{SS}	Ground
NC	No Connection

Presence Detect Pins*

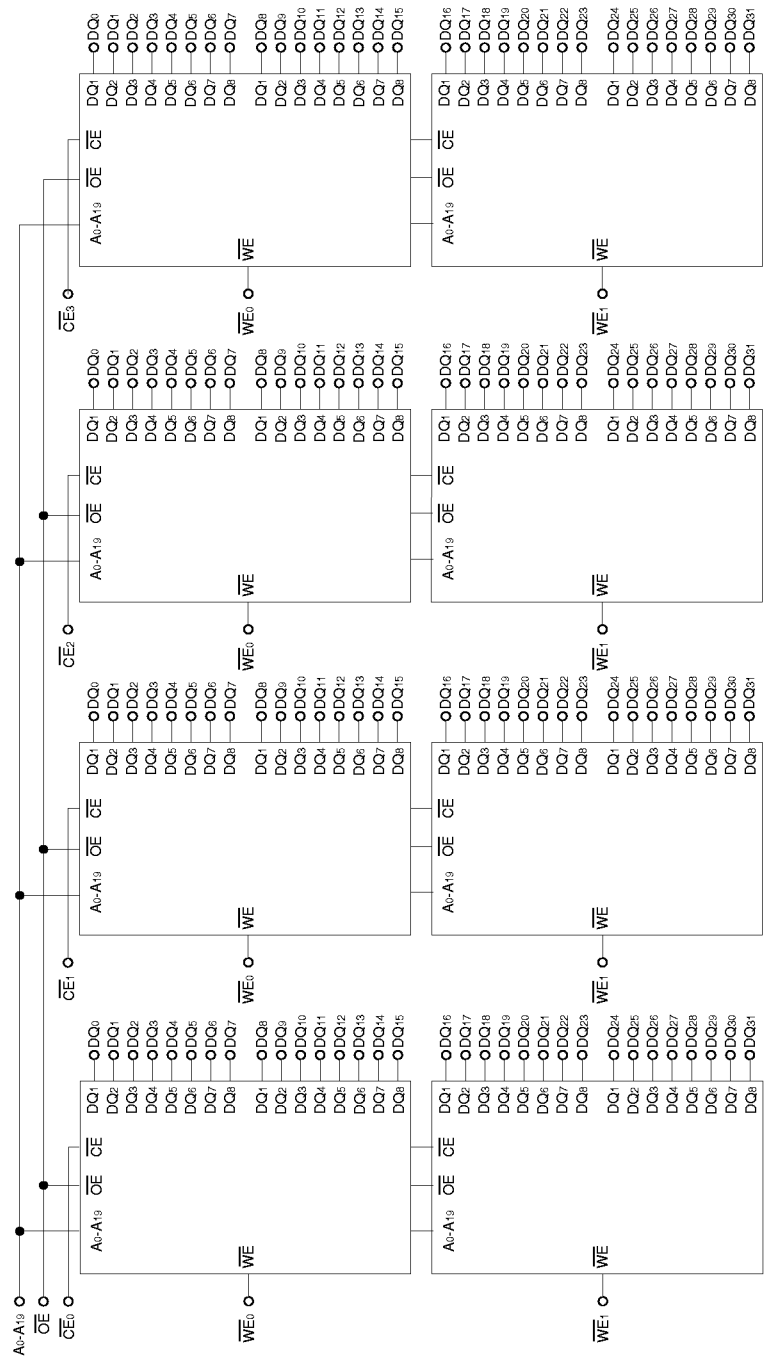
(Optional)

Pin Name	Signal
PD_1	NC
PD_2	V_{SS}
PD_3	V_{SS}
PD_4	V_{SS}
PD_5	V_{SS}
PD_6	NC
PD_7	V_{SS}

* Pin Connection Changing Available



FUNCTIONAL BLOCK DIAGRAM



Notes:

1. $\overline{RP}$ of all flash memory components is optionally tied to V_{CC}; tied to $\overline{RST}$ (Pin 7 of PCB), or connected to power supervisor circuit.
2. RD/$\overline{BY}$ of the flash memory components are not connected.

ABSOLUTE MAXIMUM RATINGS[1]

Item	Symbol	Rating	Units
Voltage on Any Pin Relative to V_{SS}[2]	V_{IN}, V_{OUT}	-2.0 to +7.0	V
Voltage on V_{CC} Relative to V_{SS}[2]	V_{RST}	-2.0 to +7.0	V
Storage Temperature	T_{stg}	-65 to +125	°C
Short Circuit Output Current[4]	I_{OS}	100	mA

1. Permanent device damage may occur if "ABSOLUTE MAXIMUM RATINGS" are exceeded. Functional Operation should be restricted to the conditions as detailed in the oprerational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.
2. Minimum DC voltage on input or I/O pins is -0.5 V and on V_{CC}, $\overline{RST}$ and V_{PP} is -0.2V. During voltage transitions, this level may undershoot V_{SS} to -2.0 V for periods of up to 20 ns. Maximum DC voltage on input and I/O pins is V_{CC}+0.5 V. During voltage transitions, input and I/O pins may overshoot to V_{CC}+2.0 V for periods up to 20 ns.
3. Maximum DC voltage on V_{PP} and $\overline{RST}$ may overshoot to +14.0V for periods <20ns.
4. No more than one output shorted to ground at a time. Duration of the short circuit should not be greater than one second.

CAPACITANCE (T_A=25 °C; V_{CC}=5.0V±0.5V; f=1MHz)

Item	Symbol	Typ	Units
A_0-A_{19}, $\overline{OE}$, $\overline{RST}$ Input Capacitance (V_{IN}=0)	C_{IN1}	63	pF
$\overline{WE}_0$-$\overline{WE}_1$ Input Capacitance (V_{IN}=0)	C_{IN2}	39	pF
$\overline{CE}_0$-$\overline{CE}_3$ Input Capacitance (V_{IN}=0)	C_{IN3}	39	pF
DQ_0-DQ_{31} Input Capacitance (V_{IN}=0)	C_{IN4}	45	pF
DQ_0-DQ_{31}Output Capacitance (V_{OUT}=0)	C_{OUT}	50	pF

DC CHARACTERISTICS (V_{CC}=5.0V±0.5V; T_A= 0°C to +70°C)

Parameter	Symbol	Min	Typ	Max	Units	Notes
Input Load Current (V_{IN}=V_{SS} or V_{CC}, V_{CC}=V_{CC}Max)	I_{LI}			±8	µA	1
Output Leakage Current (V_{OUT}=V_{SS} or V_{CC}, V_{CC}=V_{CC} Max)	I_{LO}			±40	µA	1
V_{CC} Standby Current (V_{CC}=V_{CC} Max, $\overline{CE}$=$\overline{RST}$=V_{CC}±0.2V, CMOS) (V_{CC}=V_{CC} Max, $\overline{CE}$=$\overline{RST}$=V_{IH}, TTL)	I_{CCS}		200 16	800 32	µA mA	1,5
V_{CC} Deep Power Down Current ($\overline{RST}$=V_{SS}±0.2V)	I_{CCD}			120	µA	1
V_{CC} Read Current (CMOS input) ($\overline{CE}$=V_{IL}, $\overline{OE}$=V_{IH}, f=10MHz, I_{OUT}=0mA)	$I_{CCR}1$			101	mA	1,4,5
V_{CC} Read Current (TTL input) ($\overline{CE}$=V_{IL}, $\overline{OE}$=V_{IH}, f=10MHz, I_{OUT}=0mA)	$I_{CCR}2$			154	mA	1,4,5
V_{CC} Program/Set Lock-Bit Current (V_{PP}=5.0V±10%)	I_{CCW}			94	mA	1,6
V_{CC} Block Erase/Clear Block Lock-Bit Current (V_{PP}=5.0V±10%)	I_{CCE}			84	mA	1,6
V_{CC} Program/Block Erase Suspend Current ($\overline{CE}$=V_{IH})	I_{CCES}		4	44	mA	1,2
V_{PP} Standby Current (V_{PP}≤V_{CC})	I_{PPS}		±16	±120	µA	1
V_{PP} Read Current (V_{PP}>V_{CC})	I_{PPR}		80	1600	µA	
V_{PP} Deep Power Down Current ($\overline{RST}$=V_{SS}±0.2V)	I_{PPD}		0.8	40	µA	1
V_{PP} Program or Set Lock-Bit Current (V_{PP}=5.0V±10%)	I_{PPW}			161	mA	1,6
V_{PP} Block Erase or Clear Block Lock-Bit Current (V_{PP}=5.0V±10%)	I_{PPE}			81	mA	1,6
V_{PP} Program or Block Erase Suspend Current (Block Erase Suspended)	I_{PPES}		80	1600	µA	1,2
Input Low Voltage	V_{IL}	-0.5		0.8	V	
Input High Voltage	V_{IH}	2.0		V_{CC}+0.5	V	
Output Low Voltage (I_{OL}=5.8 mA, V_{CC}=V_{CC}Min)	V_{OL}			0.45	V	
Output High Voltage (TTL) (I_{OH}=-2.5mA, V_{CC}=V_{CC}Min)	V_{OH1}		2.4		V	
Output High Voltage (CMOS) (I_{OH}=-2.5mA, V_{CC}=V_{CC}Min) (I_{OH}=-100µA, V_{CC}=V_{CC}Min)	V_{OH2}		0.85V_{CC} V_{CC}-0.4		V V	
V_{PP} Write/Erase Lock Voltage	V_{PPLK}			1.5	V	3
V_{PP} during Write/Erase Operations	V_{PPH1}	4.5	5.0	5.5	V	
V_{CC} Write/Erase Lock Voltage	V_{LKO}		2.0		V	

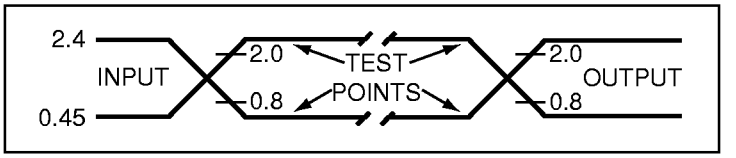
Notes:

1. All currents are in RMS unless otherwise noted. Typical values at V_{CC}=5.0V, T_A=25°C.
2. I_{CCES} are specified with the device deselected. If the device is read while in erase suspend mode, current draw is the sum of I_{CCES} and I_{CCR}.
3. BlockErases, Programs, and Lock Block operations are inhibited when V_{PP}≤V_{PPLK} and not guaranteed in the ranges between V_{PPLK}(max) and V_{PPH1}(min), between V_{PPH1}(max) and V_{PPH2}(min), and above V_{PPH2}(max).
4. Automatic Power Saving (APS) reduces I_{CCR} to 2mA typical in Static operation.
5. CMOS inputs are either V_{CC}±0.2V or V_{SS}±0.2V. TTL inputs are either V_{IL} or V_{IH}.
6. Sampled, not 100% tested.

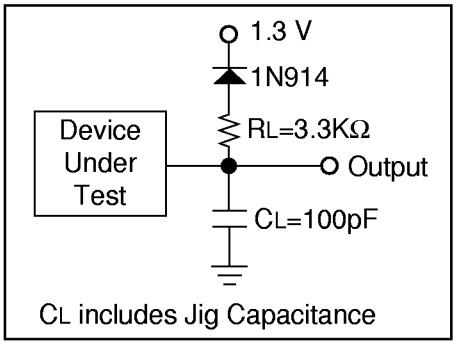
AC CHARACTERISTICS

AC Test Conditions

AC test inputs are driven at V_{OH} (2.4 V_{TTL}) for a Logic "1" and V_{OL} (0.45 V_{TTL}) for a logic "0." Input timing begins at V_{IH} (2.0 V_{TTL}) and V_{IL} (0.8 V_{TTL}). Output timing ends at V_{IH} and V_{IL}. Input rise and fall times (10% to 90%) <10ns. Refer to the Transient Input/Output Reference Waveform and Transient Equivalent Testing Load Circuit figures below.



Transient Input/Output Reference Waveform



Transient Equivalent Testing Load Circuit

Read Only Operations[1] (V_{CC}=5V±10%; T_A=0°C to 70°C)

Parameter	Symbol	Min	Max	Unit	Notes
Read cycle time	t_{AVAV}	100		ns	
Address to output delay	t_{AVQV}		100	ns	
$\overline{CE}$ to output delay	t_{ELQV}		100	ns	2
$\overline{RST}$ to output delay	t_{PHQV}		400	ns	
$\overline{OE}$ to output delay	t_{GLQV}		40	ns	2
$\overline{CE}$ to output in low Z	t_{ELQX}	0		ns	
$\overline{CE}$ to output high Z	t_{EHQZ}		35	ns	
$\overline{OE}$ to output in low Z	t_{GLQX}	0		ns	
$\overline{OE}$ to output high Z	t_{GHQZ}		15	ns	
Output hold from address, $\overline{CE}$ or $\overline{OE}$ change, whichever occurs first	t_{OH}	0		ns	

1. See AC input/output reference waveforms for timing measurements.
2. $\overline{OE}$ may be delayed up to t_{ELQV}-t_{GLQV} after the falling edge of $\overline{CE}$, without impacting t_{ELQV}.

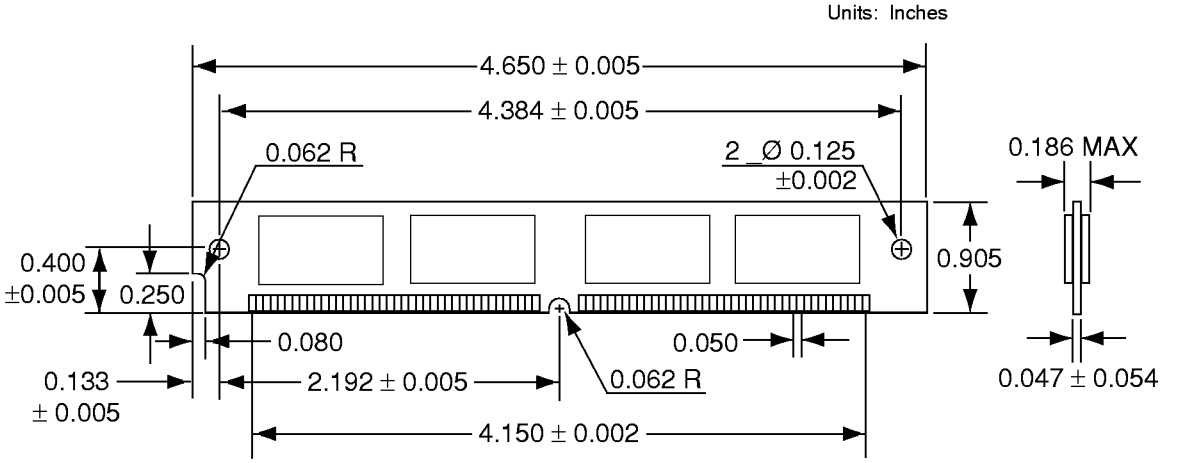
AC CHARACTERISTICS (continued)

Write Operations[1,2] (V_{CC}=5V±10%; T_A=0°C to 70°C)

Parameter	Symbol	Min	Max	Unit	Notes
$\overline{RST}$ high recovery to $\overline{WE}$ ($\overline{CE}$) going low	t_{PHWL} (t_{PHEL})	1		µs	5
$\overline{CE}$ setup to $\overline{WE}$ going low	t_{ELWL}	10		ns	3
$\overline{WE}$ setup to $\overline{CE}$ going low	t_{WLEL}	0		ns	3
Write pulse width	t_{WP}	40		ns	3
Data setup to $\overline{WE}$ ($\overline{CE}$) going high	t_{DVWH} (t_{DVEH})	40		ns	
Address setup to $\overline{WE}$ ($\overline{CE}$) going high	t_{AVWH} (t_{AVEH})	40		ns	
$\overline{CE}$ ($\overline{WE}$) hold from $\overline{WE}$ ($\overline{CE}$) high	t_{WHEH} (t_{EHWH})	10		ns	
Data hold from $\overline{WE}$ ($\overline{CE}$) high	t_{WHDX} (t_{EHDX})	5		ns	
Address hold from $\overline{WE}$ ($\overline{CE}$) high	t_{WHAX} (t_{EHAX})	5		ns	
Write pulse width high	t_{WPH}	30		ns	4
V_{PP} setup to $\overline{WE}$ ($\overline{CE}$) going high	t_{VPWH} (t_{VPEH})	100		ns	5
Write recovery before read	t_{WHGL} (t_{EHGL})	0		ns	

1. Read timing characteristics during block erase, program, and lock-bit configuration operations are the same as during read-only operations. Refer to AC Characteristicsfor read-only operations.
2. A write operation can be initiated and terminated with either $\overline{CE}$ or $\overline{WE}$.
3. Write pulse width (t_{WP}) is defined from $\overline{CE}$ or $\overline{WE}$ going low (whichever goes low last) to $\overline{CE}$ or $\overline{WE}$ going high (whichever goes high first). Hence $t_{WP}=t_{WLWH}=t_{ELEH}=t_{WLEH}=t_{ELWH}$. If $\overline{CE}$ is driven low 10ns before $\overline{WE}$ going low, $\overline{WE}$ pulse width requirement decreases to t_{WP}-20ns.
4. Write pulse width high (t_{WPH}) is defined from $\overline{CE}$ or $\overline{WE}$ going high (whichever goes high first) to $\overline{CE}$ or $\overline{WE}$ going low (whichever goes low last). Hence, $t_{WPH}=t_{WHWL}=t_{WHEL}=t_{WHEL}=t_{EHWL}$.
5. Sampled, not 100% tested.

PACKAGE DIMENSIONS



TOLERANCES: ±0.005 UNLESS OTHERWISE SPECIFIED

ORDERING INFORMATION

W P F 29 162 - 100 X 8 X I

FLASH MANUFACTURER:
I = Intel

RESET:
V = $\overline{\text{RESET}}$ tied to Vcc
P = $\overline{\text{RESET}}$ tied to Power Supervisor Circuit
R = $\overline{\text{RESET}}$ tied to pin 7 (not JEDEC Standard)

V_{PP} PROGRAMMING VOLTAGE
8 = 5V Vcc / 5V V_{PP}

LEAD FINISH:
G = Gold Edge Connectors
T = Tin Edge Connectors

ACCESS TIME (ns)

ORGANIZATION, 4M x 32

MECHANICAL OPTIONS
29 = 80 pin SIMM with TSOP Components

Flash PROM

Plastic Module

WHITE MICROELECTRONICS