1M x32 FLASH SIMM

*PRELIMINARY**

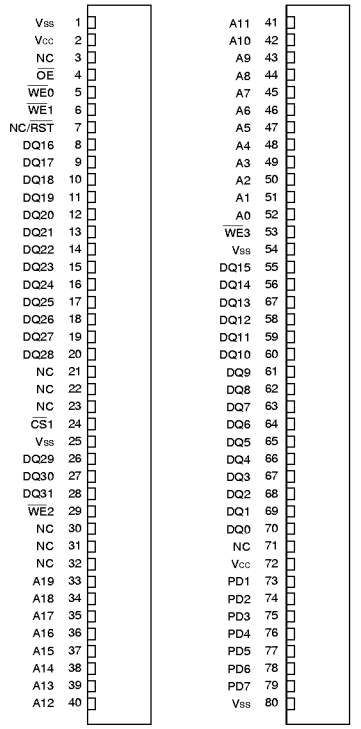
FEATURES

- Access Time of 90ns
- Packaging:
  - 80 pin SIMM
  - 80 pin SIMM, Low profile **
  - The module is manufactured with four 1M x8 CMOS flash memory devices in TSOP on a laminate substrate.
- JEDEC standard
- Reset control options:
  - $\overline{\text{RESET}}$ tied to Vcc
  - $\overline{\text{RESET}}$ tied to pin 7 for system control of reset
  - $\overline{\text{RESET}}$ tied to Power Supervisor Circuit.
- Sector Architecture
  - 16 equal size sectors of 64KBytes per each 1M x8 chip
  - Two step sequence of erase ensures that memory contents are not accidently erased.
- AMD Part Number Am29F080-90 Flash Memory Components
- 100,000 Erase/Program Cycles
- Organized as 1M x32
- Commercial Temperature Range
- 5 Volt Programming. 5V ± 10% Supply.
- Low Power CMOS (0 - 70°C)
- Built-in Decoupling Caps and Multiple Ground Pins for Low Noise Operation, Separate Power and Ground Planes to improve noise immunity
- Standard Programming Algorithms for AMD Am29F080 Flash

* *This data sheet describes a product under development, not fully characterized, and is subject to change without notice.*

** *Package to be developed.*

FIG. 1 PIN CONFIGURATION FOR WPF1M32X-90XC5



PIN DESCRIPTION

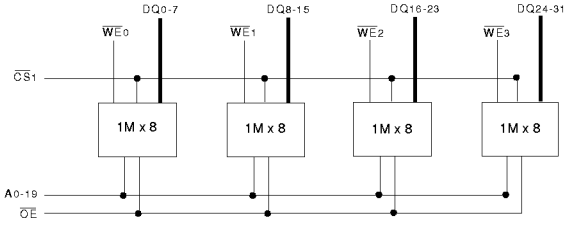
DQ_{0-31}	Data Inputs/Outputs
A_{0-19}	Address Inputs
$\overline{WE}_{0-3}$	Write Enables
$\overline{CS}_1$	Chip Enable
$\overline{OE}$	Output Enable
$\overline{RST}$	Reset (optional)
Vcc	Power Supply
Vss	Ground
PD_{1-7}	Presence Detects
NC	No Connect

Presence Detect

Speed	PD1	PD2	PD3	PD4	PD5	PD6	PD7
90ns	1	0	1	0	1	1	0

0: GND 1: Open

BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Ratings	Unit
Voltage on Any Pin Relative to Vss (except Vcc)	V_T	-2.0 to +7.0	V
Power Dissipation	P_T	1.32	W
Operating Temperature	T_A	0 to +70	°C
Storage Temperature	Tstg	-65 to +125	°C
Short Circuit Output Current	Ios	200	mA

CAPACITANCE

(T_A = +25°C)

Parameter	Symbol	Conditions	Max	Unit
$\overline{OE}$ capacitance	C_{OE}	V_{IN} = 0 V, f = 1.0 MHz	60	pF
$\overline{WE}$ capacitance	C_{WE}	V_{IN} = 0 V, f = 1.0 MHz	20	pF
$\overline{CS}$ capacitance	C_{CS}	V_{IN} = 0 V, f = 1.0 MHz	50	pF
Data I/O capacitance	$C_{I/O}$	$V_{I/O}$ = 0 V, f = 1.0 MHz	18	pF
Address input capacitance	C_{AD}	V_{IN} = 0 V, f = 1.0 MHz	60	pF

This parameter is guaranteed by design but not tested.

RECOMMENDED DC OPERATING CONDITIONS

Parameter	Symbol	Min	Typ	Max	Unit
Supply Voltage	V_{CC}	4.5	5.0	5.5	V
Ground	Vss	0	0	0	V
Input High Voltage	V_{IH}	0.7 x Vcc	-	Vcc + 0.3	V
Input Low Voltage	V_{IL}	-0.5	-	+0.8	V
Voltage for Autoselect and Sector Unprotect	V_{ID}	11.5	-	12.5	V

DC CHARACTERISTICS - CMOS COMPATIBLE

(V_{CC} = 5.0V, V_{SS} = 0V, T_A = 0°C to +70°C)

Parameter	Symbol	Conditions	Min	Max	Unit
Input Leakage Current	I_{LI}	V_{CC} = 5.5, V_{IN} = Vss or Vcc		10	µA
Output Leakage Current	I_{LO}	V_{CC} = 5.5, V_{IN} = Vss or Vcc		10	µA
Vcc Active Current for Read (1)	I_{CC1}	$\overline{CS}$ = V_{IL}, $\overline{OE}$ = V_{IH}, f = 5MHz		120	mA
Vcc Active Current for Program or Erase (2)	I_{CC2}	$\overline{CS}$ = V_{IL}, $\overline{OE}$ = V_{IH}		240	mA
Vcc Standby Current	I_{CC4}	V_{CC} = 5.5, $\overline{CS}$ = V_{IH}, f = 5MHz		1.0	mA
Vcc Static Current	I_{CC3}	V_{CC} = 5.5, $\overline{CS}$ = V_{IH}		20	µA
Output Low Voltage	V_{OL}	I_{OL} = 12.0 mA, Vcc = 4.5		0.45	V
Output High Voltage	V_{OH1}	I_{OH} = -2.5 mA, Vcc = 4.5	0.85 x Vcc		V
Low Vcc Lock-Out Voltage	V_{LKO}		3.2	4.2	V

NOTES:

1. The Icc current listed includes both the DC operating current and the frequency dependent component (at 5 MHz). The frequency component typically is less than 2 mA/MHz, with $\overline{OE}$ at V_{IH}.
2. Icc active while Embedded Algorithm (program or erase) is in progress.
3. DC test conditions: V_{IL} = 0.3V, V_{IH} = Vcc - 0.3V

AC CHARACTERISTICS – WRITE/ERASE/PROGRAM OPERATIONS, $\overline{WE}$ CONTROLLED

(V_{CC} = 5.0V, T_A = 0°C to +70°C)

Parameter	Symbol		-90		Unit
			Min	Max	
Write Cycle Time	t_{AVAV}	t_{WC}	90		ns
Chip Select Setup Time	t_{ELWL}	t_{CS}	0		ns
Write Enable Pulse Width	t_{WLWH}	t_{WP}	45		ns
Address Setup Time	t_{AVWH}	t_{AS}	0		ns
Data Setup Time	t_{DVWH}	t_{DS}	45		ns
Data Hold Time	t_{WHDX}	t_{DH}	0		ns
Address Hold Time	t_{WHAX}	t_{AH}	45		ns
Write Enable Pulse Width High	t_{WHWL}	t_{WPH}	20		ns
Duration of Byte Programming Operation	t_{WHWH1}			1.0	ms
Sector Erase Time	t_{WHWH2}			15	sec
Read Recovery Time before Write	t_{GHWL}		0		µs
Vcc Set-up Time	t_{VCS}		50		µs
Chip Programming Time				50	sec
Output Enable Setup Time		t_{OES}	0		ns
Output Enable Hold Time (1)		t_{OEH}	10		ns
Chip Erase Time				240	sec
$\overline{RESET}$ Pulse Width (2)		t_{RP}	500		ns

1. For Toggle and Data Polling.
2. Reset optional.

AC CHARACTERISTICS – READ ONLY OPERATIONS

(V_{CC} = 5.0V, T_A = 0°C to +70°C)

Parameter	Symbol		-90		Unit
			Min	Max	
Read Cycle Time	t_{AVAV}	t_{RC}	90		ns
Address Access Time	t_{AVQV}	t_{ACC}		90	ns
Chip Select Access Time	t_{ELQV}	t_{CE}		90	ns
Output Enable to Output Valid	t_{GLQV}	t_{OE}		40	ns
Chip Select to Output High Z (1)	t_{EHQZ}	t_{DF}		20	ns
Output Enable High to Output High Z (1)	t_{GHQZ}	t_{DF}		20	ns
Output Hold from Address, $\overline{CS}$ or $\overline{OE}$ Change, whichever is First	t_{AXQX}	t_{OH}	0		ns
$\overline{RST}$ Low to Read Mode (1) (2)		t_{Ready}		20	µs

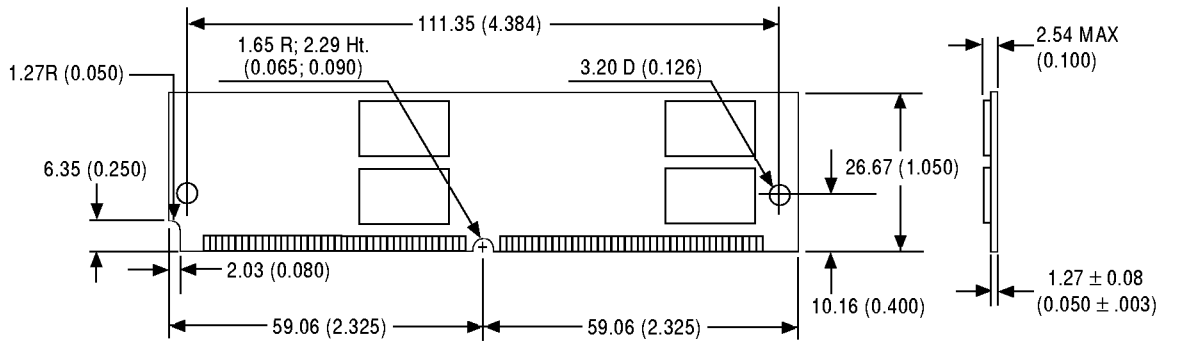
1. Guaranteed by design, but not tested.
2. Reset optional.

AC CHARACTERISTICS – WRITE/ERASE/PROGRAM OPERATIONS, $\overline{CS}$ CONTROLLED

(V_{CC} = 5.0V, V_{SS} = 0V, T_A = 0°C to +70°C)

Parameter	Symbol		-90		Unit
			Min	Max	
Write Cycle Time	t_{AVAV}	t_{WC}	90		ns
Write Enable Setup Time	t_{WLEL}	t_{WS}	0		ns
Chip Select Pulse Width	t_{ELEH}	t_{CP}	45		ns
Address Setup Time	t_{AVEL}	t_{AS}	0		ns
Data Setup Time	t_{DVEH}	t_{DS}	45		ns
Data Hold Time	t_{EHDX}	t_{DH}	0		ns
Address Hold Time	t_{ELAX}	t_{AH}	45		ns
Chip Select Pulse Width High	t_{EHEL}	t_{CPH}	20		ns
Duration of Byte Programming Operation	t_{WHWH1}			1.0	ms
Sector Erase Time	t_{WHWH2}			15	sec
Read Recovery Time	t_{GHEL}		0		µs
Chip Programming Time				50	sec
Chip Erase Time				240	sec

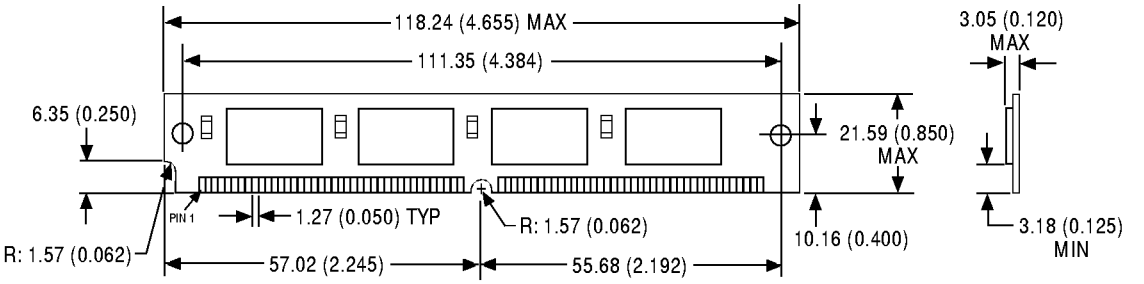
PACKAGE DIMENSION: 80-PIN SIMM



±0.13 (±0.005) TOLERANCE UNLESS OTHERWISE SPECIFIED

ALL LINEAR DIMENSIONS ARE MILLIMETERS AND PARENTHETICALLY IN INCHES

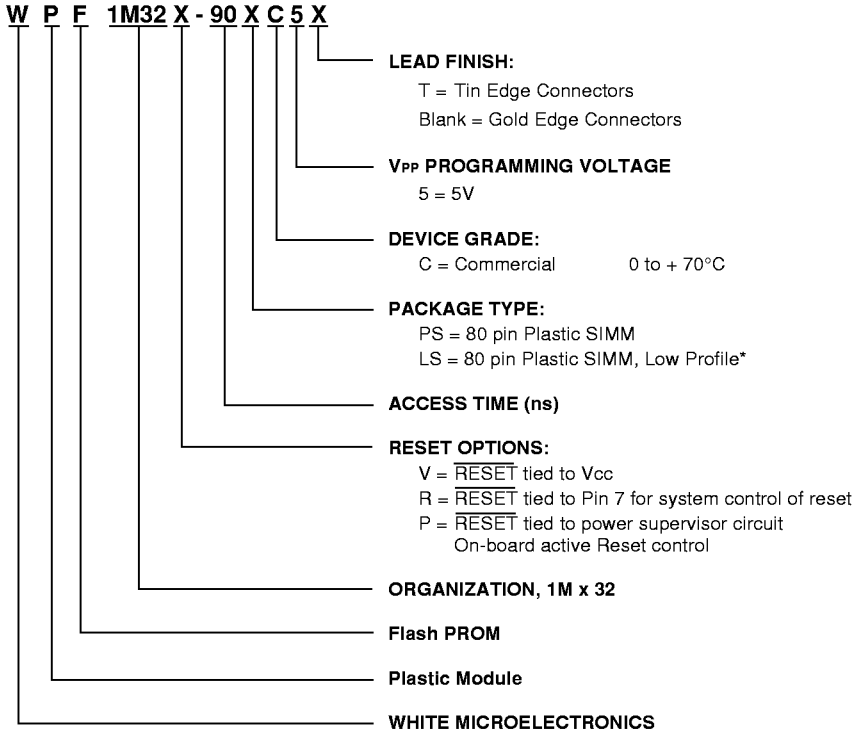
PACKAGE DIMENSION: 80-PIN SIMM, LOW PROFILE



±0.13 (±0.005) TOLERANCE UNLESS OTHERWISE SPECIFIED

ALL LINEAR DIMENSIONS ARE MILLIMETERS AND PARENTHETICALLY IN INCHES

ORDERING INFORMATION



* *Package to be developed.*