3-V to 20-V Integrated FET Hot Swap

Check for Samples: TPS2421-1, TPS2421-2

FEATURES

- **Integrated Pass MOSFET**
- **3.3-V to 20-V Bus Operation**
- **Programmable Fault Current**
- **Current Limit Proportionally Larger than Fault Current**
- **Programmable Fault Timer**
- **Internal MOSFET Power Limiting**
- **Latch-Off on Fault (-1) and Retry (-2) Versions**
- **SO-8 PowerPad™ Package**
- **–40°C to 125°C Junction Temperature Range**
- **UL Listed - File Number E169910**

APPLICATIONS

- **RAID Arrays**
- **Telecommunications**
- **Plug-In Circuit Boards**
- **Disk Drive**

DESCRIPTION

The TPS2421 provides highly integrated hot swap power management and superior protection in applications where the load is powered by voltages between 3.0 V and 20 V. These devices are very effective in systems where a voltage bus must be protected to prevent shorts from interrupting or damaging the unit. The TPS2421 is an easy to use devices in an 8-pin PowerPad™ SO-8 package.

The TPS2421 has multiple programmable protection features. Load protection is accomplished by a non-current limiting fault threshold, a hard current limit, and a fault timer. The current dual thresholds allow the system to draw short high current pulses, while the fault timer is running, without causing a voltage droop at the load. An example of this is a disk drive startup. This technique is ideal for loads that experience brief high demand, but benefit from protection levels in-line with their average current draw.

Hotswap MOSFET protection is provided by power limit circuitry which protects the internal MOSFET against SOA related failures.

The TPS2421 is available in latch-off on fault (-1) and retry on fault (-2).

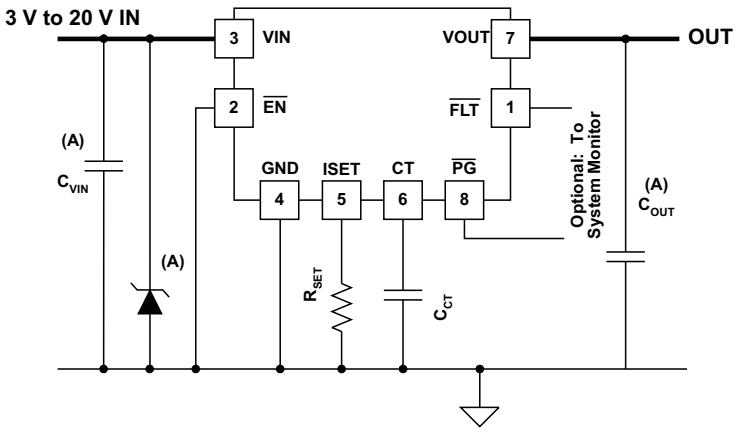


Figure 1. Typical Application

NOTE

(A) Required only in systems with lead and/or load inductance.

Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

PowerPad is a trademark of Texas Instruments.

PRODUCT INFORMATION(1)

DEVICE	FEATURE	PACKAGE	MARKING
TPS2421-1	Latchoff	DDA (SO8 PowerPad™)	2421-1
TPS2421-2	Auto-retry		2421-2

(1) For the most current package and ordering information, see the Package Option Addendum at the end of this document, or visit the device product folder on www.ti.com.

ABSOLUTE MAXIMUM RATINGS

over operating free-air temperature range (unless otherwise noted) (1) (2)

		VALUE	UNIT
V_{IN}, V_{OUT}	Input voltage range	–0.3 to 25	V
$\overline{FLT}$, $\overline{PG}$	Voltage range	–0.3 to 20	
I_{SET}, C_T	Voltage	1.75	
I_{MAX}	Maximum continuous output current	9	A
$\overline{FLT}$, $\overline{PG}$	Output sink current	10	mA
$\overline{EN}$	Input voltage range	–0.3 to 6	V
CT,(3) ISET(3)	Voltage range	-0.3 to 3	
	ESD rating, HBM	2.5	kV
	ESD rating, CDM	400	V
T_J	Operating junction temperature range	Internally Limited	°C
T_{stg}	Storage temperature range	–65 to 150	

(1) Stresses beyond those listed under *absolute maximum ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *recommended operating conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) All voltage values are with respect to GND.
(3) Do not apply voltage to these pins.

DISSIPATION RATINGS(1)

PACKAGE	θ_{JA} LOW K, °C/W	θ_{JA} HIGH K, °C/W	θ_{JA} BEST(2), °C/W
DDA	190(3)	45(4)	45

(1) Tested per JEDEC JESD51, natural convection. The definitions of high-k and low-k are per JESD 51-7 and JESD 51-3.
(2) The best case thermal resistance is obtained using the recommendations per SLMA002A (2 signal – 2 plane with the pad connected to the plane).
(3) Low-k (2 signal – no plane, 3 in. by 3 in. board, 0.062 in. thick, 1 oz. copper) test board with the pad soldered, and an additional 0.12 in.2 of top-side copper added to the pad.
(4) High-k is a (2 signal – 2 plane) test board with the pad soldered.

RECOMMENDED OPERATING CONDITIONS

		MIN	NOM	MAX	UNIT
V_{IN}, V_{OUT}	Input voltage range	3		20	V
$\overline{EN}$	Voltage range	0		5	
$\overline{FLT}$, $\overline{PG}$	Voltage range	0		20	
I_{OUT}	Continuous output current	0		6	A
$\overline{FLT}$, $\overline{PG}$	Output sink current	0		1	mA
C_{CT}		100		10	pF/µF
	Junction temperature	–40		125	°C

ELECTRICAL CHARACTERISTICS

Unless otherwise noted: 3 V ≤ V_{IN} ≤ 18 V, $\overline{EN}$ = 0 V, $\overline{PG}$ = $\overline{FLT}$ = open, R_{OUT} = open, C_{LOAD} = 0, R_{SET} = 49.9 kΩ, –40°C ≤ T_J ≤ 125°C

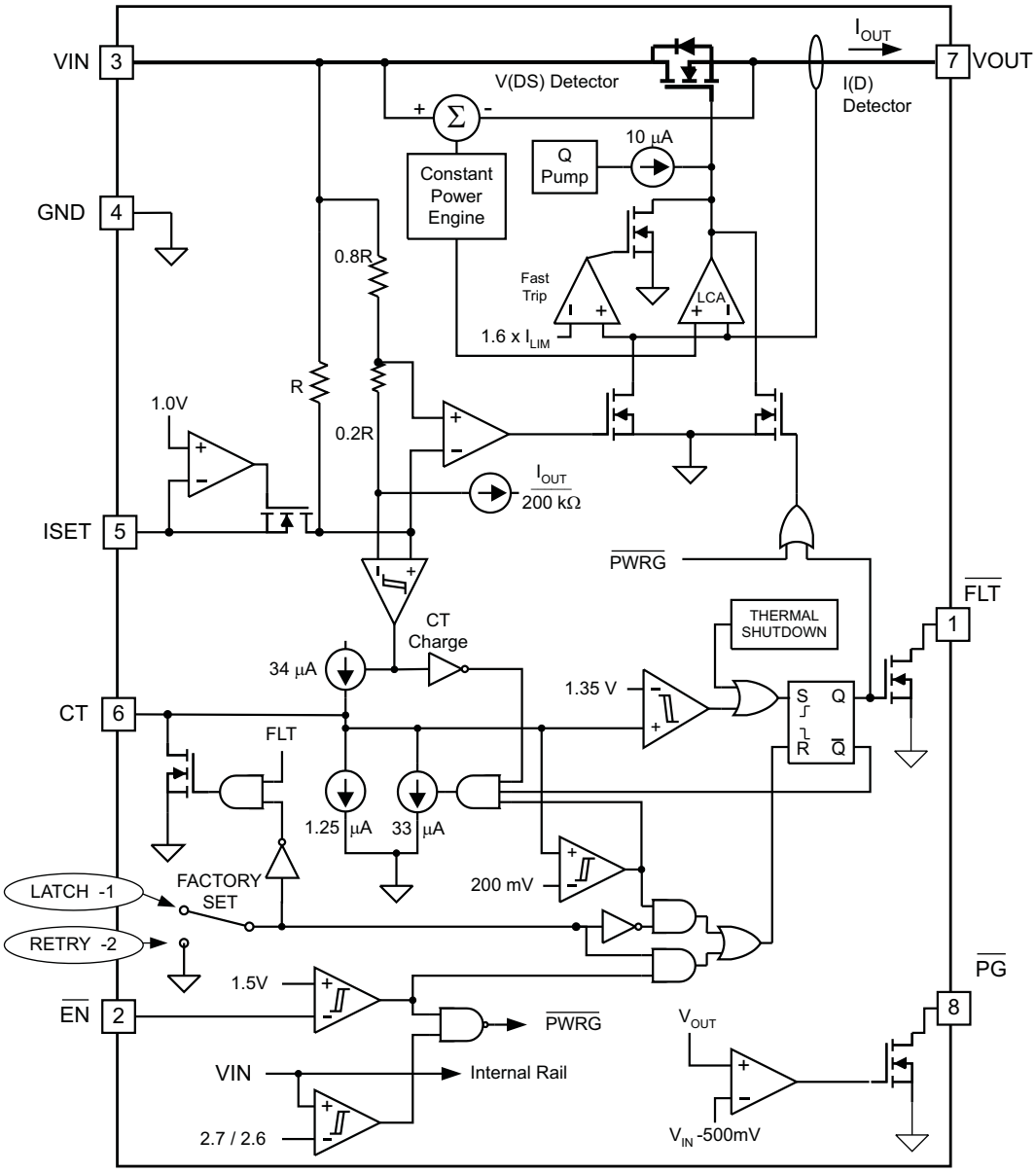
	PARAMETER	TEST CONDITIONS		MIN	TYP	MAX	UNIT
	VIN						
	UVLO	VIN rising		2.6	2.85	2.9	V
		Hysteresis			150		mV
	Bias current	$\overline{EN}$ = 2.4V			25	100	µA
		$\overline{EN}$ = 0V			3.9	5	mA
	VIN, VOUT						
	R_{ON}	$R_{VIN-VOUT}$, I_{VOUT} < I_{RMAX} or I_{VOUT} < (I_{SET} × 1.25), 1 A ≤ I_{VOUT} ≤ 4.5 A			33	50	mΩ
	Power limit TPS242x	V_{IN}: 12 V, C_{OUT} = 1000 µF $\overline{EN}$: 3 V → 0 V		3	5	7.5	V
	Reverse diode voltage	V_{OUT} > V_{IN} , $\overline{EN}$ = 5 V, I_{IN} = –1 A			0.77	1.0	
	ISET						
I_{SET}	Fault current threshold	I_{VOUT} ↑, I_{CT}: sinking → sourcing, pulsed test					A
		0°C ≤ T_J ≤ 85°C	R_{RSET} = 200 kΩ	0.80		1.2	
			R_{RSET} = 100 kΩ	1.80		2.2	
			R_{RSET} = 49.9 kΩ	3.60		4.40	
		-40°C ≤ T_J ≤ 125°C	R_{RSET} = 200 kΩ	0.75		1.25	
			R_{RSET} = 100 kΩ	1.75		2.25	
			R_{RSET} = 49.9 kΩ	3.60		4.40	
I_{LIM} / I_{FLT}	Ratio I_{LIM} / I_{FLT}	R_{RSET} = 200 kΩ		1.1	1.8	2.6	–
		R_{RSET} = 100 kΩ		1.1	1.5	2.1	
		R_{RSET} = 49.9 kΩ		1.1	1.4	1.6	
I_{LIM}	Current limit	I_{VOUT} rising, $V_{VIN-VOUT}$ = 0.3 V, pulsed test	R_{RSET} = 200 kΩ	1.1	1.8	2.4	
			R_{RSET} = 100 kΩ	2.3	3.0	3.7	A
			R_{RSET} = 49.9 kΩ	4.6	5.5	6.3	
	CT						
	Charge/discharge current	I_{CT} sourcing, V_{CT} = 1 V, In current limit		29	35	41	µA
		I_{CT} sinking, V_{CT} = 1 V, drive CT to 1 V, measure current		1.0	1.4	1.8	
	Threshold voltage	V_{CT} rising		1.3	1.4	1.5	V
		V_{CT} falling, drive CT to 1 V, measure current		0.1	0.16	0.3	
	ON/OFF fault duty cycle	V_{VOUT} = 0 V		2.8%	3.7%	4.6%	

ELECTRICAL CHARACTERISTICS (continued)

Unless otherwise noted: 3 V ≤ V_{IN} ≤ 18 V, $\overline{EN}$ = 0 V, $\overline{PG}$ = $\overline{FLT}$ = open, R_{OUT} = open, C_{LOAD} = 0, R_{SET} = 49.9 kΩ, –40°C ≤ T_J ≤ 125°C

	PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
	$\overline{EN}$					
	Threshold voltage	$V_{\overline{EN}}$ falling	0.8	1.0	1.5	V
		Hysteresis	20	150	250	mV
	Input bias current	$\overline{VEN}$ = 2.4 V	–2.0	0	0.5	µA
		$\overline{VEN}$ = 0.2 V	–3.0	1	0.5	
	Turn on propagation delay	V_{IN} = 3.3 V, I_{LOAD} = 1 A, $V_{\overline{EN}}$: 2.4 V → 0.2 V, V_{OUT}: rising 90% × V_{IN}		350	500	µs
	Turn off propagation delay	V_{IN} = 3.3 V, I_{LOAD} = 1 A, $V_{\overline{EN}}$: 0.2 V → 2.4 V, V_{OUT}: ↓ 10% × V_{IN}		30	50	
	$\overline{FLT}$					
V_{OL}	Low level output voltage	V_{CT} = 1.8 V, $I_{\overline{FLT}}$ = 1 mA		0.2	0.4	V
	Leakage current	$V_{\overline{FLT}}$ = 18 V			1	µA
	$\overline{PG}$					
	PG threshold	$V_{(VIN-VOUT)}$ falling	0.4	0.5	0.75	V
		Hysteresis	0.1	0.25	0.4	
V_{OL}	Low level output voltage	$I_{\overline{PG}}$ = 1 mA		0.2	0.4	
	Leakage current	$V_{\overline{PG}}$ = 18 V			1	µA
	Thermal Shutdown					
	Thermal shutdown	Junction temperature rising		160		°C
		Hysteresis		10		

BLOCK DIAGRAM



PINOUT DIAGRAM

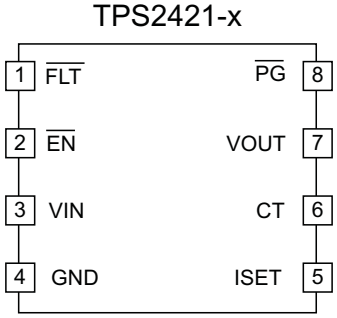


Table 1. TERMINAL FUNCTIONS

FUNCTION	PIN NO.	DESCRIPTION
$\overline{FLT}$	1	Fault low indicated the fault time has expired and the FET is switched off
$\overline{EN}$	2	Device is enabled when this pin is pulled low
VIN	3	Power In and control supply voltage
GND	4	GND
ISET	5	A resistor to ground sets the fault current, the current limit is 125% of the fault current. TPS2421 only
CT	6	A capacitor to ground sets the fault time
VOUT	7	Output to the load
$\overline{PG}$	8	Power Good low represents the output voltage is within 300 mV of the input voltage

PIN DESCRIPTION

CT: Connect a capacitor form CT to GND to set the fault time. The fault timer starts when the fault current threshold is exceeded, charging the capacitor with 36 μA from GND towards an upper threshold of 1.4 V. If the capacitor reaches the upper threshold, the internal pass MOSFET is turned off. The MOSFET will stay off until $\overline{EN}$ is cycled if a latching version is used. If an auto-retry version is used, the capacitor will discharge at 5 μA to 0.2 V and then re-enable the pass MOSFET. When the device is disabled, CT is pulled to GND through a 100-kΩ resistor.

The timer period must be chosen long enough to allow the external load capacitance to charge. The fault timer period is selected using Equation 1 where T_{FAULT} is the minimum timer period in seconds and C_{CT} is in Farads.

$$C_{CT} = \frac{T_{FAULT}}{38.9 \cdot 10^3} \tag{1}$$

This equation does not account for component tolerances. In autoretry versions, the second and subsequent retry timer periods will be approximately 85% as long as the first retry period.

In autoretry versions, the fault timer discharges the capacitor for a nominal T_{SD} in seconds with C_{CT} in Farads per Equation 2.

$$T_{SD} = 1.0 \times 10^6 \times C_{CT} \tag{2}$$

The nominal ratio of on to off times represents about a 3% duty cycle when a hard fault is present on the output of an autoretry version part.

$\overline{FLT}$: Open-drain output that pulls low on any condition that causes the output to open. These conditions are either an overload with a fault time-out, or a thermal shutdown. $\overline{FLT}$ becomes operational before UV, when V_{IN} is greater than 1 V.

GND: This is the most negative voltage in the circuit and is used as reference for all voltage measurements unless otherwise specified.

ISET: A resistor from this pin to GND sets both the fault current (I_{FAULT}) and current limit (I_{MAX}) levels. The current limit is internally set at 125% of the fault current. The fault timer function on C_T starts charging C_T if I_{VIN} exceeds the programmed fault current. If this current continues long enough for V_{CT} to reach its upper trip threshold, the output is turned off. If I_{VIN} falls below the fault current threshold before C_T reaches its upper threshold, C_T is discharged and normal operation continues.

The internal MOSFET actively limits current if I_{VIN} reaches the current limit set point. The fault timer operation is the same in this mode as described previously.

The fault current value is programmed as follows;

$$R_{IFLT} = \frac{200\ k\Omega}{I_{FAULT}} \tag{3}$$

$\overline{\text{EN}}$: When this pin is pulled low, the device is enabled. The input threshold is hysteretic, allowing the user to program a startup delay with an external RC circuit. $\overline{\text{EN}}$ is pulled to V_{IN} by a 10-MΩ resistor, pulled to GND by 16.8 MΩ and is clamped to ground by a 7-V Zener diode. Because high impedance pullup/down resistors are used to reduce current draw, any external FET controlling this pin should be low leakage.

If $\overline{\text{EN}}$ is tied to GND at startup and V_{IN} does not ramp quickly the TPS2421 may momentarily turn off then on during startup. This can happen if a capacitive load momentarily pulls down the input voltage below the UV threshold. If necessary, this can be avoided by delaying $\overline{\text{EN}}$ assertion until V_{IN} is fully up.

V_{IN}: Input voltage to the TPS2421. The recommended operating voltage range is 3 V to 20 V. All VIN pins should be connected together and to the power source.

V_{OUT}: Output connection for the TPS2421. When switched on the output voltage will be approximately:

$$V_{OUT} = V_{IN} - 0.04 \times I_{OUT} \tag{4}$$

All V_{OUT} pins should be connected together and to the load.

$\overline{\text{PG}}$: Active low, Open Drain output, Power Good indicates that there is no fault condition and the output voltage is within 0.5 V of the input voltage. $\overline{\text{PG}}$ becomes operational before UV, whenever V_{IN} is greater than 1 V.

TYPICAL CHARACTERISTICS

FAULT CURRENT vs JUNCTION TEMPERATURE

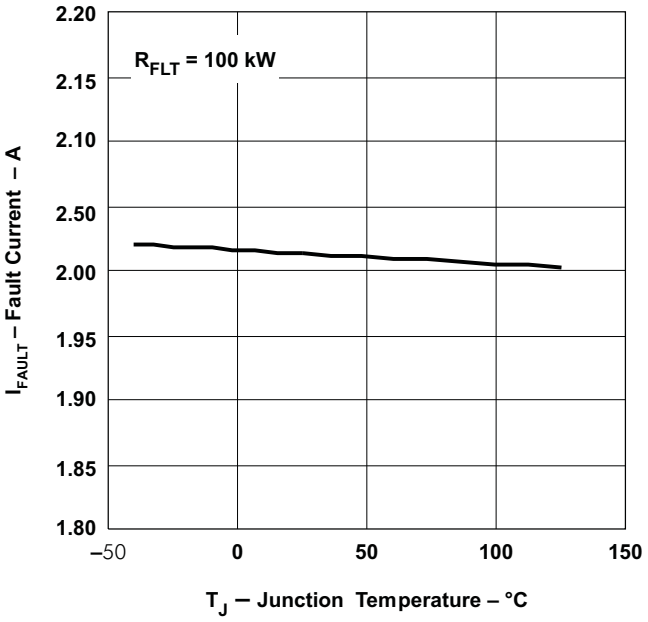


Figure 2.

FAULT TIMER THRESHOLD VOLTAGE vs JUNCTION TEMPERATURE

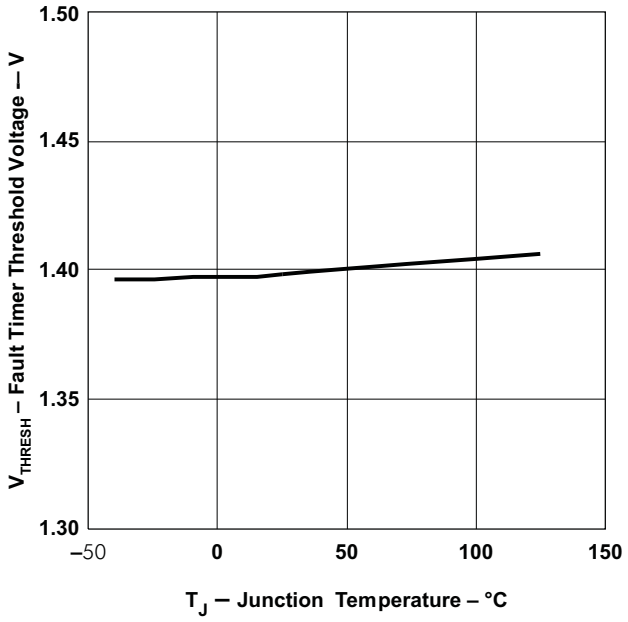


Figure 3.

POWER LIMIT vs JUNCTION TEMPERATURE

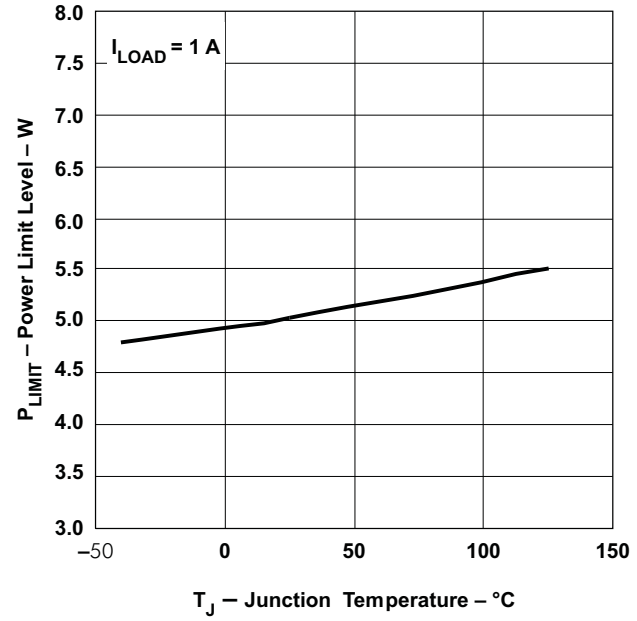


Figure 4.

SUPPLY CURRENT vs JUNCTION TEMPERATURE

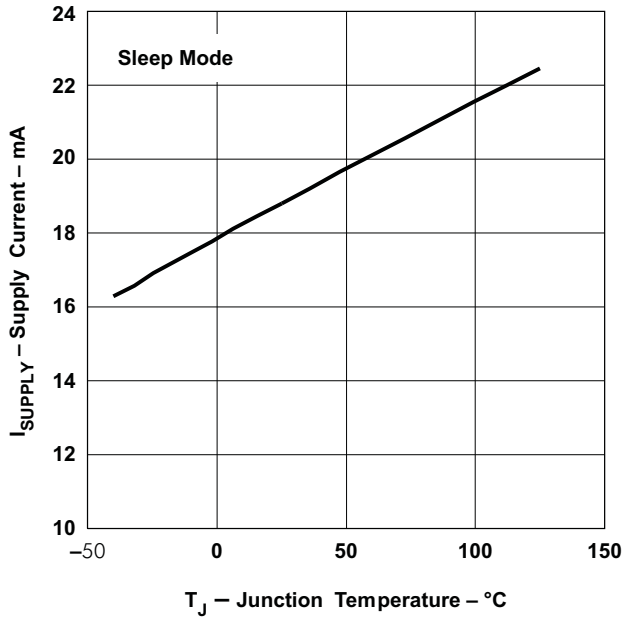


Figure 5.

TYPICAL CHARACTERISTICS (continued)

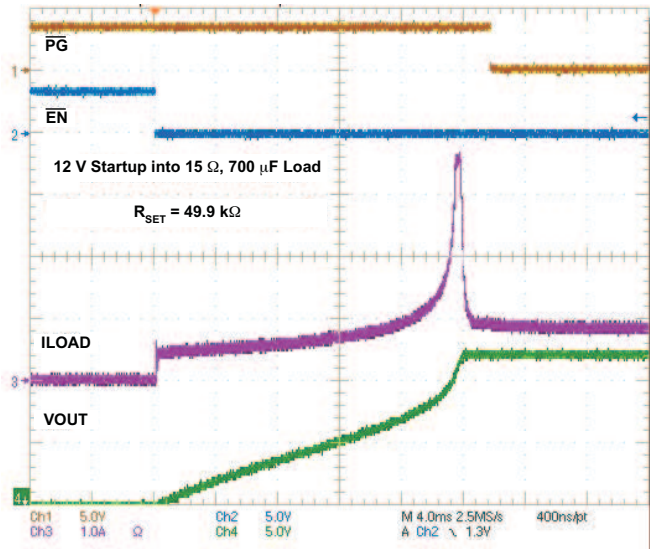


Figure 6. 12-V Startup Into 15 Ω, 700 µF Load

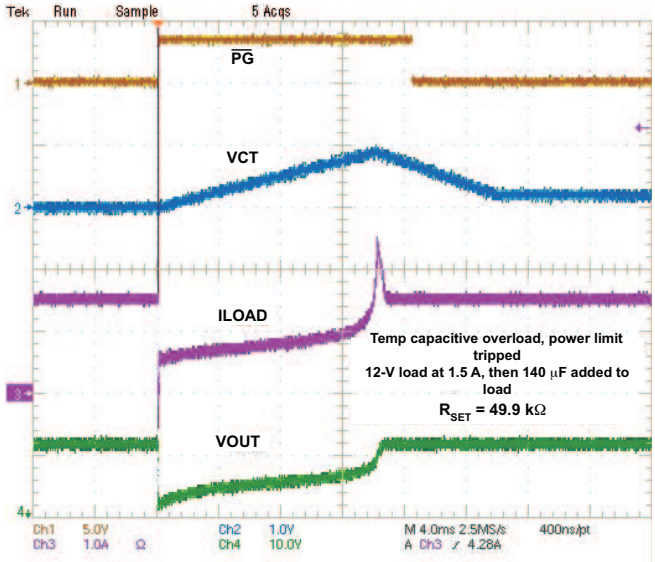


Figure 7. 12-V, 140 µF Added to 8 Ω Load

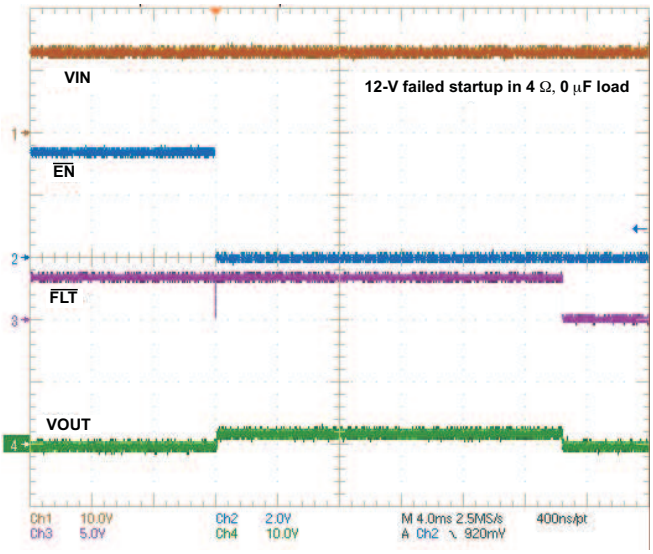


Figure 8. 12-V Faulted Startup Into 4 Ω Load

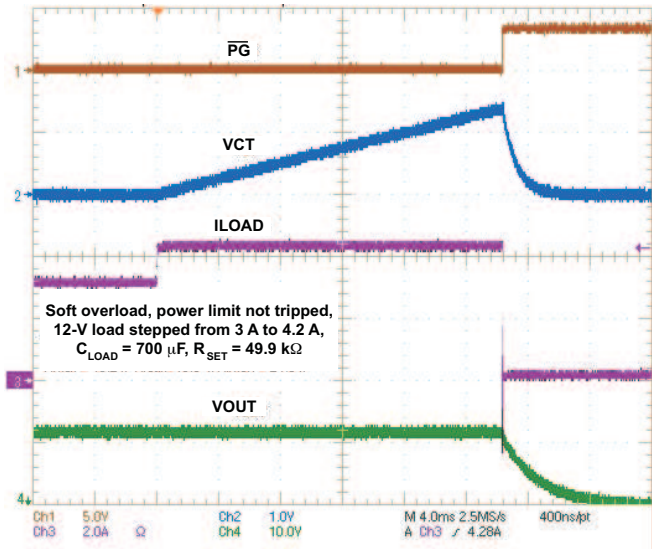


Figure 9. 12-V Soft Overload, 3 A to 4.2 A, Power Limit Not Tripped

TYPICAL CHARACTERISTICS (continued)

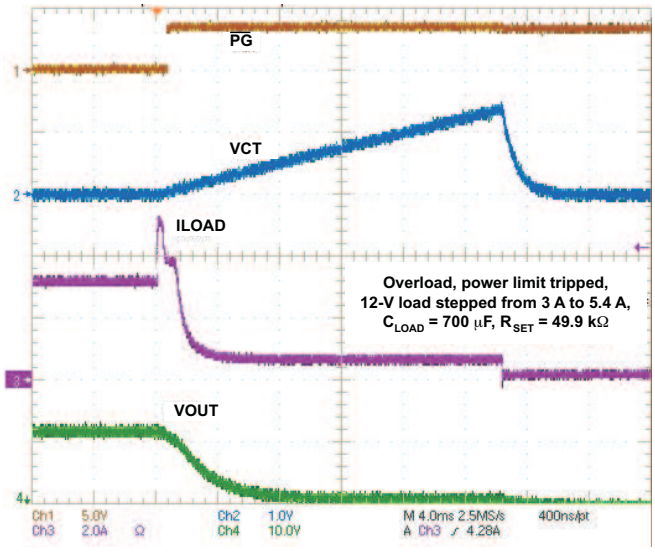


Figure 10. 12-V Firm Overload, 3 A to 5.4 A, Power Limit Tripped

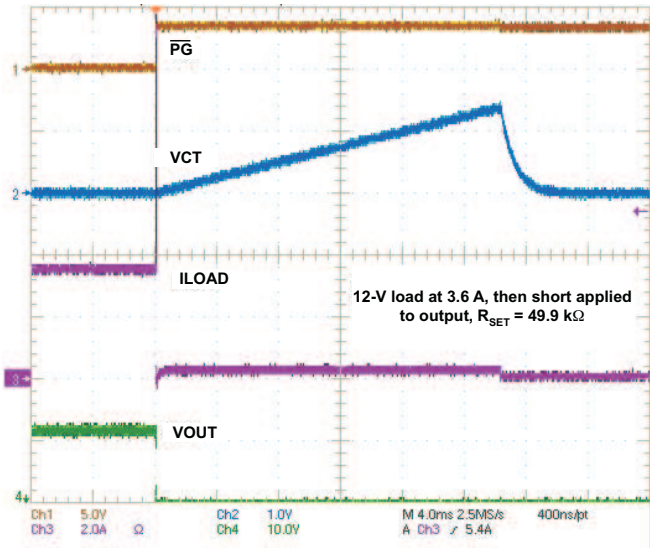


Figure 11. 12-V Hard Overload, 3.6-A LoaD Then Short

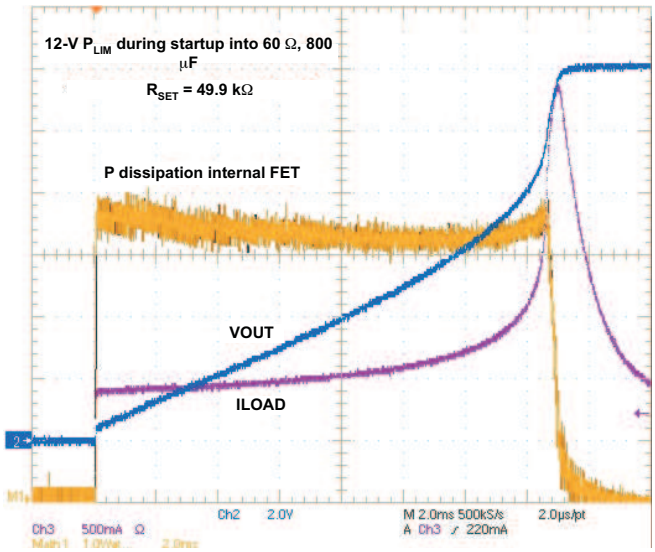


Figure 12. Power Dissipation During 12-V Startup into 60 Ω, 800 µF

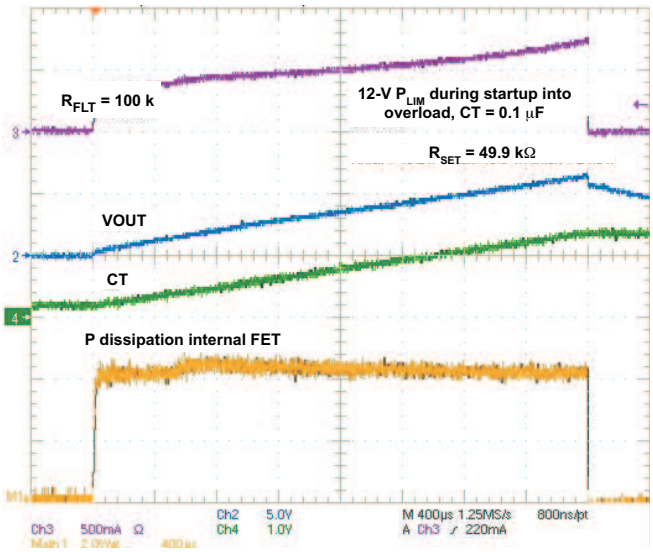


Figure 13. Power Dissipation During 12-V Startup into 15 Ω, 140 µF

TYPICAL CHARACTERISTICS (continued)

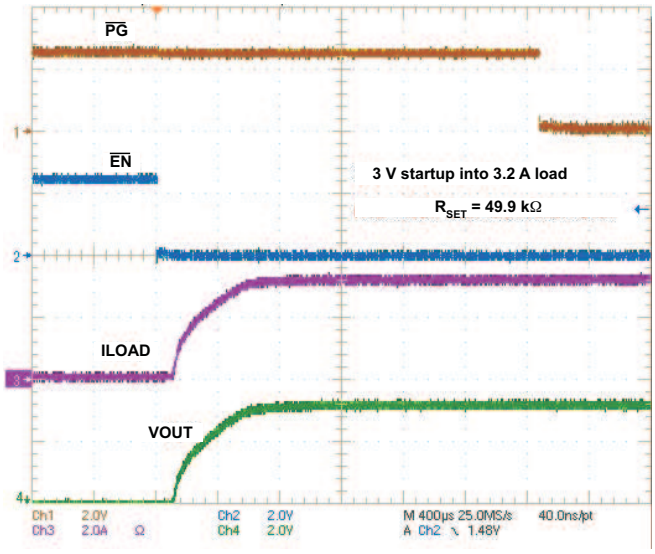


Figure 14. 3-V Startup into 1-Ω Load

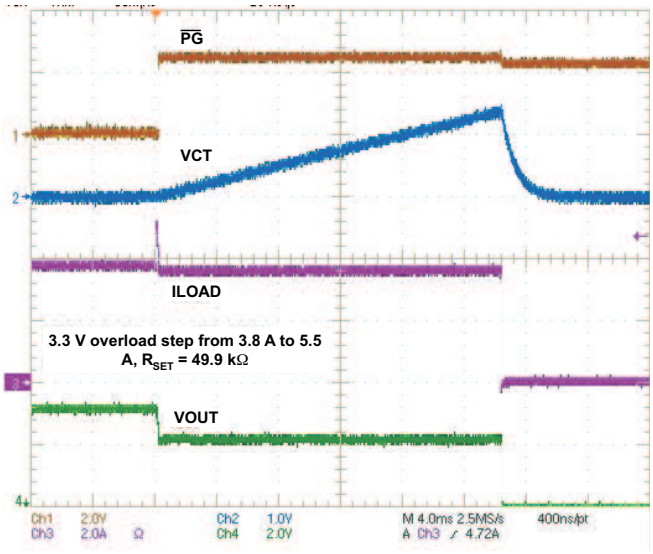


Figure 15. 3-V Firm Overload, Load Stepped From 3.8 A to 5.5 A

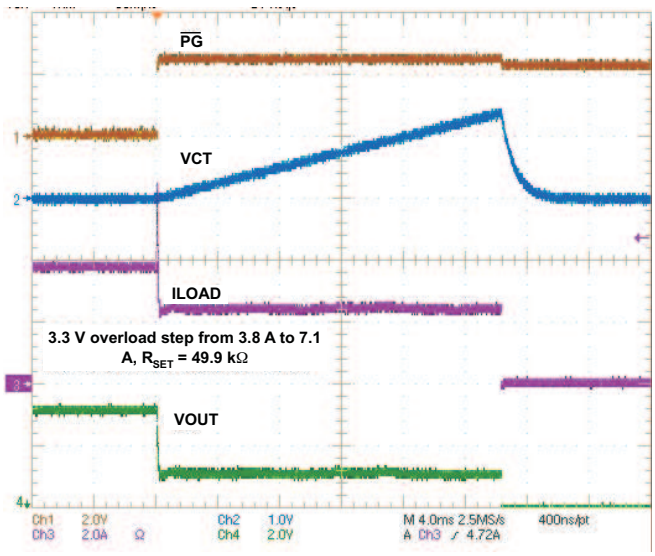


Figure 16. 3-V Hard Overload, Load Stepped From 3.8 A to 7.1 A

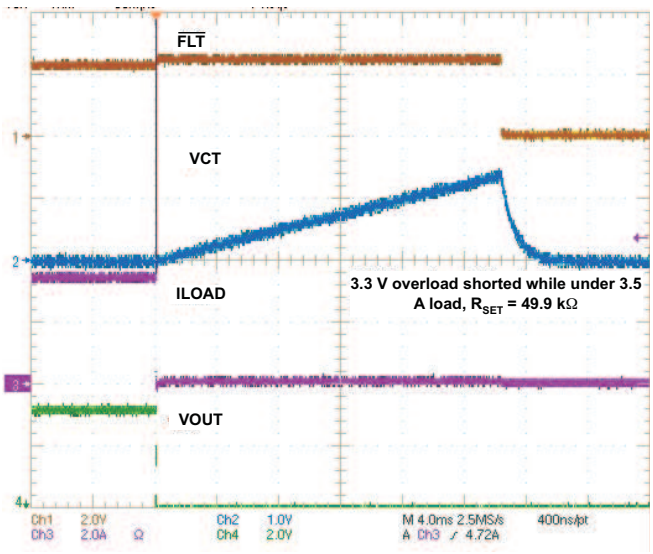


Figure 17. 3-V Output Shorted While Under 3.5-A Load

TYPICAL CHARACTERISTICS (continued)

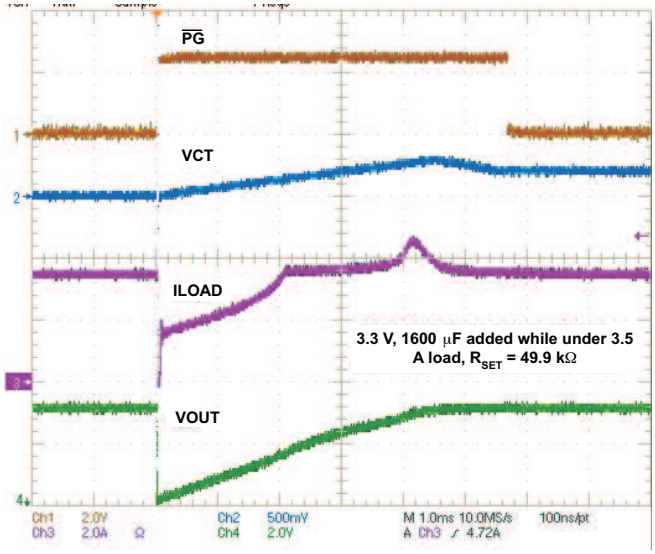


Figure 18. 3 V, 1600 µF Added To 3.5-A Load

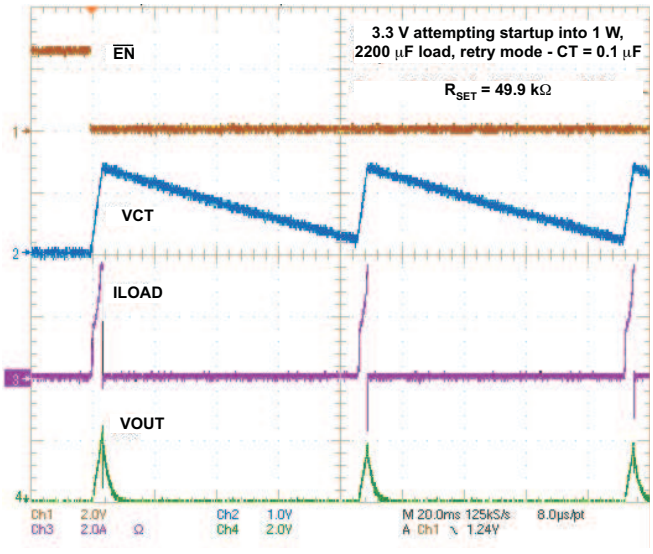


Figure 19. 3-V Retry Startup into 1 Ω, 2200-µF Load

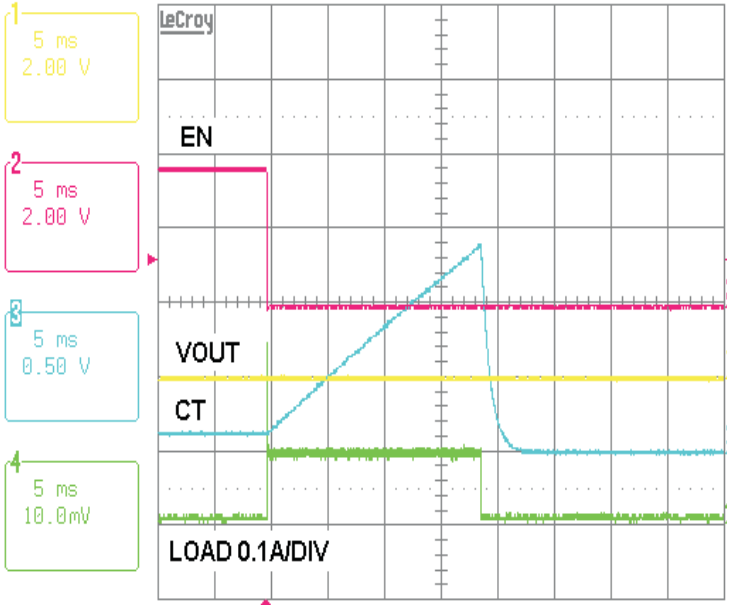


Figure 20. Startup Into a Short Circuit Output

APPLICATION INFORMATION

Maximum Load at Startup

The power limiting function of the TPS2421 provides very effective protection for the internal FET. Expectedly, there is a supply voltage dependent maximum load which the device will be able to power up. Loads above this level may cause the device to shut off current before startup is complete. Neglecting any load capacitance, the maximum load (minimum load resistance) is calculated using the equation;

$$R_{MIN} = \frac{V_{IN}^2}{12} \quad (5)$$

Adding load capacitance may reduce the maximum load which can be present at start up.

If $\overline{EN}$ is tied to GND at startup and V_{IN} does not ramp quickly the TPS2421 may momentarily turn off then on during startup. This can happen if a capacitive load momentarily pulls down the input voltage below the UV threshold. If necessary, this can be avoided by delaying $\overline{EN}$ assertion until V_{IN} is fully up.

Transient Protection

The need for transient protection in conjunction with hot-swap controllers should always be considered. When the TPS2421 interrupts current flow, input inductance generates a positive voltage spike on the input and output inductance generates a negative voltage spike on the output. Such transients can easily exceed twice the supply voltage if steps are not taken to address the issue. Typical methods for addressing transients include;

- Minimizing lead length/inductance into and out of the device
- Voltage Suppressors (TVS) on the input to absorb inductive spikes
- Shottky diode across the output to absorb negative spikes
- A combination of ceramic and electrolytic capacitors on the input and output to absorb energy
- Use PCB GND planes

The following equation estimates the magnitude of these voltage spikes:

$$V_{SPIKE(absolute)} = V_{NOM} + I_{LOAD} \times \sqrt{L/C} \quad (6)$$

where

- V_{NOM} is the nominal supply voltage
- I_{LOAD} is the load current
- C is the capacitance present at the input or output of the TPS2421
- L equals the effective inductance seen looking into the source or the load

Calculating the inductance due to a straight length of wire is shown in Equation 7.

$$L_{straightwire} \approx 0.2 \times L \times \ln\left(\frac{4 \times L}{D} - 0.75\right) (nH) \quad (7)$$

where

- L is the length of the wire
- D is diameter of the wire

Some applications may require the addition of a TVS to prevent transients from exceeding the absolute ratings if sufficient capacitance cannot be included.

Operation

When load current exceeds the user programmed fault limit (I_{SET}) during normal operation the fault timer starts. If load current drops below the I_{SET} threshold before the fault timer expires, normal operation continues. If load current stays above the I_{SET} threshold the fault timer expires and a fault is declared. When a fault is declared a device operating in latch mode turns off and can be restarted by cycling power or toggling the $\overline{EN}$ signal. A device operating in retry mode attempts to turn on at a 3% duty cycle until the fault is cleared. When the I_{MAX} limit is reached during a fault the device goes into current limit and the fault timer keeps running. I_{MAX} is automatically set to 1.25 times I_{SET}.

Startup

When power is first applied to a load with discharged capacitors there is a large inrush current. The inrush is controlled by the TPS2421 by initially entering the power limit mode and turning on the fault timer. See Figure 13. As the charge builds on the capacitor, the current increases to I_{MAX}. When the capacitor is fully charged, current output is set by the dc load value, The fault timer is turned off. The FET is then fully enhanced and the power good signal is true.

In order to start properly, the fault timer must be set to exceed the capacitor charge time.

When the load has a resistive component as well as capacitive, the fault time needs to be increased because current to the resistive load is unavailable to charge the capacitor. The startup time for some selected loading is given in Table 2.

Table 2 data was taken with I_{SET} equal to 4 A. Lower current settings of TPS2421 do not have a great influence on the start up timer because of operation at power limit. Load capacitance and dc resistance was selected for a measured start time. The start time is measured from the assertion of the $\overline{EN}$ pin to the assertion of the $\overline{PG}$ pin.

Table 2. Start Time for Input Voltage and Output Loading (1)

INPUT VOLTAGE (V)	LOAD CAPACITANCE (μF)	DC LOAD RESISTANCE (Ω)	START TIME (ms)
5	220	OPEN	2.5
		5	2.7
		12	2.6
	1000	OPEN	4
		5	4
		12	4
12	220	OPEN	4.4
		5	No start
		12	7
	1000	OPEN	14
		5	No start
		12	23

(1) I_{SET} = 4 A

Some combinations of loading and current limit settings exceed the 5-W power limit of the internal MOSFET. The output voltage will not turn on regardless of the fault time setting. One way to work with the physical limits that create this problem is to allow the power manager to charge only the capacitive component of the load and use the $\overline{PG}$ signal to turn on the resistive component. This is common usage in dc-to-dc converters and other electrical equipment with power good inputs.

Start Up Into a Short

The controller attempts to power on into a short for the duration of the timer. Figure 20 shows a small current resulting from power limiting the internal MOSFET. This happens only once for the latch off part, TPS2421-1. For the retry part, TPS2421-2, Figure 19 shows this cycle repeating at an interval based on the C_T time.

Shutdown Modes

Hard Overload - Fast Trip

When a hard overload causes the load current to exceed ~1.6 × I_{SET} the TPS2421 immediately shuts off current to the load without waiting for the fault timer to expire. After such a shutoff the TPS2421 enters into startup mode and attempts to apply power to the load.

If the hard overload is caused by a current transient, then a normal startup can be expected with a low probability of disruption to the load, assuming there is sufficient load capacitance to hold up the load during the fractions of a millisecond that make up the fast trip/restart cycle.

If the hard overload is caused by a real, continuous failure then the TPS2421 goes into current limit during the attempt at restart. The timer starts and eventually runs out, shutting off current to the load. See the fast trip Figure 17. When the hard overload occurs the current is turned off, the $\overline{PG}$ pin becomes false, and the $\overline{FLT}$ pin stays false. The $\overline{FLT}$ pin becomes true only when the fault timer times out.

Overcurrent Shutdown

Overcurrent shutdown occurs when the output current exceeds I_{SET} for the duration of the fault timer. Figure 9 shows a step rise in output current which exceeds the I_{FLT} threshold but not the I_{MAX} threshold. The increased current is on for the duration of the timer. At conclusion of the timer, the output is turned off.

Layout

Support Components

Locate all TPS2421 support components, R_{SET}, C_T, etc. or any input or output voltage clamps, close to their connection pin. Connect the other end of the component to the inner layer GND without trace length.

PowerPad™

When properly mounted the PowerPad package provides significantly greater cooling ability than an ordinary package. To operate at rated power the Power Pad must be soldered directly to the PC board GND plane directly under the device. The PowerPad is at GND potential and can be connected using multiple vias to inner layer GND. Other planes, such as the bottom side of the circuit board can be used to increase heat sinking in higher current applications.

Refer to Technical Briefs: *PowerPAD™ Thermally Enhanced Package* (TI Literature Number SLMA002) and *PowerPAD™ Made Easy* (TI Literature Number SLMA004) for more information on using this PowerPadTM package.These documents are available at www.ti.com (Search by Keyword).

Design Example

This TPS2421 Design supports 12 V to operate a hot plugged disk drive.

The 12 V specification for a disk drive is approximately 1-A operating current and 2-A typical spin-up. Selecting a 2.5 A setting for I_{SET} would allow some margin for the operating current and satisfy the start current requirements.

Calculate R_{IFLT} using equation Equation 8 or select it using Table 3.

$$R_{IFLT} = \frac{200\,k\Omega}{I_{FAULT}} \times \frac{200{,}000}{2.5} = 80\ (k\Omega) \tag{8}$$

Because I_{SET} satisfies the spin up current, the timer can be set for the additional loading of charging the capacitor. Estimate approximately 20 ms. Use either Equation 9 or Table 3 to estimate the capacitance.

$$C_{CT} = \frac{T_{FAULT}}{38.9 \times 10^{3}} = 20 \times \frac{10^{-3}}{38.9 \times 10^{3}} = 0.514 \times 10^{-6} \tag{9}$$

To alter parameters I_{IAX}, I_{FAULT}, I_{IMON} or C_{CT} use the formulas in the *Pin Description* section or use Table 3 .

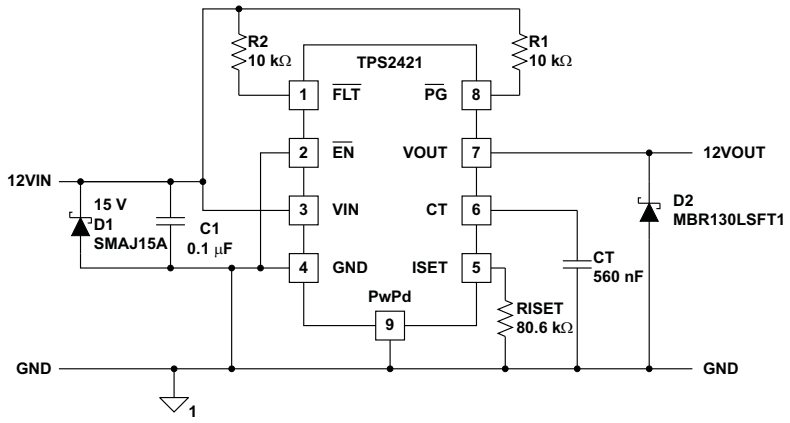


Figure 21. 12-V, 2.5-A Steady State Current, 3.125-A Max Currrent

NOTE

D1, D2, and C1 are required only in systems with significant feed and/or load inductance.

Table 3. Typical Design Examples

I_{SET} (A)	R_{ISET} (kΩ)	C_{CT} (µF)	T_{FAULT} (ms)	T_{SD} (ms)	$I_{LOAD(max)}$ (A)
1	200	0.022	0.86	22	1
1.5	133	0.047	1.83	47	1.5
2	100	0.1	3.89	100	2
2.5	80.6	0.22	8.56	220	2.5
3	65.5	0.47	18.28	470	3
3.5	56.2	0.68	26.45	680	3.5
4	49.9	1	38.9	1000	4

REVISION HISTORY

Changes from Revision A (March 2009) to Revision B	Page
• Changed MARKING	2
• Added For the most current package and ordering information, see the Package Option Addendum at the end of this document, or visit the device product folder on www.ti.com.	2

Changes from Revision B (June 2010) to Revision C	Page
• Changed T_{SD} (ms) column	16

Changes from Revision C (July 2010) to Revision D	Page
• Added UL Listed - File Number E169910	1

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/ Ball Finish	MSL Peak Temp (3)	Samples (Requires Login)
TPS2421-1DDA	ACTIVE	SO PowerPAD	DDA	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	Purchase Samples
TPS2421-1DDAR	ACTIVE	SO PowerPAD	DDA	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	Request Free Samples
TPS2421-2DDA	ACTIVE	SO PowerPAD	DDA	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	Purchase Samples
TPS2421-2DDAR	ACTIVE	SO PowerPAD	DDA	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	Request Free Samples

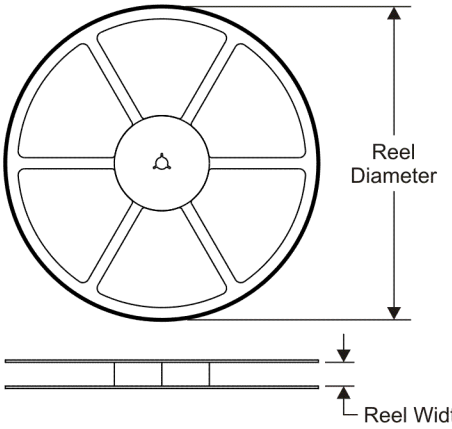
(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

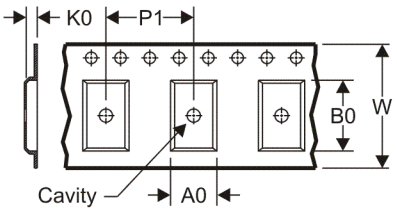
(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

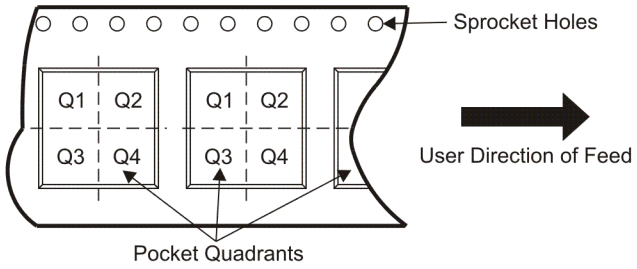


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

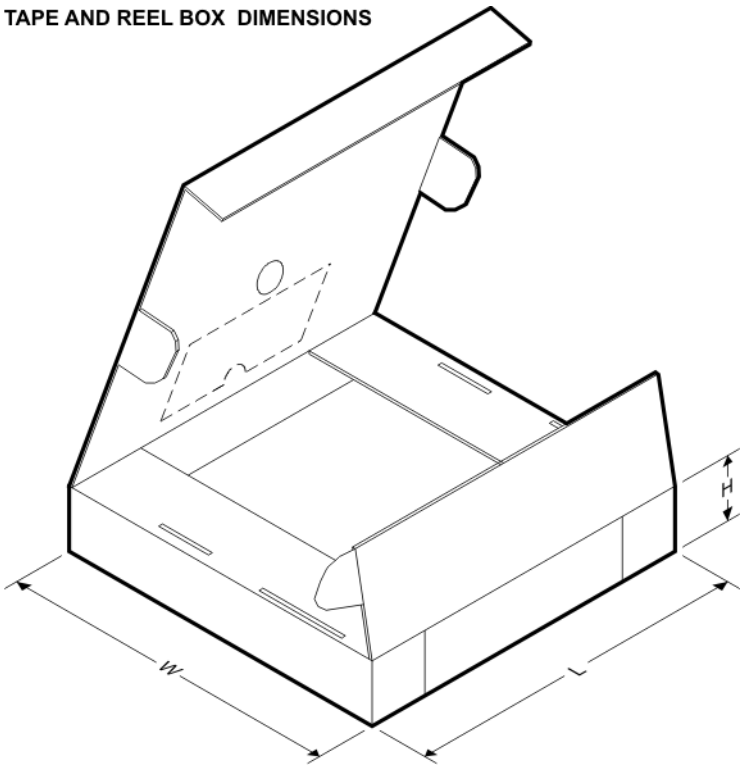
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPS2421-1DDAR	SO Power PAD	DDA	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
TPS2421-2DDAR	SO Power PAD	DDA	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1

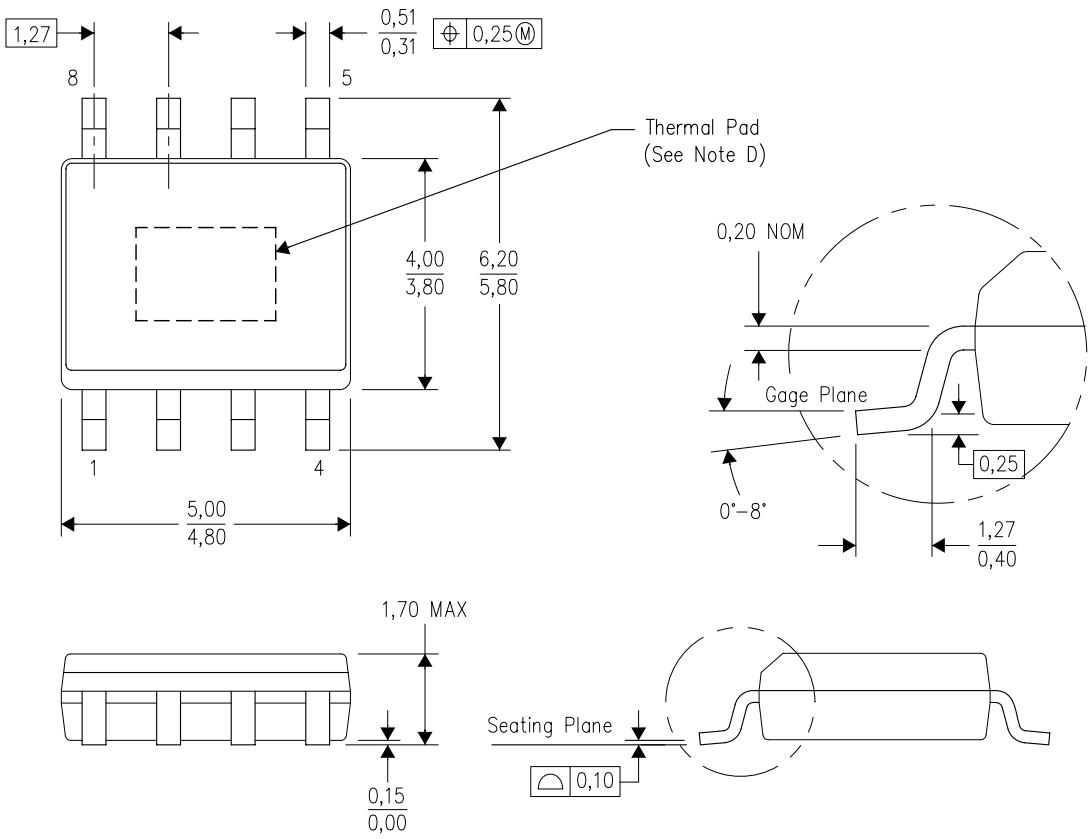
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPS2421-1DDAR	SO PowerPAD	DDA	8	2500	358.0	335.0	35.0
TPS2421-2DDAR	SO PowerPAD	DDA	8	2500	358.0	335.0	35.0

DDA (R–PDSO–G8) PowerPAD™ PLASTIC SMALL–OUTLINE



4202561/E 09/10

NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5–1994.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion not to exceed 0,15.
D. This package is designed to be soldered to a thermal pad on the board. Refer to Technical Brief, PowerPad Thermally Enhanced Package, Texas Instruments Literature No. SLMA002 for information regarding recommended board layout. This document is available at www.ti.com <http://www.ti.com>.
E. This package complies to JEDEC MS–012 variation BA

PowerPAD is a trademark of Texas Instruments.

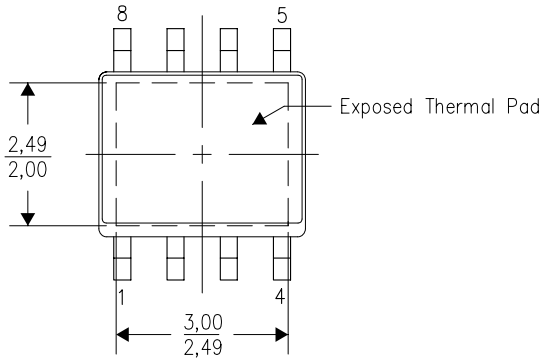
DDA (R–PDSO–G8) PowerPAD™ PLASTIC SMALL OUTLINE

THERMAL INFORMATION

This PowerPAD™ package incorporates an exposed thermal pad that is designed to be attached to a printed circuit board (PCB). The thermal pad must be soldered directly to the PCB. After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For additional information on the PowerPAD package and how to take advantage of its heat dissipating abilities, refer to Technical Brief, PowerPAD Thermally Enhanced Package, Texas Instruments Literature No. SLMA002 and Application Brief, PowerPAD Made Easy, Texas Instruments Literature No. SLMA004. Both documents are available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.



Top View

Exposed Thermal Pad Dimensions

4206322–3/J 01/11

NOTE: A. All linear dimensions are in millimeters

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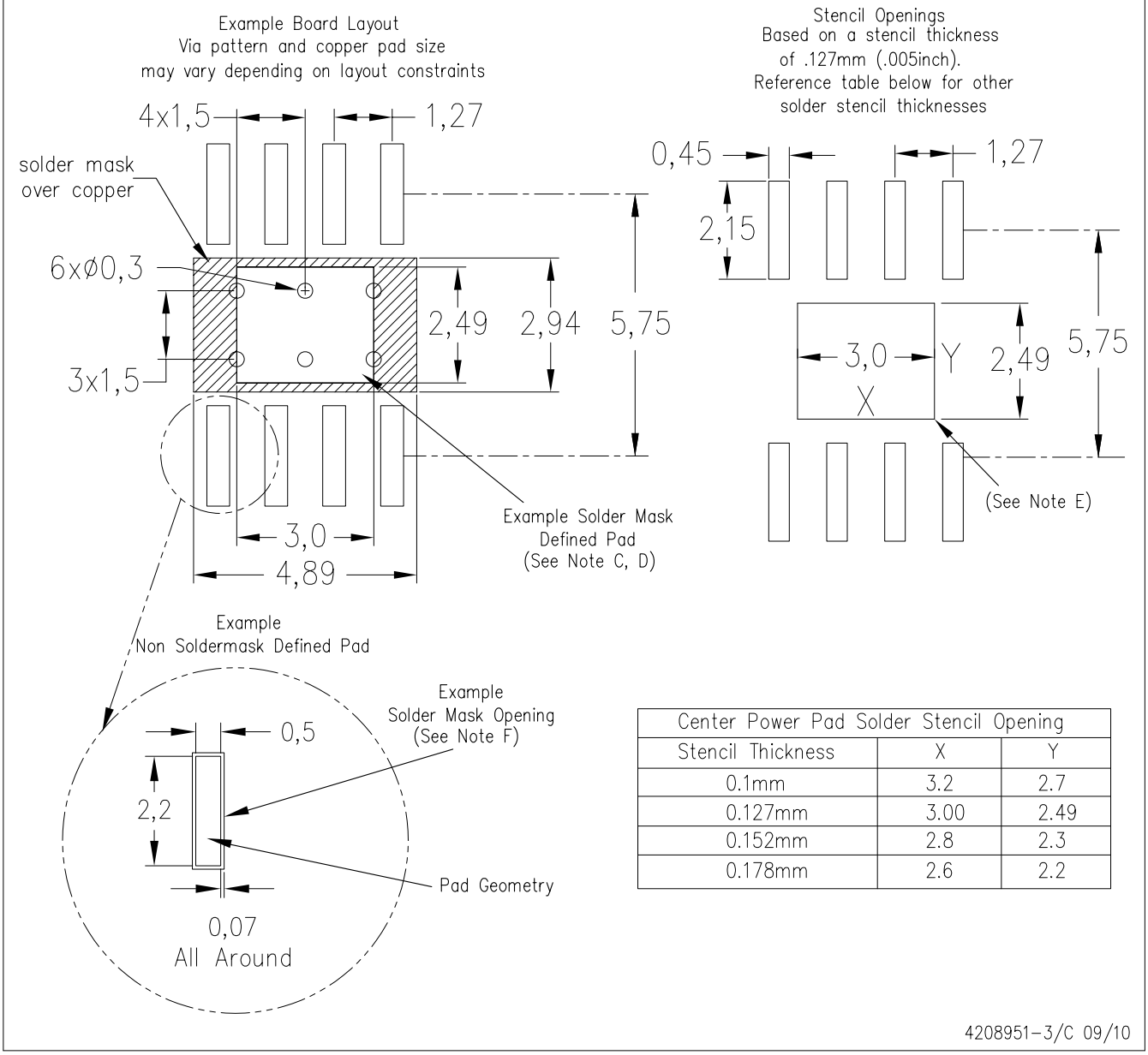
DDA (R–PDSO–G8) PowerPAD™ PLASTIC SMALL OUTLINE



Center Power Pad Solder Stencil Opening		
Stencil Thickness	X	Y
0.1mm	3.2	2.7
0.127mm	3.00	2.49
0.152mm	2.8	2.3
0.178mm	2.6	2.2

NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Customers should place a note on the circuit board fabrication drawing not to alter the center solder mask defined pad.
D. This package is designed to be soldered to a thermal pad on the board. Refer to Technical Brief, PowerPad Thermally Enhanced Package, Texas Instruments Literature No. SLMA002, SLMA004, and also the Product Data Sheets for specific thermal information, via requirements, and recommended board layout. These documents are available at www.ti.com <http://www.ti.com>. Publication IPC–7351 is recommended for alternate designs.
E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Example stencil design based on a 50% volumetric metal load solder paste. Refer to IPC–7525 for other stencil recommendations.
F. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

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