2. S1D15200 Series

Contents

1. DESCRIPTION

The S1D15200 series of dot matrix LCD drivers are designed for the display of characters and graphics. The drivers generate LCD drive signals derived from bit mapped data stored in an internal RAM.
The drivers are available in two configurations
The S1D15200 series drivers incorporate innovative circuit design strategies to achieve very low power dissipation at a wide range of operating voltages.
These features give the designer a flexible means of implementing small to medium size LCD displays for compact, low power systems.

- The S1D15200 which is able to drive two lines of twelve characters each.
- The S1D15201 which is able to drive 80 segments for extention.
- The S1D15202 which is able to drive one line of thirteen characters each.

2. FEATURES

- Fast 8-bit MPU interface compatible with 80- and 68-family microcomputers
- Many command set
- Total 80 (segment + common) drive sets
- Low power — 30 μW at 2 kHz external clock
- Wide range of supply voltages
  V_{DD} – V_{SS}: –2.4 to –7.0 V
  V_{DD} – V5: –3.5 to –13.0 V
- Low-power CMOS

Line-up

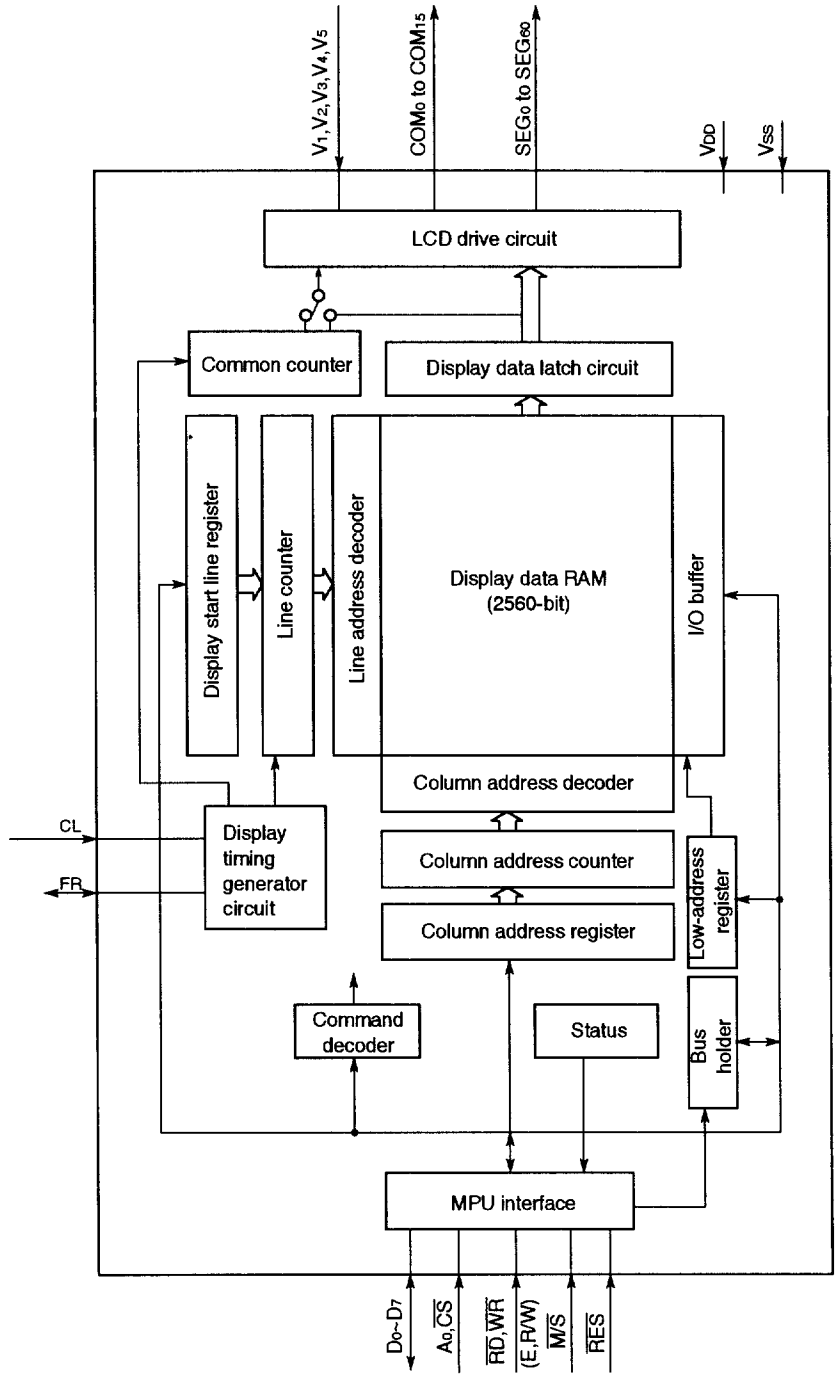
Product Name	Clock Frequency		Applicable Driver	Number of SEG Drivers	Number of CMOS Drivers	Duty
	On-Chip	External				
S1D15200*00**	18 kHz	18 kHz	S1D15200*00**, S1D15201*00**	61	16	1/16, 1/32
S1D15201*00**	—	18 kHz	S1D15200*00**, S1D15202*00**	80	0	1/8 to 1/32
S1D15202*00**	18 kHz	18 kHz	S1D15202*00**, S1D15201*00**	69	8	1/8, 1/16
S1D15200*10**	—	2 kHz	S1D15200*10**, S1D15201*10**	61	16	1/16, 1/32
S1D15201*10**	—	2 kHz	S1D15200*10**, S1D15200*10**	80	0	1/8 to 1/32
S1D15202*10**	—	2 kHz	S1D15200*10**, S1D15201*10**	69	8	1/8, 1/16

- Package code (For example S1D15200)
  S1D15200T : TCP
  S1D15200F**** : PKG
    - S1D15200F**A* (QFP5-100pin)
    - S1D15200F**C* (QFP15-100pin)

  S1D15200D**** : Chip
    - S1D15200D**A* (Al-pad)
    - S1D15200D**B* (Au-bump)
    - S1D15200D**E* (Au-bump)

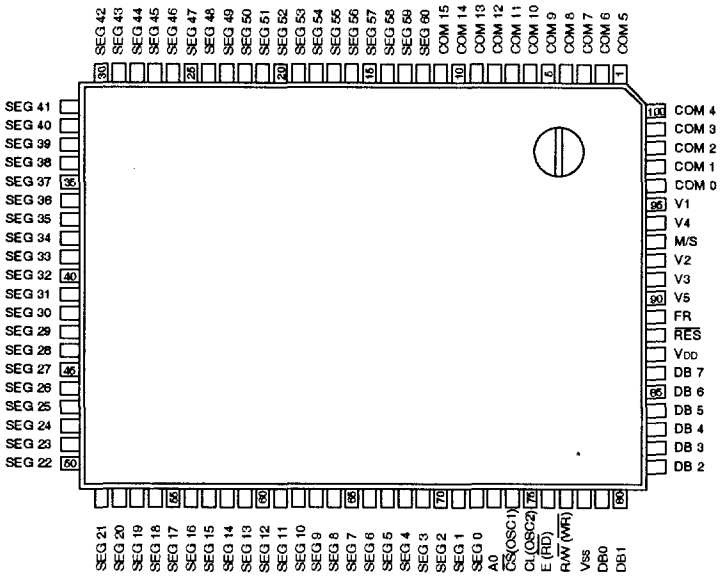
3. BLOCK DIAGRAM

An example of S1D15200*10A*:

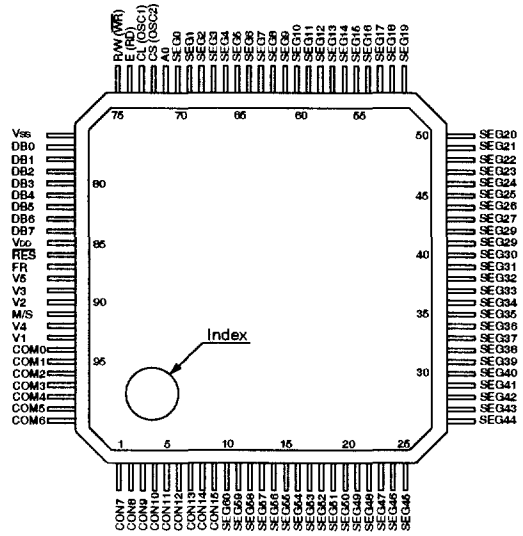


4. PIN LAYOUT

QFP5



QFP15



Note: This is an example of S1D15200F pin assignment. The modified pin names are given below.

Product Name	Pin/Pad Number					
	74	75	96 to 100, 1 to 11	93	94	95
S1D15200F00A*	OSC1	OSC2	COM0 to COM15*	M/S	V4	V1
S1D15201F00A*	CS	CL	SEG76 to SEG61	SEG79	SEG78	SEG77
S1D15202F00A*	OSC1	OSC2	COM0 to 7, SEG68 to 61	M/S	V4	V1
S1D15200F10A*	CS	CL	COM0 to COM15*	M/S	V4	V1
S1D15201F10A*	CS	CL	SEG76 to SEG61	SEG79	SEG78	SEG77
S1D15202F10A*	CS	CL	COM0 to 7, SEG68 to 61	M/S	V4	V1

S1D15200: Common outputs COM0 to COM15 of the master LSI correspond to COM31 to COM16 of the slave LSI.

S1D15202: Common outputs COM0 to COM15 of the master LSI correspond to COM15 to COM8 of the slave LSI.

5. PAD

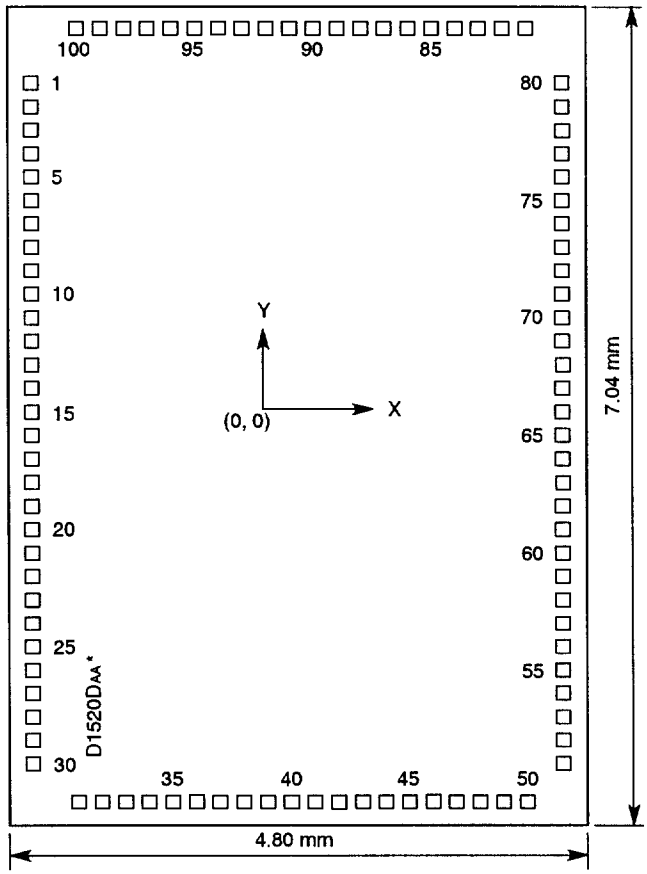
Pad Layout

Chip specifications of AL pad package

Chip size: 4.80×7.04×0.400 mm
Pad pitch: 100×100 μm

Chip specifications of gold bump package

Chip size: 4.80×7.04×0.525 mm
Bump pitch: 199 μm (Min.)
Bump height: 22.5 μm (Typ.)
Bump size: 132×111 μm (±20 μm) for mushroom model
116×92 μm (±4 μm) for vertical model



Note: An example of S1D15200D10A* die numbers is given. These numbers are the same as the bump package.

Pad Center Coordinates

An example of S1D15200D10** pin names is given. The asterisk (*) can be A for AL pad package or B for gold bump package.

S1D15200D10B* Pad Center Coordinates

Pad No.	Pin Name	X	Y
1	COM5	159	6507
2	COM6	159	6308
3	COM7	159	6108
4	COM8	159	5909
5	COM9	159	5709
6	COM10	159	5510
7	COM11	159	5310
8	COM12	159	5111
9	COM13	159	4911
10	COM14	159	4712
11	COM15	159	4512
12	SEG60	159	4169
13	SEG59	159	3969
14	SEG58	159	3770
15	SEG57	159	3570
16	SEG56	159	3371
17	SEG55	159	3075
18	SEG54	159	2876
19	SEG53	159	2676
20	SEG52	159	2477
21	SEG51	159	2277
22	SEG50	159	2078
23	SEG49	159	1878
24	SEG48	159	1679
25	SEG47	159	1479
26	SEG46	159	1280
27	SEG45	159	1080
28	SEG44	159	881
29	SEG43	159	681
30	SEG42	159	482
31	SEG41	504	159
32	SEG40	704	159
33	SEG39	903	159
34	SEG38	1103	159
35	SEG37	1302	159
36	SEG36	1502	159
37	SEG35	1701	159
38	SEG34	1901	159
39	SEG33	2100	159
40	SEG32	2300	159
41	SEG31	2499	159
42	SEG30	2699	159
43	SEG29	2898	159
44	SEG28	3098	159
45	SEG27	3297	159
46	SEG26	3497	159
47	SEG25	3696	159
48	SEG24	3896	159
49	SEG23	4095	159
50	SEG22	4295	159
51	SEG21	4641	482
52	SEG20	4641	681
53	SEG19	4641	881
54	SEG18	4641	1080
55	SEG17	4641	1280
56	SEG16	4641	1479
57	SEG15	4641	1679
58	SEG14	4641	1878
59	SEG13	4641	2078
60	SEG12	4641	2277
61	SEG11	4641	2477
62	SEG10	4641	2676
63	SEG9	4641	2876
64	SEG8	4641	3075
65	SEG7	4641	3275
66	SEG6	4641	3474
67	SEG5	4641	3674
68	SEG4	4641	3948
69	SEG3	4641	4148
70	SEG2	4641	4347
71	SEG1	4641	4547
72	SEG0	4641	4789
73	A0	4641	5048
74	CS	4641	5247
75	CL	4641	5447
76	E ($\overline{RD}$)	4641	5646
77	R/W ($\overline{WR}$)	4641	5846
78	V_{SS}	4641	6107
79	DB0	4641	6307
80	DB1	4641	6506
81	DB2	4295	6884
82	DB3	4095	6884
83	DB4	3896	6884
84	DB5	3696	6884
85	DB6	3497	6884
86	DB7	3297	6884
87	V_{DD}	3098	6884
88	$\overline{RES}$	2898	6884
89	FR	2699	6884
90	V_5	2499	6884
91	V_3	2300	6884
92	V_2	2100	6884
93	M/S	1901	6884
94	V_4	1701	6884
95	V_1	1502	6884
96	COM0	1302	6884
97	COM1	1103	6884
98	COM2	903	6884
99	COM3	704	6884
100	COM4	504	6884

The other S1D15200 series packages have the different pin names as shown.

Package/Pad No.	74	75	96 to 100, 1 to 11	93	94	95
S1D15200D00**	OSC1	OSC2	COM0 to COM15 *	M/S	V_4	V_1
S1D15202D00**	OSC1	OSC2	COM0 to 7, SEG68 to 61	M/S	V_4	V_1
S1D15202D10**	OSC1	OSC2	COM0 to 7, SEG68 to 61	M/S	V_4	V_1
S1D15201D00**	CS	CL	SEG76 to SEG61	SEG79	SEG78	SEG77
S1D15201D10**	CS	CL	SEG76 to SEG61	SEG79	SEG78	SEG77

6. PIN DESCRIPTION

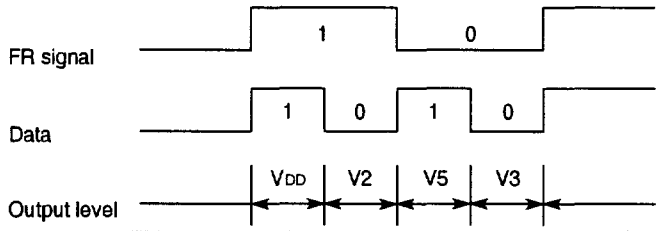
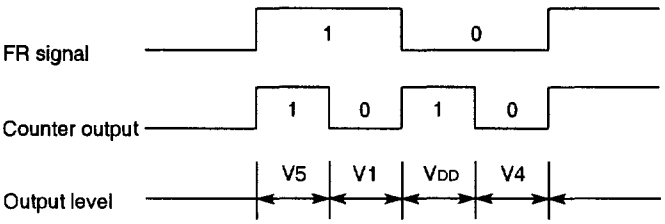
(1) Power Supply Pins

Name	Description
V_{DD}	Connected to the +5Vdc power. Common to the V_{CC} MPU power pin.
V_{SS}	0 Vdc pin connected to the system ground.
V_1, V_2, V_3, V_4, V_5	Multi-level power supplies for LCD driving. The voltage determined for each liquid crystal cell is divided by resistance or it is converted in impedance by the op amp, and supplied. These voltages must satisfy the following: $V_{DD} \geq V_1 \geq V_2 \geq V_3 \geq V_4 \geq V_5$

(2) System Bus Connection Pins

D7 to D0	Three-state I/O. The 8-bit bidirectional data buses to be connected to the 8- or 16-bit standard MPU data buses.
A0	Input. Usually connected to the low-order bit of the MPU address bus and used to identify the data or a command. A0=0: D0 to D7 are display control data. A0=1: D0 to D7 are display data.
$\overline{RES}$	Input. When the $\overline{RES}$ signal goes ¬└┌ the 68-series MPU is initialized, and when it goes _┌└_ , the 80-series MPU is initialized. The system is reset during edge sense of the $\overline{RES}$ signal. The interface type to the 68-series or 80-series MPU is selected by the level input as follows: High level: 68-series MPU interface Low level: 80-series MPU interface
$\overline{CS}$	Input. Active low. Effective for an external clock operation model only. An address bus signal is usually decoded by use of chip select signal, and it is entered. If the system has a built-in oscillator, this is used as an input pin to the oscillator amp and an Rf oscillator resistor is connected to it. In such case, the $\overline{RD}$, $\overline{WR}$ and E signals must be ORed with the $\overline{CS}$ signals and entered.
E ($\overline{RD}$)	• If the 68-series MPU is connected: Input. Active HIGH. Used as an enable clock input of the 68-series MPU. • If the 80-series MPU is connected: Input. Active LOW. The $\overline{RD}$ signal of the 80-series MPU is entered in this pin. When this signal is kept low, the SED1520 data bus is in the output status.
R/W ($\overline{WR}$)	• If the 68-series MPU is connected: Input. Used as an input pin of read control signals (if R/W is HIGH) or write control signals (if LOW). • If the 80-series MPU is connected: Input. Active LOW. The $\overline{WR}$ signal of the 80-series MPU is entered in this pin. A signal on the data bus is fetched at the rising edge of $\overline{WR}$ signal.

(3) LCD Drive Circuit Signals

Name	Description
CL	Input. Effective for an external clock operation model only. This is a display data latch signal to count up the line counter and common counter at each signal falling and rising edges. If the system has a built-in oscillator, this is used as an output pin of the oscillator amp and an Rf oscillator resistor is connected to it.
FR	Input/output. This is an I/P pin of LCD AC signals, and connected to the M terminal of common driver. I/O selection • Common oscillator built-in model: Output if M/S is 1; Input if M/S is 0. • Dedicate segment model: Input
SEGn	Output. The output pin for LCD column (segment) driving. A single level of V_{DD}, V_2, V_3 and V_5 is selected by the combination of display RAM contents and RF signal. 
COMn	Output. The output pin for LCD common (low) driving. A single level of V_{DD}, V_1, V_4 and V_5 is selected by the combination of common counter output and RF signal. The slave LSI has the reverse common output scan sequence than the master LSI. 
M/S	Input. The master or slave LSI operation select pin for the S1D15200 or S1D15202. Connected to V_{DD} (to select the master LSI operation mode) or V_{SS} (to select the slave LSI operation mode). When this M/S pin is set, the functions of FR, COM0 to COM15, OSC1 ($\overline{CS}$), and OSC2 (CL) pins are changed.

	M/S	FR	COM output	OSC1	OSC2
S1D15200F00A*	V_{DD}	Output	COM0 to COM15	Input	Output
	V_{SS}	Input	COM31 to COM16	NC	Input
S1D15202F00A*	V_{DD}	Output	COM0 to COM7	Input	Output
	V_{SS}	Input	COM15 to COM8	NC	Input

* The slave driver has the reverse common output scan sequence than the master driver.

7. FUNCTION DESCRIPTION

System Bus

MPU interface

1. Selecting an interface type

The S1D15200 series transfers data via 8-bit bidirectional data buses (D0 to D7). As its Reset pin has the MPU interface select function, the 80-series MPU or the 68-series MPU can directly be connected to the MPU bus by the selection of HIGH or LOW $\overline{RES}$ signal level after reset (see Table 1).
When the $\overline{CS}$ signal is high, the S1D15200 series is disconnected from the MPU bus and set to stand by. However, the reset signal is entered regardless of the internal setup status.

Table 1

$\overline{RES}$ signal input level	MPU type	A0	E	R/W	CS	D0 to D7
⊓ Active	68-series	↑	↑	↑	↑	↑
⊓ Active	80-series	↑	$\overline{RD}$	$\overline{WR}$	↑	↑

(1) Data transfer

The S1D15200 and S1D15201 drivers use the A0, E (or $\overline{RD}$) and R/$\overline{W}$ (or $\overline{WR}$) signals to transfer data between the system MPU and internal registers. The combinations used Access to Display Date RAM and Internal Registers are given in the table blow.

This means that a dummy read cycle has to be executed at the start of every series of reads. See Figure 1.
No dummy cycle is required at the start of a series of writes as data is transferred automatically from the input latch to its destination.

Table 2

Common	68 MPU	80 MPU		Function
A0	R/$\overline{W}$	$\overline{RD}$	$\overline{WR}$	
1	1	0	1	Read display data
1	0	1	0	Write display data
0	1	0	1	Read status
0	0	1	0	Write to internal register (command)

In order to match the timing requirements of the MPU with those of the display data RAM and control registers all data is latched into and out of the driver. This introduces a one cycle delay between a read request for data and the data arriving. For example when the MPU executes a read cycle to access display RAM the current contents of the latch are placed on the system data bus while the desired contents of the display RAM are moved into the latch.

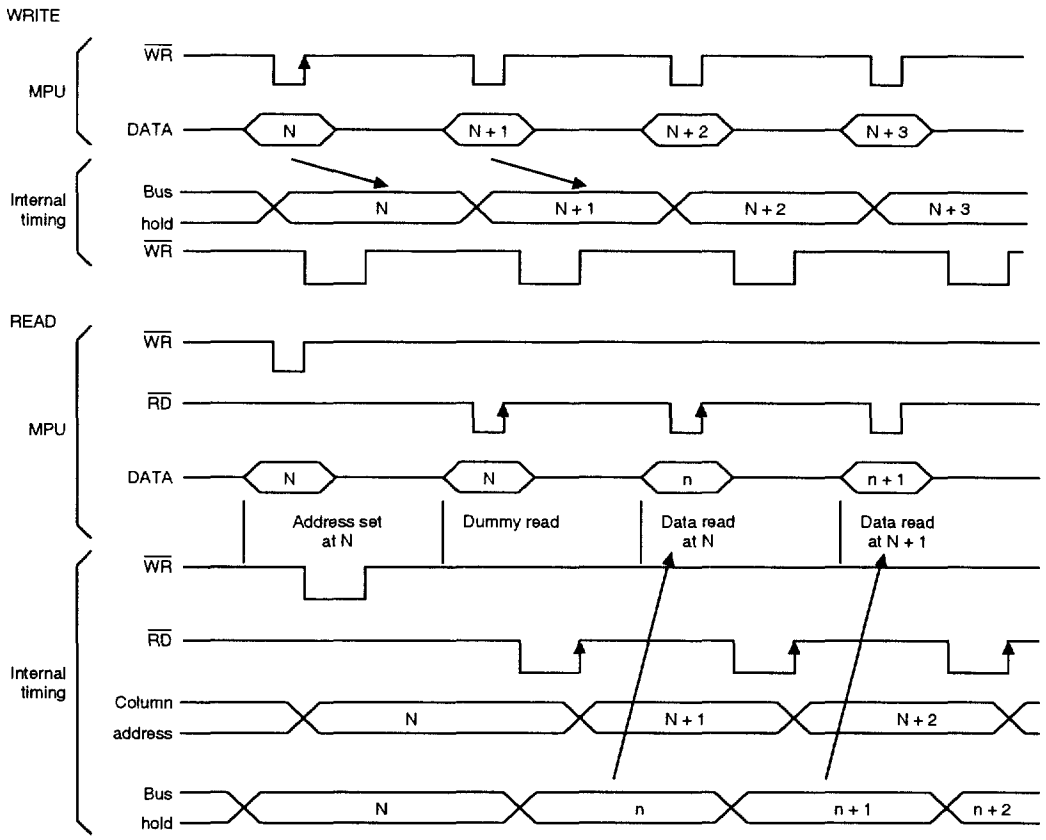


Figure 1 Bus Buffer Delay

(2) Busy flag

When the Busy flag is logical 1, the S1D15200 series is executing its internal operations. Any command other than Status Read is rejected during this time. The Busy flag is output at pin D7 by the Status Read command. If an appropriate cycle time (tcyc) is given, this flag needs not be checked at the beginning of each command and, therefore, the MPU processing capacity can greatly be enhanced.

(3) Display Start Line and Line Count Registers

The contents of this register form a pointer to a line of data in display data RAM corresponding to the first line of the display (COM0), and are set by the Display Start Line command. See section 3.

The contents of the display start line register are copied into the line count register at the start of every frame, that is on each edge of FR. The line count register is incremented by the CL clock once for every display line, thus generating a pointer to the current line of data, in display data RAM, being transferred to the segment driver circuits.

(4) Column Address Counter

The column address counter is a 7-bit presettable counter that supplies the column address for MPU access to the display data RAM. See Figure 2. The counter is incremented by one every time the driver receives a Read or Write Display Data command. Addresses above 50H are invalid, and the counter will not increment past this value. The contents of the column address counter are set with the Set Column Address command.

(5) Page Register

The page resiter is a 2-bit register that supplies the page address for MPU access to the display data RAM. See Figure 2. The contents of the page register are set by the Set Page Register command.

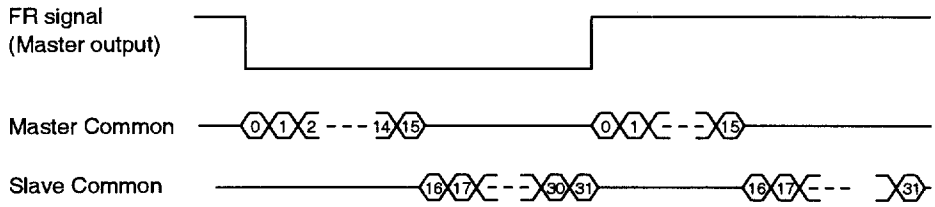
(6) Display Data RAM

The display data RAM stores the LCD display data, on a 1-bit per pixel basis. The relation-ship between display data, display address and the display is shown in Figure 2.

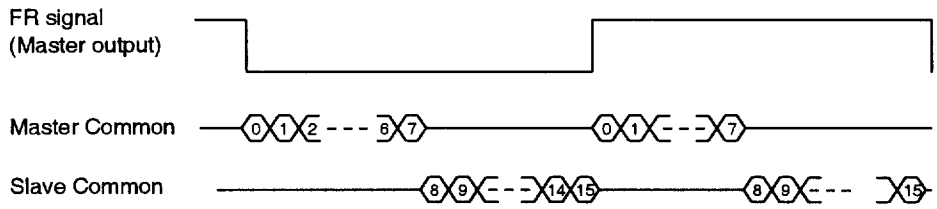
(7) Common Timing Generator Circuit

Generates common timing signals and FR frame signals from the CL basic clock. The 1/16 or 1/32 duty (for S1D15200) or 1/8 or 1/16 duty (for S1D15202) can be selected by the Duty Select command. If the 1/32 duty is selected for the S1D15200 and 1/16 duty is selected for the S1D15202, the 1/32 and 1/16 duties are provided by two chips consisting of the master and slave chips in the common multi-chip mode.

S1D15200



S1D15220



(8) Display Data Latch Circuit

This latch stores one line of display data for use by the LCD driver interface circuitry. The output of this latch is controlled by the Display ON/OFF and Static Drive ON/OFF commands.

(9) LCD Driver Circuit

The LCD driver circuitry generates the 80 4-level signals used to drive the LCD panel, using output from the display data latch and the common timing generator circuitry.

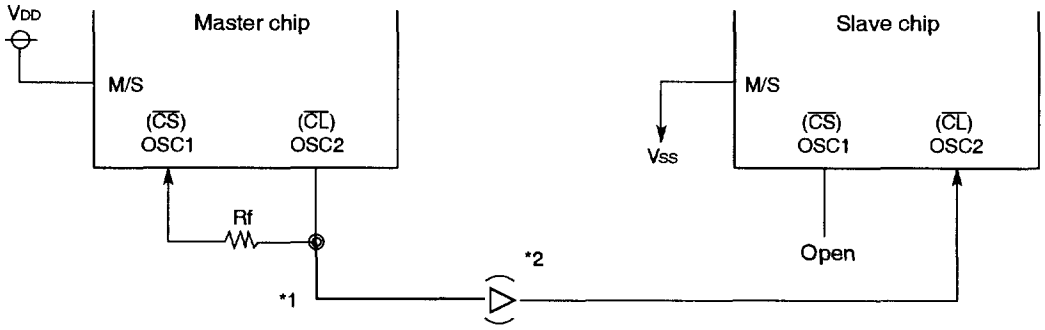
(10) Display Timing Generator

This circuit generates the internal display timing signal using the basic clock, CL, and the frame signals, FR. FR is used to generate the dual frame AC-drive waveform (type B drive) and to lock the line counter and common timing generator to the system frame rate. CL is used to lock the line counter to the system line scan rate. If a system uses both S1D15200 or S1D15202 and S1D15201 they must have the same CL frequency rating.

(11) Oscillator Circuit (S1D15200*0A Only)

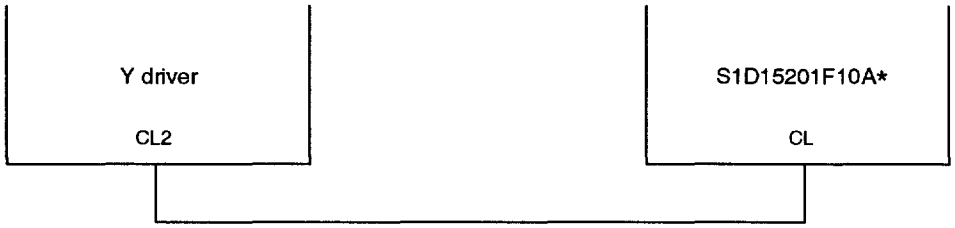
A low power-consumption CR oscillator for adjusting the oscillation frequency using Rf oscillation resistor only. This circuit generates a display timing signal. Some of S1D15200 and S1D15202 series models have a built-in oscillator and others use an external clock. This difference must be checked before use.
Connect the Rf oscillation resistor as follows. To suppress the built-in oscillator circuit and drive the MPU using an external clock, enter the clock having the same phase as the OSC2 of mater chip into OSC2 of the slave chip.

- MPU having a built-in oscillator



*1 If the parasitic capacitance of this section increases, the oscillation frequency may shift to the lower frequency. Therefore, the Rf oscillation frequency must be reduced below the specified level.
*2 A CMOS buffer is required if the oscillation circuit is connected to two or more slave MPU chips.

- MPU driven with an external clock



(12) Reset Circuit

Detects a rising or falling edge of an $\overline{RES}$ input and initializes the MPU during power-on.

- Initialization status
  1. Display is off.
  2. Display start line register is set to line 1.
  3. Static drive is turned off.
  4. Column address counter is set to address 0.
  5. Page address register is set to page 3.
  6. 1/32 duty (S1D15200) or 1/16 duty (S1D15202) is selected.
  7. Forward ADC is selected (ADC command D0 is 1 and ADC status flag is 1).
  8. Read-modify-write is turned off.

The input signal level at $\overline{RES}$ pin is sensed, and an MPU interface mode is selected as shown on Table 1. For the 80-series MPU, the $\overline{RES}$ input is passed through the inverter and the active high reset signal must be entered. For the 68-series MPU, the active low reset signal must be entered.
As shown for the MPU interface (reference example), the $\overline{RES}$ pin must be connected to the Reset pin and reset at the same time as the MPU initialization.
If the MPU is not initialized by the use of $\overline{RES}$ pin during power-on, an unrecoverable MPU failure may occur.
When the Reset command is issued, initialization

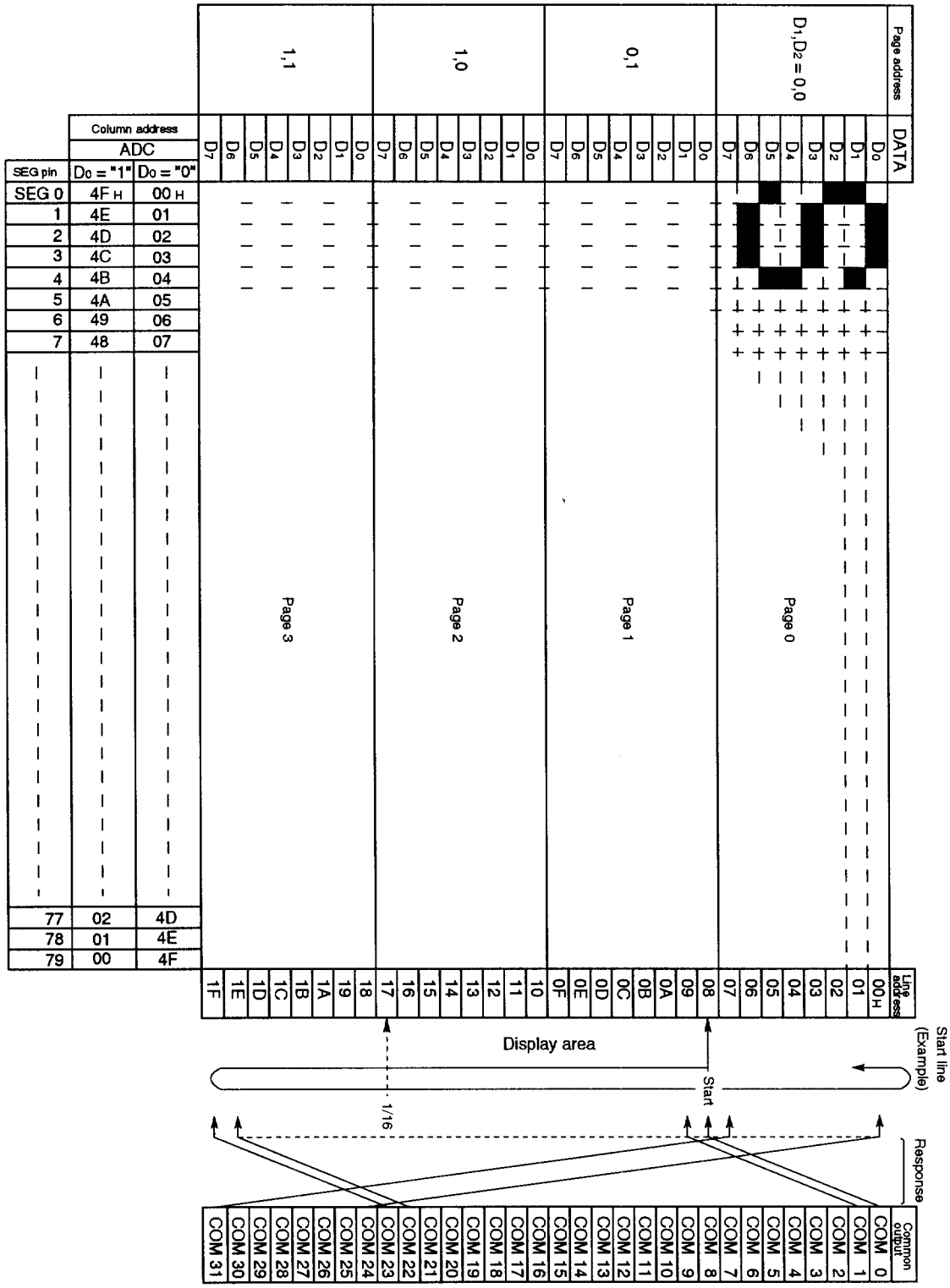


Figure 2 Display Data RAM Addressing

1/5 bias, 1/16 duty
1/6 bias, 1/32 duty

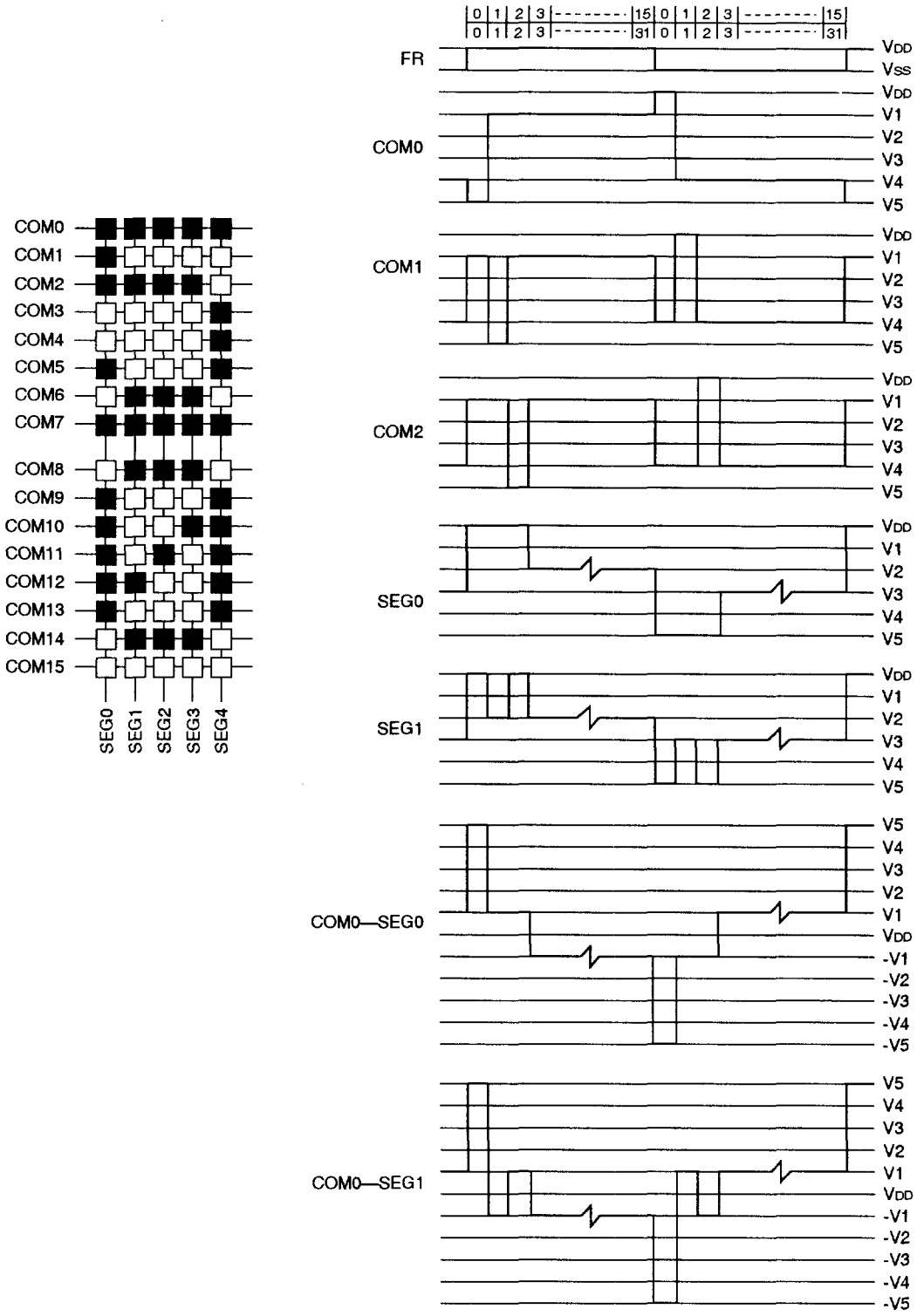


Figure 4 LCD drive waveforms example

8. COMMANDS

Table 3

Command	Code											Function
	A0	$\overline{RD}$	$\overline{WR}$	D7	D6	D5	D4	D3	D2	D1	D0	
(1) Display On/OFF	0	1	0	1	0	1	0	1	1	1	0/1	Turns display on or off. 1: ON, 0: OFF
(2) Display start line	0	1	0	1	1	0Display start address (0 to 31)						Specifies RAM line corresponding to top line of display.
(3) Set page address	0	1	0	1	0	1	1	1	0	Page (0 to 3)		Sets display RAM page in page address register.
(4) Set column (segment) address	0	1	0	0	Column address (0 to 79)							Sets display RAM column address in column address register.
(5) Read status	0	0	1	Busy	ADC	ON/OFF	Reset	0	0	0	0	Reads the following status: BUSY 1: Busy 0: Ready ADC 1: CW output 0: CCW output ON/OFF 1: Display off 0: Display on RESET 1: Being reset 0: Normal
(6) Write display data	1	1	0	Write data								Writes data from data bus into display RAM.
(7) Read display data	1	0	1	Read data								Reads data from display RAM onto data bus.
(8) Select ADC	0	1	0	1	0	1	0	0	0	0	0/1	0: CW output, 1: CCW output
(9) Static drive ON/OFF	0	1	0	1	0	1	0	0	1	0	0/1	Selects static driving operation. 1: Static drive, 0: Normal driving
(10) Select duty	0	1	0	1	0	1	0	1	0	0	0/1	Selets LCD duty cycle 1: 1/32, 0: 1/16
(11) Read-Modify-Write	0	1	0	1	1	1	0	0	0	0	0	Read-modify-write ON
(12) End	0	1	0	1	1	1	0	1	1	1	0	Read-modify-write OFF
(13) Reset	0	1	0	1	1	1	0	0	0	1	0	Software reset

Command Description

Table 3 is the command table. The S1D15200 series identifies a data bus using a combination of A0 and R/W ($\overline{RD}$ or $\overline{WR}$) signals. As the MPU translates a command in the internal timing only (independent from the external clock), its speed is very high. The busy check is usually not required.

(1) Display ON/OFF

A0	$\overline{RD}$	R/$\overline{W}$ $\overline{WR}$	D7	D6	D5	D4	D3	D2	D1	D0	
0	1	0	1	0	1	0	1	1	1	D	AEH, AFH

This command turns the display on and off.

- D=1: Display ON
- D=0: Display OFF

(2) Display Start Line

This command specifies the line address shown in Figure 3 and indicates the display line that corresponds to COM0. The display area begins at the specified line address and continues in the line address increment direction. This area having the number of lines of the specified display duty is displayed. If the line address is changed dynamically by this command, the vertical smooth scrolling and paging can be used.

A0	$\overline{RD}$	R/$\overline{W}$ $\overline{WR}$	D7	D6	D5	D4	D3	D2	D1	D0	
0	1	0	1	1	0	A4	A3	A2	A1	A0	C0H to DFH

This command loads the display start line register.

A4	A3	A2	A1	A0	Line Address
0	0	0	0	0	0
0	0	0	0	1	1
		:			:
		:			:
1	1	1	1	1	31

See Figure 2.

(3) Set Page Address

This command specifies the page address that corresponds to the low address of the display data RAM when it is accessed by the MPU. Any bit of the display data RAM can be accessed when its page address and column address are specified. The display status is not changed even when the page address is changed.

A0	$\overline{RD}$	R/$\overline{W}$ $\overline{WR}$	D7	D6	D5	D4	D3	D2	D1	D0	
0	1	0	1	0	1	1	1	0	A1	A0	B8H to BBH

This command loads the page address register.

A1	A0	Page
0	0	0
0	1	1
1	0	2
1	1	3

See Figure 2.

(4) Set Column Address

This command specifies a column address of the display data RAM. When the display data RAM is accessed by the MPU continuously, the column address is incremented by 1 each time it is accessed from the set address. Therefore, the MPU can access to data continuously. The column address stops to be incremented at address 80, and the page address is not changed continuously.

A0	$\overline{RD}$	R/$\overline{W}$ $\overline{WR}$	D7	D6	D5	D4	D3	D2	D1	D0	
0	1	0	0	A6	A5	A4	A3	A2	A1	A0	00H to 4FH

This command loads the column address register.

A6	A5	A4	A3	A2	A1	A0	Column Address
0	0	0	0	0	0	0	0
0	0	0	0	0	0	1	1
			⋮				⋮
1	0	0	1	1	1	1	79

(5) Read Status

A0	$\overline{RD}$	R/$\overline{W}$ $\overline{WR}$	D7	D6	D5	D4	D3	D2	D1	D0
0	0	1	BUSY	ADC	ON/OFF	RESET	0	0	0	0

Reading the command I/O register (A0=0) yields system status information.

- The busy bit indicates whether the driver will accept a command or not.
  Busy=1: The driver is currently executing a command or is resetting. No new command will be accepted.
  Busy=0: The driver will accept a new command.
- The ADC bit indicates the way column addresses are assigned to segment drivers.
  ADC=1: Normal. Column address n → segment driver n.
  ADC=0: Inverted. Column address 79-u → segment driver u.
- The ON/OFF bit indicates the current status of the display.
  It is the inverse of the polarity of the display ON/OFF command.
  ON/OFF=1: Display OFF
  ON/OFF=0: Display ON
- The RESET bit indicates whether the driver is executing a hardware or software reset or if it is in normal operating mode.
  RESET=1: Currently executing reset command.
  RESET=0: Normal operation

(6) Write Display Data

A0	$\overline{RD}$	R/$\overline{W}$ $\overline{WR}$	D7	D6	D5	D4	D3	D2	D1	D0
1	1	0	Write data							

Writes 8-bits of data into the display data RAM, at a location specified by the contents of the column address and page address registers and then increments the column address register by one.

(7) Read Display Data

A0	$\overline{RD}$	R/$\overline{W}$ $\overline{WR}$	D7	D6	D5	D4	D3	D2	D1	D0
1	0	1	Read data							

Reads 8-bits of data from the data I/O latch, updates the contents of the I/O latch with display data from the display data RAM location specified by the contents of the column address and page address registers and then increments the column address register.
After loading a new address into the column address register one dummy read is required before valid data is obtained.

(8) Select ADC

A0	$\overline{RD}$	R/$\overline{W}$ $\overline{WR}$	D7	D6	D5	D4	D3	D2	D1	D0	
0	1	0	1	0	1	0	0	0	0	D	A0H, A1H

This command selects the relationship between display data RAM column addresses and segment drivers.
D=1: SEG0 ← column address 4FH, ... (inverted)
D=0: SEG0 ← column address 00H, ... (normal)
This command is provided to reduce restrictions on the placement of driver ICs and routing of traces during printed circuit board design. See Figure 2 for a table of segments and column addresses for the two values of D.

(9) Static Drive ON/OFF

A0	$\overline{RD}$	R/$\overline{W}$ $\overline{WR}$	D7	D6	D5	D4	D3	D2	D1	D0	
0	1	0	1	0	1	0	0	1	0	D	A4H, A5H

Forces display on and all common outputs to be selected.
D=1: Static drive on
D=0: Static drive off

(10) Select Duty

A0	$\overline{RD}$	R/$\overline{W}$ $\overline{WR}$	D7	D6	D5	D4	D3	D2	D1	D0	
0	1	0	1	0	1	0	1	0	0	D	A8H, A9H

This command sets the duty cycle of the LCD drive and is only valid for the S1D15200F and S1D15202F. It is invalid for the S1D15201F which performs passive operation. The duty cycle of the S1D15201F is determined by the externally generated FR signal.

	S1D15200	S1D15202
D=1:	1/32 duty cycle	1/16 duty cycle
D=0:	1/16 duty cycle	1/8 duty cycle

When using the S1D15200F00A*, S1D15202F00A* (having a built-in oscillator) and the S1D15201F00A* continuously, set the duty as follows:

		S1D15201F00A*
S1D15200F00A*	1/32	1/32
	1/16	1/16
S1D15202F00A*	1/16	1/32
	1/8	1/16

(11) Read-Modify-Write

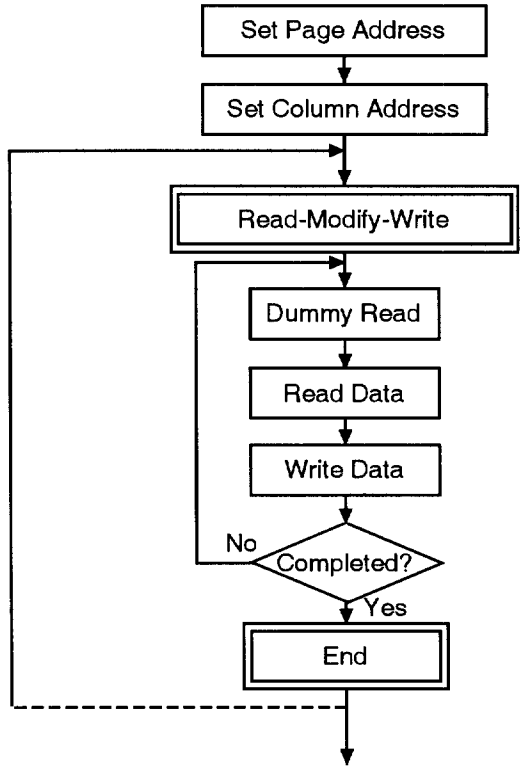
A0	$\overline{RD}$	R/$\overline{W}$ $\overline{WR}$	D7	D6	D5	D4	D3	D2	D1	D0	
0	1	0	1	1	1	0	0	0	0	0	E0H

This command defeats column address register auto-increment after data reads. The current conetents of the column address register are saved. This mode remains active until an End command is received.

- Operation sequence during cursor display

When the End command is entered, the column address is returned to the one used during input of Read-Modify-Write command. This function can reduce the load of MPU when data change is repeated at a specific display area (such as cursor blinking).

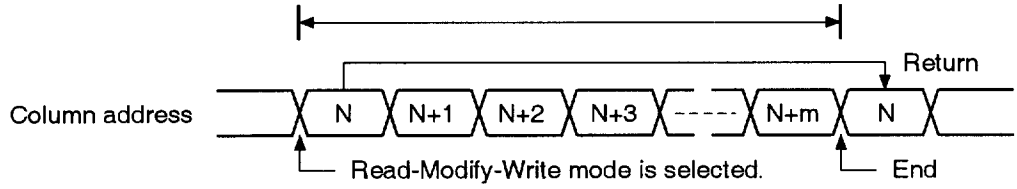
* Any command other than Data Read or Write can be used in the Read-Modify-Write mode. However, the Column Address Set command cannot be used.



(12) End

A0	$\overline{RD}$	R/$\overline{W}$ $\overline{WR}$	D7	D6	D5	D4	D3	D2	D1	D0	
0	1	0	1	1	1	0	1	1	1	0	EEH

This command cancels read-modify-write mode and restores the contents of the column address register to their value prior to the receipt of the Read-Modify-Write command.



(13) Reset

A0	$\overline{RD}$	R/$\overline{W}$ / $\overline{WR}$	D7	D6	D5	D4	D3	D2	D1	D0	
0	1	0	1	1	1	0	0	0	1	0	E2H

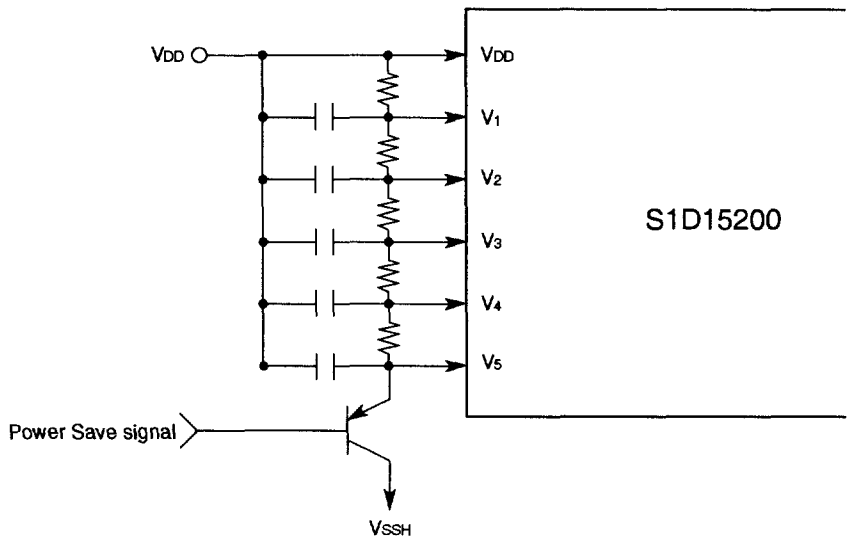
This command clears
- the display start line register.
- and set page address register to 3 page.

  It does not affect the contents of the display data RAM.

When the power supply is turned on, a Reset signal is entered in the $\overline{RES}$ pin. The Reset command cannot be used instead of this Reset signal.

(14) Power Save (Combination command)

The Power Save mode is selected if the static drive is turned ON when the display is OFF. The current consumption can be reduced to almost the static current level. In the Power Save mode:
(a) The LCD drive is stopped, and the segment and common driver outputs are set to the VDD level.
(b) The external oscillation clock input is inhibited, and the OSC2 is set to the floating mode.
(c) The display and operation modes are kept.
The Power Save mode is released when the display is turned ON or when the static drive is turned OFF. If the LCD drive voltage is supplied from an external resistance divider circuit, the current passing through this resistor must be cut by the Power Save signal.



If the LCD drive power is generated by resistance division, the resistance and capacitance are determined by the LCD panel size. After the panel size has been determined, reduce the resistance to the level where the display quality is not affected and reduce the power consumption using the divider resistor.

9. ABSOLUTE MAXIMUS RATINGS

Parameter	Symbol	Rating	Unit
Supply voltage (1)	V_{SS}	–8.0 to +0.3	V
Supply voltage (2)	V_5	–16.5 to +0.3	V
Supply voltage (3)	V_1, V_4, V_2, V_3	V5 to +0.3	V
Input voltage	V_{IN}	V_{SS}–0.3 to +0.3	V
Output voltage	V_O	V_{SS}–0.3 to +0.3	V
Power dissipation	P_D	250	mW
Operating temperature	T_{opr}	–40 to +85	°C
Storage temperature	T_{stg}	–65 to +150	°C
Soldering temperature time at lead	T_{sol}	260, 10	°C, sec

Notes: 1. All voltages are specified relative to V_{DD} = 0 V.
2. The following relation must be always hold
$V_{DD} \geq V_1 \geq V_2 \geq V_3 \geq V_4 \geq V_5$
3. Exceeding the absolute maximum ratings may cause permanent damage to the device. Functional operation under these conditions is not implied.
4. Moisture resistance of flat packages can be reduced by the soldering process, so care should be taken to avoid thermally stressing the package during board assembly.

10. ELECTRICAL CHARCTERISTICS

DC Characteristics

Ta = –20 to 75 °C, V_{DD} = 0 V unless stated otherwise

Parameter		Symbol	Condition		Rating Min.	Rating Typ.	Rating Max.	Unit	Applicable Pin
Operating voltage (1) See note 1.	Recommended	V_{SS}			–5.5	–5.0	–4.5	V	V_{SS}
	Allowable				–7.0	—	–2.4		
Operating voltage (2)	Recommended	V_5			–13.0	—	–3.5	V	V_5 See note 10.
	Allowable				–13.0	—	—		
	Allowable	V_1, V_2			0.6×V_5	—	V_{DD}	V	V_1, V_2
	Allowable	V_3, V_4			V_5	—	0.4×V_5	V	V_3, V_4
High-level input voltage		V_{IHT}			V_{SS}+2.0	—	V_{DD}	V	See note 2 & 3.
		V_{IHC}			0.2×V_{SS}	—	V_{DD}		
		V_{IHT}	V_{SS} = –3 V		0.2×V_{SS}	—	V_{DD}		See note 2 & 3.
		V_{IHC}	V_{SS} = –3 V		0.2×V_{SS}	—	V_{DD}		
Low-level input voltage		V_{ILT}			V_{SS}		V_{SS}+0.8		See note 2 & 3.
		V_{ILC}			V_{SS}		0.8×V_{SS}		
		V_{ILT}	V_{SS} = –3 V		V_{SS}		0.85×V_{SS}		See note 2 & 3.
		V_{ILC}	V_{SS} = –3 V		V_{SS}		0.8×V_{SS}		
High-level output voltage		V_{OHT}	I_{OH} = –3.0 mA		V_{SS}+2.4	—	—	V	OSC2 See note 4 & 5.
		V_{OHC1}	I_{OH} = –2.0 mA		V_{SS}+2.4	—	—		
		V_{OHC2}	I_{OH} = –120 µA		0.2×V_{SS}	—	—		
		V_{OHT}	V_{SS} = –3 V	I_{OH} = –2 mA	0.2×V_{SS}			V	See note 4 & 5. OSC2
		V_{OHC1}	V_{SS} = –3 V	I_{OH} = –2 mA	0.2×V_{SS}				
		V_{OHC2}	V_{SS} = –3 V	I_{OH} = –50 µA	0.2×V_{SS}				

(continued)

Parameter	Symbol	Condition		Rating Min.	Rating Typ.	Rating Max.	Unit	Applicable Pin
Low-level output voltage	VOLT	IOL = 3.0 mA		—	—	VSS+0.4	V	OSC2 See note 4 & 5.
	VOLC1	IOL = 2.0 mA		—	—	VSS+0.4		
	VOLC2	IOL = 120 µA		—	—	0.8×VSS		
	VOLT	VSS = –3 V	IOL = 2 mA			0.8×VSS	V	See note 4 & 5. OSC2
	VOLC1	VSS = –3 V	IOL = 2 mA			0.8×VSS		
	VOLC2	VSS = –3 V	IOL = 50 µA			0.8×VSS		
Input leakage current	ILI			–1.0	—	1.0	µA	See note 6.
Output leakage current	ILO			–3.0	—	3.0	µA	See note 7.
LCD driver ON resistance	RON	Ta = 25 °C	V5 = –5.0 V	—	5.0	7.5	kΩ	SEG0 to 79, COM0 to 15, See note 11
			V5 = –3.5 V	—	10.0	50.0		
Static current dissipation	IDDQ	$\overline{CS}$ = CL = VDD		—	0.05	1.0	µA	VDD
Dynamic current dissipation	IDD (1)	During display V5 = –5.0 V	fCL = 2 kHz	—	2.0	5.0	µA	VDD See note 12, 13 & 14.
			Rf = 1 MΩ	—	9.5	15.0		
			fCL = 18 kHz	—	5.0	10.0		
		During display V5 = –5 V VSS = –3 V	fCL = 2 kHz		1.5	4.5	µA	VDD See note 12 & 13.
			Rf = 1 MΩ		6.0	12.0		
	IDD (2)	During access tcyc = 200 kHz		—	300	500	µA	See note 8.
		VSS = –3V, During access tcyc = 200 kHz			150	300		
Input pin capacitance	CIN	Ta = 25 °C, f = 1 MHz		—	5.0	8.0	pF	All input pins
Oscillation frequency	fOSC	Rf = 1.0 MΩ ±2%, VSS = –5.0 V		15	18	21	kHz	See note 9.
		Rf = 1.0 MΩ ±2%, VSS = –3.0 V		11	16	21		
Reset time	tR			1.0	—		µS	$\overline{RES}$ See note 15.

Notes:
1. Operation over the specified voltage range is guaranteed, except where the supply voltage changes suddenly during CPU access.
2. A0, D0 to D7, E (or $\overline{RD}$), R/$\overline{W}$ (or $\overline{WR}$) and $\overline{CS}$
3. CL, FR, M/$\overline{S}$ and $\overline{RES}$
4. D0 to D7
5. FR
6. A0, E (or $\overline{RD}$), R/$\overline{W}$ (or $\overline{WR}$), $\overline{CS}$, CL, M/$\overline{S}$ and $\overline{RES}$
7. When D0 to D7 and FR are high impedance.
8. During continual write acess at a frequency of tcyc. Current consumption during access is effectively proportional to the access frequency.
9. See figure below for details
10. See figure below for details
11. For a voltage differential of 0.1 V between input (V1, ..., V4) and output (COM, SEG) pins. All voltages within specified operating voltage range.
12. S1D15200*10** and S1D15201*10** and S1D15202*10** only. Does not include transient currents due to stray and panel capacitances.
13. S1D15200*00** and S1D15202*00** only. Does not include transient currents due to stray and panel capacitances.
14. S1D15201*00** only. Does not include transient currents due to stray and panel capacitances.
15. tR (Reset time) represents the time from the RES signal edge to the completion of reset of the internal circuit. Therefore, the S1D15200 series enters the normal operation status after this tR.

Relationship between fosc, fFR and Rf, and operating bounds on Vss and V5

*9 • Relationship between oscillation frequency, frames and Rf
(S1D15200F00A∗), (S1D15202F00A∗)

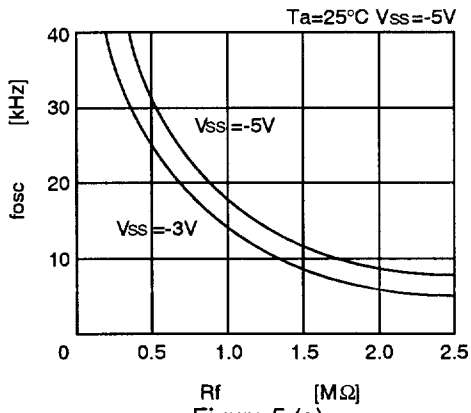


Figure 5 (a)

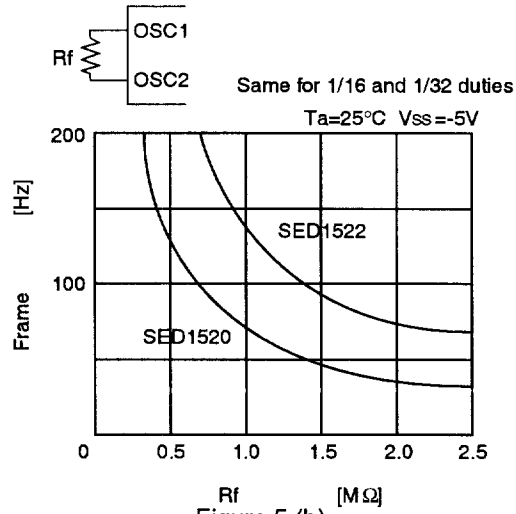


Figure 5 (b)

• Relationship between external clocks (fCL) and frames
(S1D15200F10A∗), (S1D15202F10A∗)

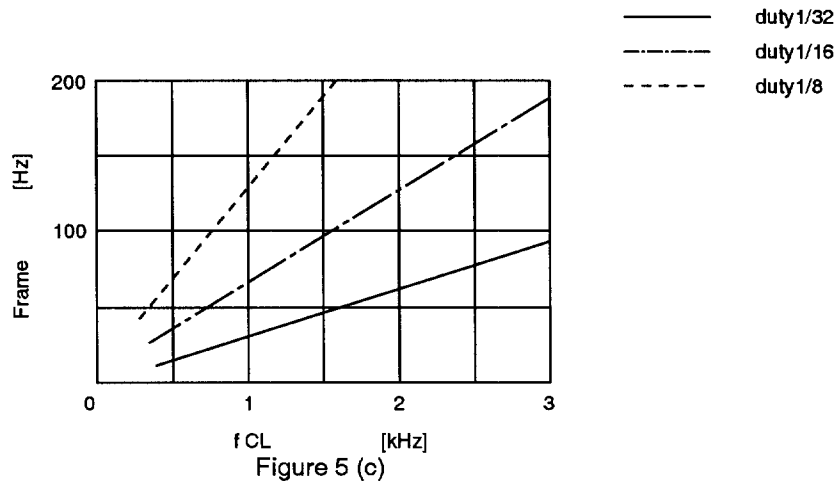


Figure 5 (c)

*10 • Operating voltage range of Vss and V5 systems

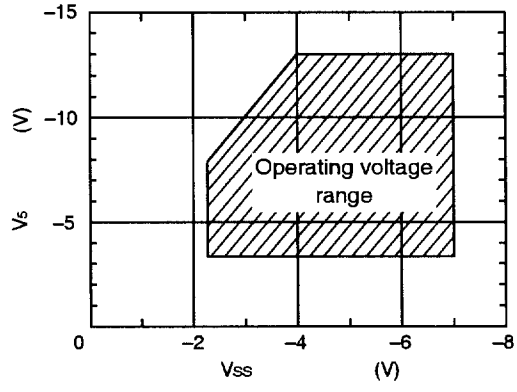
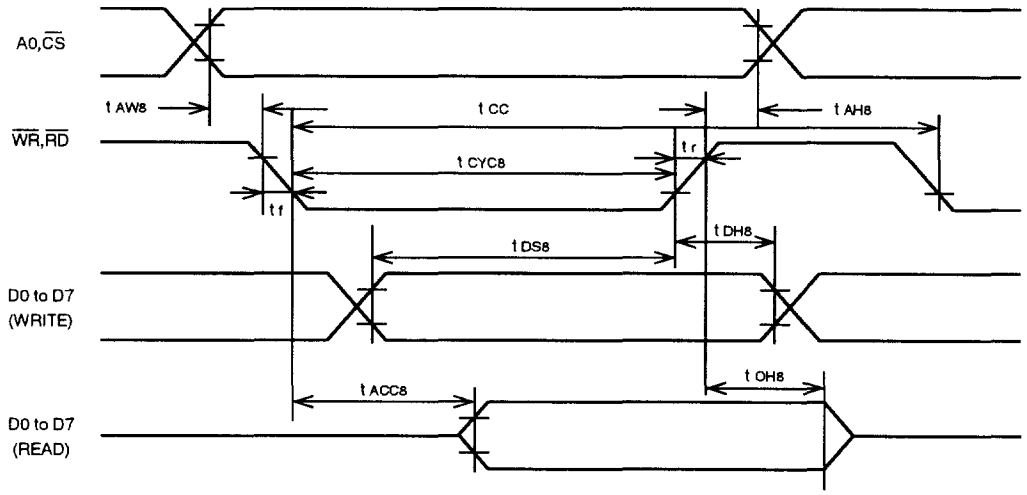


Figure 6

AC Characteristics

- MPU Bus Read/Write I (80-family MPU)



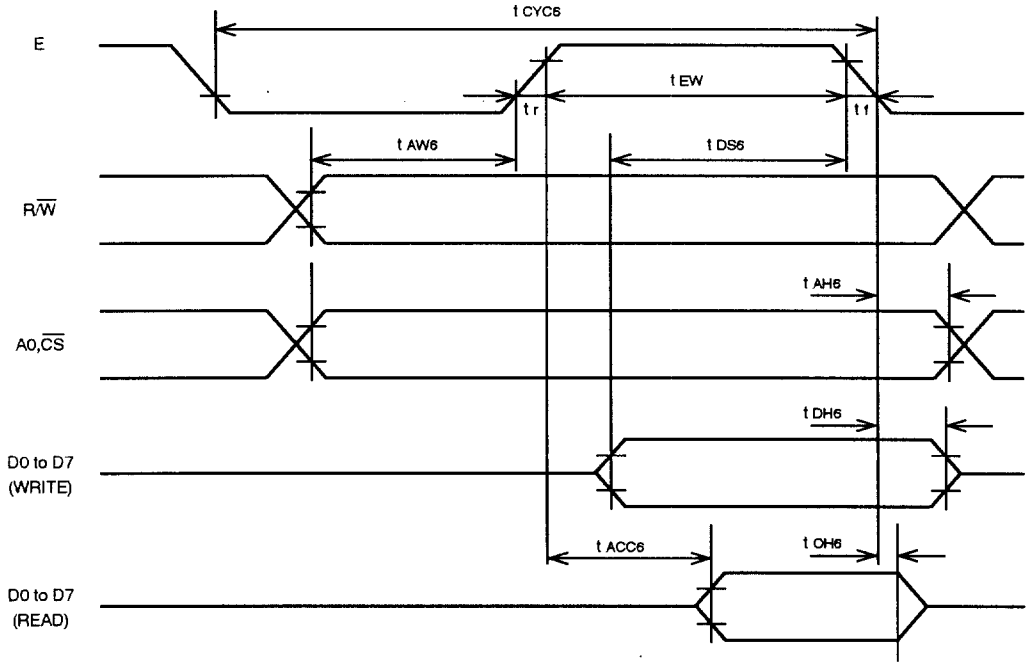
Ta = –20 to 75 °C, Vss = –5.0 V ±10% unless stated otherwise

Parameter	Symbol	Condition	Rating		Unit	Signal
			Min.	Max.		
Address hold time	tAH8		10	—	ns	A0, $\overline{CS}$
Address setup time	tAW8		20	—	ns	
System cycle time	tCYC8		1000	—	ns	$\overline{WR}$, $\overline{RD}$
Control pulsewidth	tCC		200	—	ns	
Data setup time	tDS8		80	—	ns	D0 to D7
Data hold time	tDH8		10	—	ns	
$\overline{RD}$ access time	tACC8	CL = 100 pF	—	90	ns	
Output disable time	tCH8		10	60	ns	
Rise and fall time	tr, tf	—	—	15	ns	—

(Vss = –2.7 to –4.5 V, Ta = –20 to +75°C)

Parameter	Symbol	Condition	Rating		Unit	Signal
			Min.	Max.		
Address hold time	tAH8	—	20	—	ns	A0, $\overline{CS}$
Address setup time	tAW8		40	—	ns	
System cycle time	tCYC8	—	2000	—	ns	$\overline{WR}$, $\overline{RD}$
Control pulse width	tCC		400	—	ns	
Data setup time	tDS8	—	160	—	ns	D0 to D7
Data hold time	tDH8		20	—	ns	
$\overline{RD}$ access time	tACC8	CL = 100 pF	—	180	ns	
Output disable time	tCH8		20	120	ns	
Rise and fall time	tr, tf	—	—	15	ns	—

- MPU Bus Read/Write II (68-family MPU)



Ta = –20 to 75 °C, Vss = –5 V ±10 unless stated otherwise

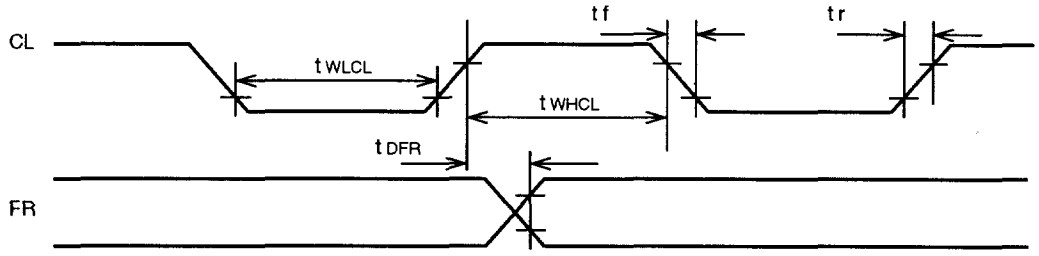
Parameter		Symbol	Condition	Rating		Unit	Signal
				Min.	Max.		
System cycle time		tCYC6		1000	—	ns	A0, CS, R/W
Address setup time		tAW6		20	—	ns	
Address hold time		tAH6		10	—	ns	
Data setup time		tDS6		80	—	ns	D0 to D7
Data hold time		tDH6		10	—	ns	
Output disable time		tOH6	CL = 100 pF	10	60	ns	
Access time		tACC6		—	90	ns	
Enable pulsewidth	Read	tEW		100	—	ns	E
	Write			80	—	ns	
Rise and fall time		tr, tf	—	—	15	ns	—

(Vss = –2.7 to – 4.5 V, Ta = –20 to +75°C)

Parameter		Symbol	Condition	Rating		Unit	Signal
				Min.	Max.		
System cycle time*1		tCYC6	—	2000	—	ns	A0, CS, R/W
Address setup time		tAW6	—	40	—	ns	
Address hold time		tAH6		20	—	ns	
Data setup time		tDS6	—	160	—	ns	D0 to D7
Data hold time		tDH6		20	—	ns	
Output disable time		tOH6	CL = 100 pF	20	120	ns	
Access time		tACC6		—	180	ns	
Enable pulse width	Read	tEW	—	200	—	ns	E
	Write			160	—	ns	
Rise and fall time		tr, tf	—	—	15	ns	—

Notes: 1. tCYC6 is the cycle time of CS. E = H, not the cycle time of E.

• Display Control Signal Timing



Input

Ta = –20 to 75 °C, Vss = –5.0 V ±10% unless stated otherwise

Parameter	Symbol	Condition	Rating			Unit	Signal
			Min.	Typ.	Max.		
Low-level pulsewidth	tWLCL		35	—	—	µs	CL
High-level pulsewidth	tWHCL		35	—	—	µs	
Rise time	tr		—	30	150	ns	
Fall time	tf		—	30	150	ns	
FR delay time	tDFR		–2.0	0.2	2.0	µs	FR

Vss = –2.7 to –4.5 V, Ta = –20 to +75°C

Parameter	Symbol	Condition	Rating			Unit	Signal
			Min.	Typ.	Max.		
Low-level pulse width	tWLCL	—	70	—	—	µs	CL
High-level pulse width	tWHCL	—	70	—	—	µs	
Rise time	tr	—	—	60	300	ns	
Fall time	tf	—	—	60	300	ns	
FR delay time	tDFR	—	–4.0	0.4	4.0	µs	FR

Note: The listed input tDFR applies to the S1D15200 and S1D15201 and S1D15202 in slave mode.

Output

Ta = –20 to 75 °C, Vss = –5.0 V ±10% unless stated otherwise

Parameter	Symbol	Condition	Rating			Unit	Signal
			Min.	Typ.	Max.		
FR delay time	tDFR	CL = 100 pF	—	0.2	0.4	µs	FR

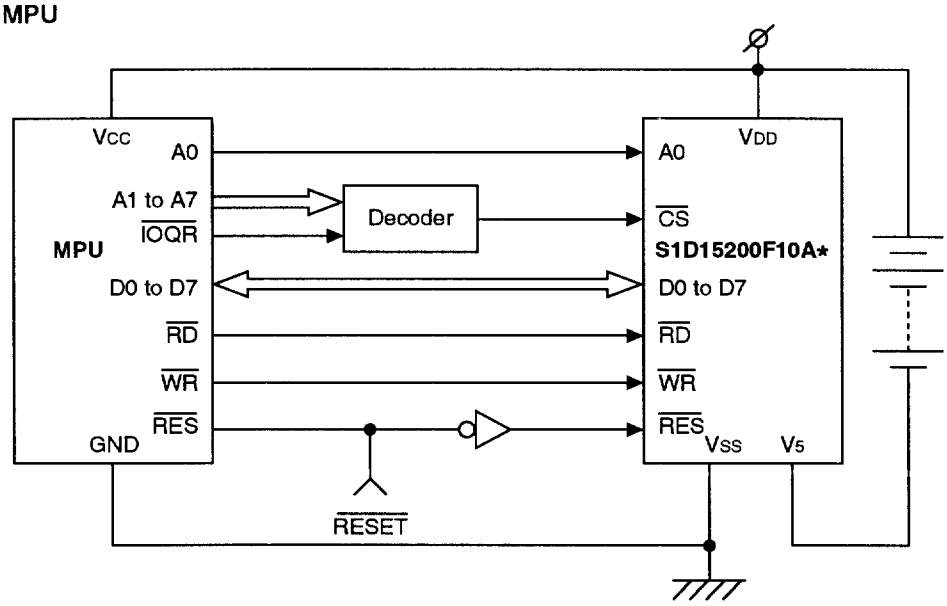
Vss = –2.7 to –4.5 V, Ta = –20 to +75°C

Parameter	Symbol	Condition	Rating			Unit	Signal
			Min.	Typ.	Max.		
FR delay time	tDFR	CL = 100 pF	—	0.4	0.8	µs	FR

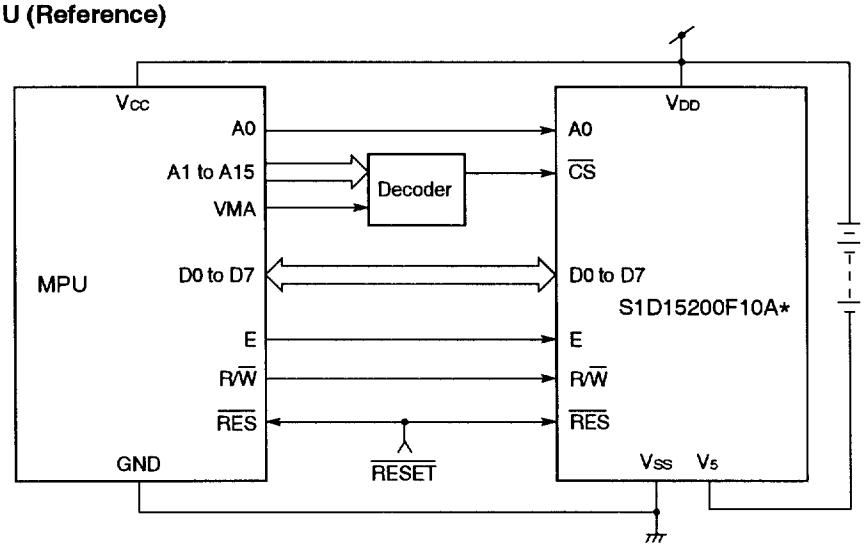
Notes: 1. The listed output tDFR applies to the S1D15200 and S1D15202 in master mode.

11. MPU INTERFACE CONFIGURATION

80 Family MPU

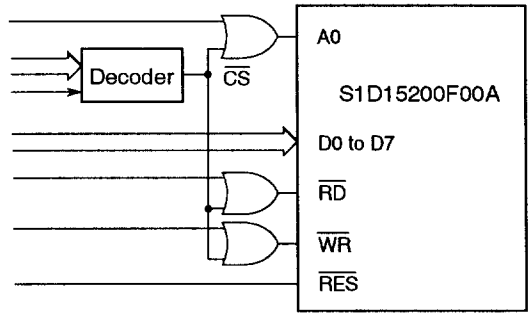


68 Family MPU (Reference)



* Refer to the figure above as to S1D15201.

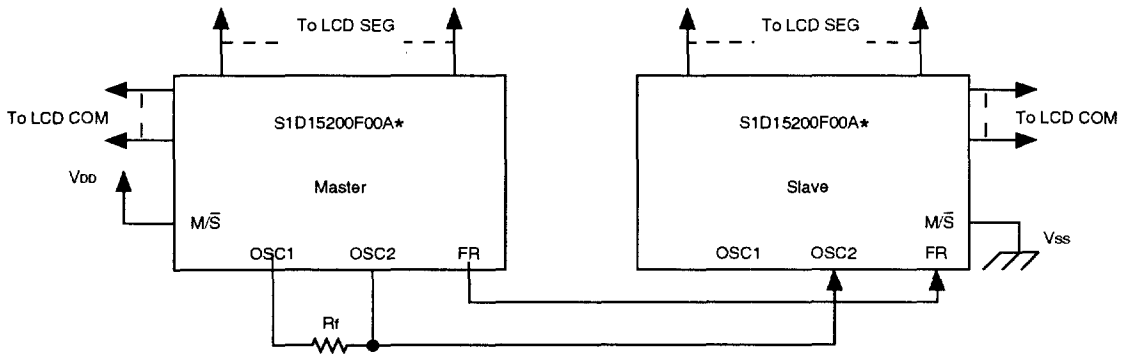
* S1D15200*00**(internal osillating) does not have $\overline{CS}$ terminal. Input OR output with $\overline{CS}$ signal to AD. $\overline{RD}$(E) $\overline{WR}$(R/$\overline{W}$)terminals as the figure belew.



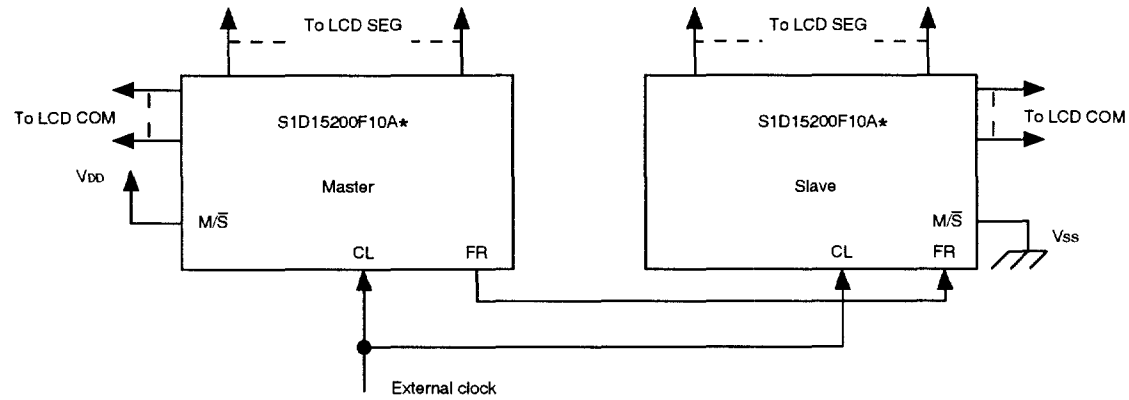
When in use of 80 Family MPU

12. LCD DRIVE INTERGFACE CONFIGURATION

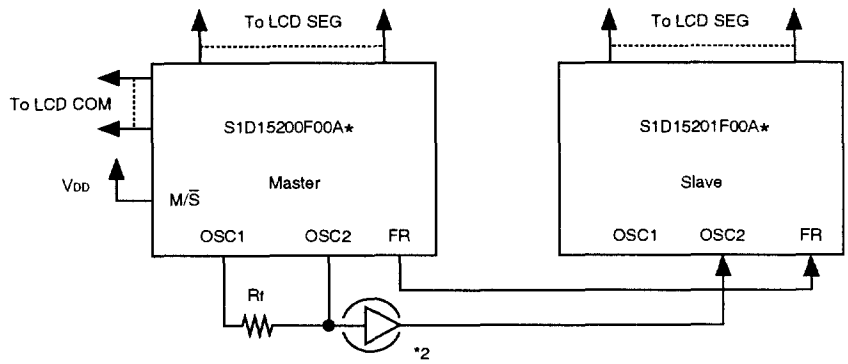
S1D15200F00A*–S1D15200F00A*
S1D15202F00A*–S1D15202F00A*



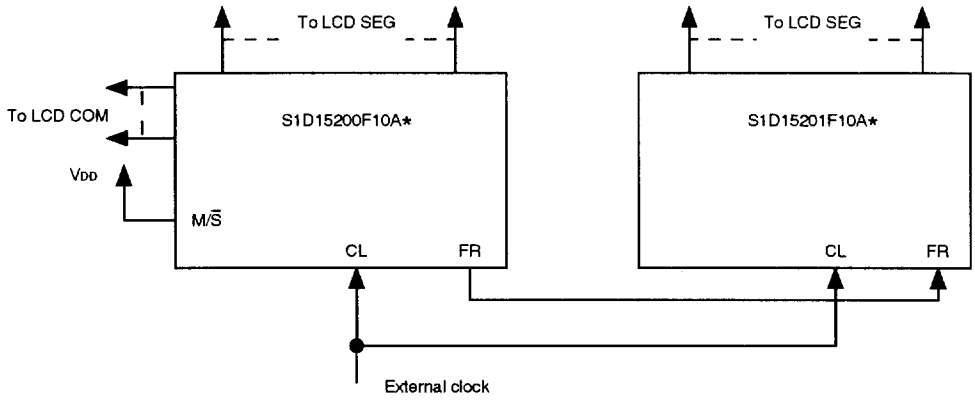
S1D15200F10A*–S1D15200F10A*
S1D15202F10A*–S1D15202F10A*



S1D15200F00A*
S1D15202F00A* **}–S1D15201F00A* (See note 1)**



S1D15200F10A*–S1D15201F10A*

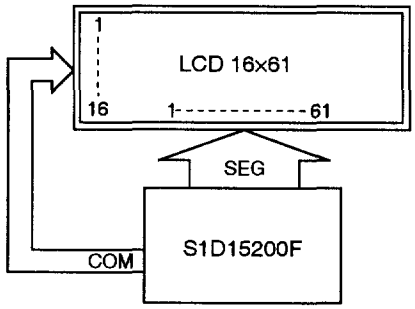


Notes: 1. The duty cycle of the slave must be the same as that for the master.
2. If a system has two or more slave drivers a CMOS buffer will be required.

13. LCD PANEL WIRING EXAMPLE
(THE FULL-DOT LCD PANEL DISPLAYS A CHARACTER IN 6×8 DOTS.)

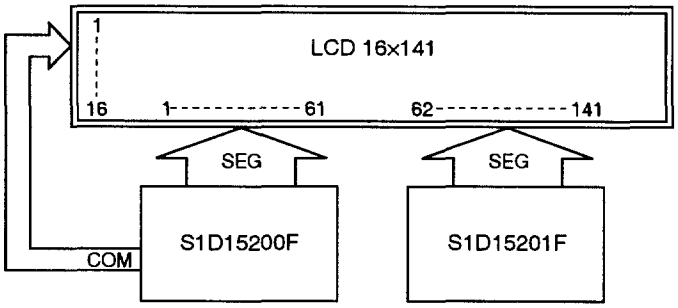
1/16 duty:

- 10 characters × 2 lines



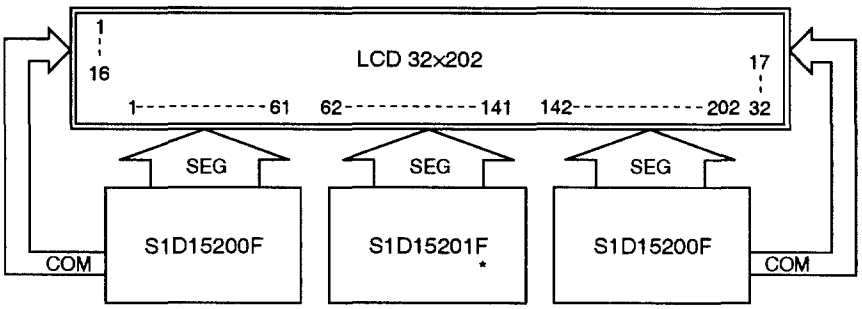
1/16 duty:

- 23 characters × 2 lines



1/32 duty:

- 33 characters × 4 lines



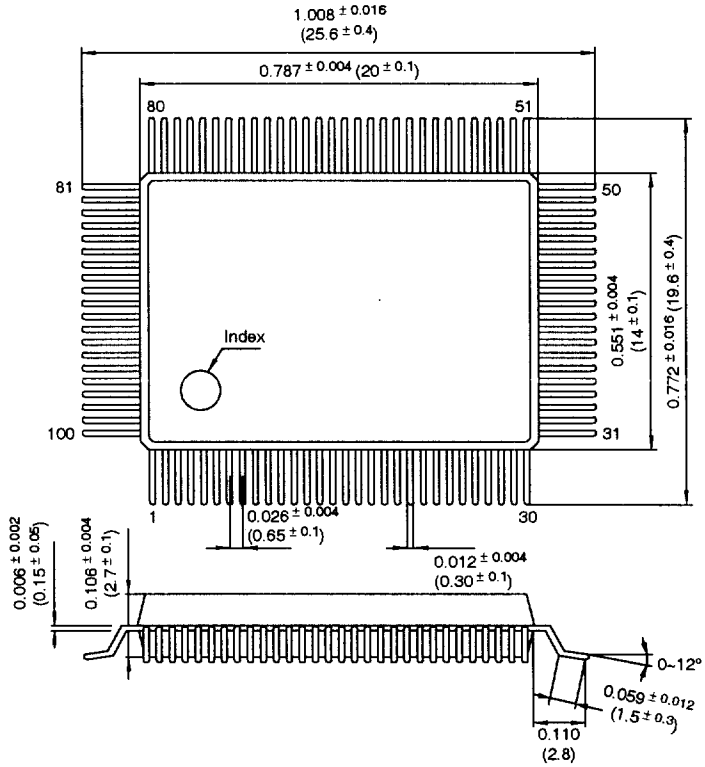
* The S1D15201F can be omitted (the 32×122-dot display mode is selected).

Note: A combination of 10B* or 10A* type chip (that uses internal clocks) and 00B* or 00A* type chip (that uses external clocks) is NOT allowed.

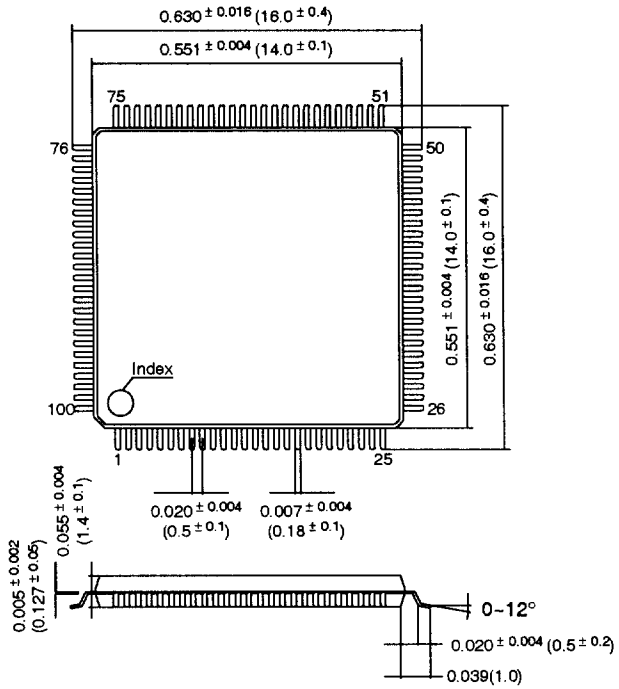
Package Dimensions

• Plastic QFP5–100 pin

Dimensions: inches (mm)



• Plastic QFP15–100 pin



TCP Dimensions