EEPLD
26V12H-20/25

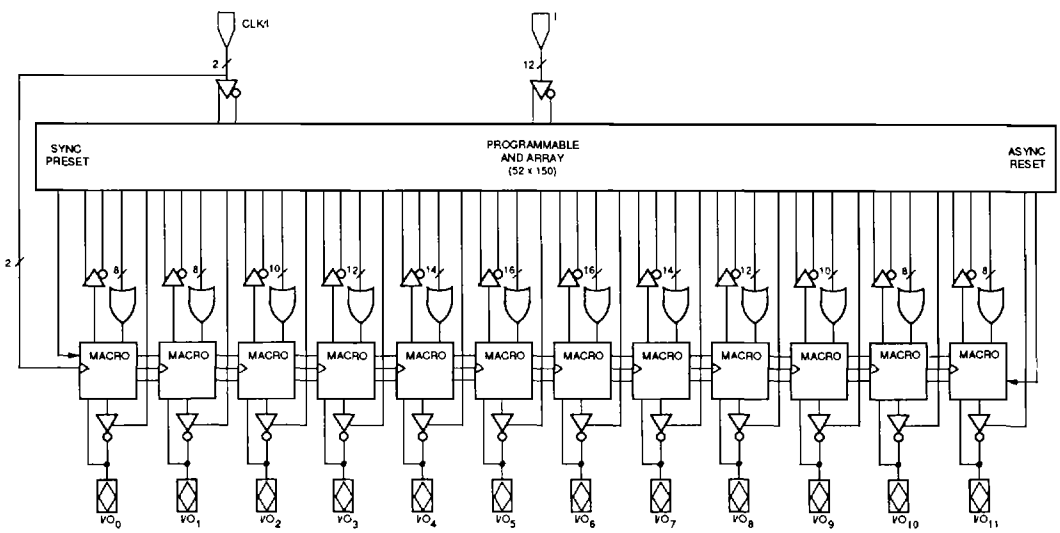
PRELIMINARY DATA SHEET *June 1989*

Features

- *28-pin versatile CMOS EEPLD with half power (only 105 mA) at high speed - 20 ns propagation delay*
- *14 dedicated inputs and 12 input/output macro cells for architectural flexibility*
- *Macro cells are a superset of the 22V10 architecture with additional feedback paths in the output logic to offer 8 different configurations*
- *Reprogrammable macro cells can be configured to be registered or combinatorial and active HIGH or active LOW*
- *Varied product term distribution allows up to 16 product terms per output*
- *Two independent clocks*
- *Extra terms provide global asynchronous reset and synchronous preset for initialization*
- *Built-in register reset on power-up and register preload to facilitate testing*
- *Quickly and easily reprogrammable in all package types*
- *Space saving 0.3" wide 28-pin Ceramic/Plastic DIP and LCC/PLCC surface mount packages*
- *Center VCC and GND pins to improve signal characteristics and minimize noise sensitivity*
- *100 reprogramming cycles, minimum*
- *Silicon security bit for design secrecy*
- *10 year data retention guaranteed*
- *Supported by ABEL™ version 3.1 software and other design tools*
- *Programmed on Sprint and other standard logic programmers*
- *Fully tested for 100% field programming/functional yield and high reliability*

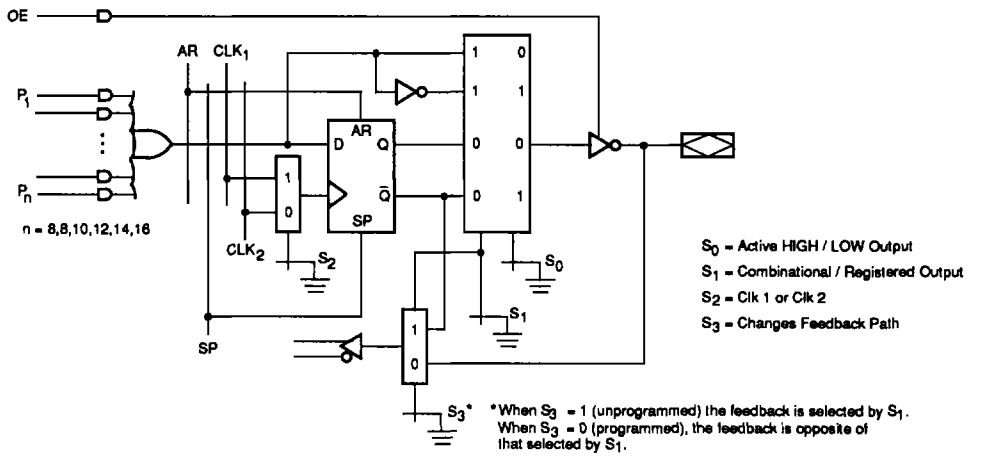
EEPLD

Block Diagram



ABEL is a trademark of DATA I/O Corporation

26V12H Super Macrocell



General Description

The EEPLD 26V12H is a 28-pin version of the popular PAL22V10 architecture. It is manufactured using SEEQ's low power, high speed, 1 micron single poly double metal Electrically Erasable CMOS technology. The 26V12H offers many unique advantages over the 22V10 because of its superior macrocell architecture. The 26V12H macrocell offers 8 distinct I/O configurations, twice that possible with the 22V10. In addition to increased functional density, the 26V12H offers low power operation at high speed when compared to 22V10 bipolar equivalents; it consumes only 105 mA (half power) with 20 ns propagation delay.

Bipolar devices cannot be reprogrammed while UV erasable PLDs can be reprogrammed only in windowed, ceramic packages. Electrically erasable devices offer reprogrammability without constraints in all package types.

Reprogrammability reduces development costs and eliminates the risks involved in preprogramming production quantities. Systems can be updated quickly by reconfiguring the EEPLDs. Reprogrammability allows SEEQ to perform extensive AC and DC tests on the EEPLDs and thus offer 100% field programming yield and high reliability.

The 26V12H with its 12 input/output macrocells utilizes the familiar sum-of-products (AND/OR) architecture that allows the designers to implement complex logic functions easily and efficiently. The user defined functions are programmed into the device through Electrically Erasable floating gate cells in the AND logic array and the macro cells. The unprogrammed state of an EE cell is a '1' while the programmed state is a '0'. In the unprogrammed state, all AND product terms float HIGH. If both true and complement of any input are connected the term will be permanently LOW.

The product terms are connected to the fixed OR array with a varied distribution. There are 6 pairs of product terms beginning at 8 product terms per output and incrementing by 2 to 16 product terms per output. The OR sum of the products feeds the output macro cell. Each macrocell can be programmed to be registered or combinatorial, active HIGH or active LOW, with registered feedback possible. The flip-flops can be clocked by one of two clock inputs to implement independent registered functions. The output configuration is determined by four electrically erasable bits controlling three multiplexers in each macro cell.

Functional Description

The EEPLD 26V12H has fourteen dedicated input lines, two of which can be used as clock inputs. Unused inputs should be tied directly to ground or V_{CC}. Buffers for device inputs and feedbacks feature both active high and active low outputs to offer user-selectable signal polarity. The inputs drive a programmable AND logic array which feeds a fixed OR logic array.

The fixed OR gates feed twelve I/O super macrocells. The 26V12H super macrocell is shown above. The super macrocell allows 8 unique output configurations, twice that possible with the 22V10 macrocell. In addition there are two clock inputs (pin1 and pin4) allowing the user to implement independent register functions.

The reprogrammable functions on the EEPLD 26V12H are automatically configured from the User's design specifications. The design specifications are processed by development software. Third party software packages like ABEL from Data I/O allow users to enter PLD designs on personal computers or engineering workstations. Common input formats are: Boolean Algebra, Truth tables, State diagrams or Schematics. The software processes the design specifications, verifies the design and automatically creates a programming file containing the EE cell pattern. These programming files, once downloaded to PLD programmers, configure PLDs according to the user's specifications.

Configuration Options

The super macrocell in the 26V12H allows 8 different output configurations as shown on page 4. The outputs can be either registered or combinatorial, and active high or active low with register or I/O pin feedback. The configuration choice is made according to the design needs of the user. Various configurations are selected by programming 4 configuration EE cell bits S_0 - S_3. EE bits S_2 and S_3 are unique to the 26V12H. The reprogrammable bits in each super macrocell control a 4:1 output multiplexer and a 2:1 feedback multiplexer. The multiplexer controls initially float to V_{CC} (1) through a reprogrammable EE cell, selecting the "1" path through the multiplexer. Programming the EE cell connects the control line to GND (0), selecting the "0" path. The state of an unprogrammed or erased EE cell is a "1" while the programmed state of the cell is a "0". See Configuration Table 1 on page 5. For details on state of EE bits S_0 - S_3 and corresponding output configuration selected. The unprogrammed state is a combinatorial active HIGH I/O pin feedback configuration.

Registered or Combinatorial Outputs

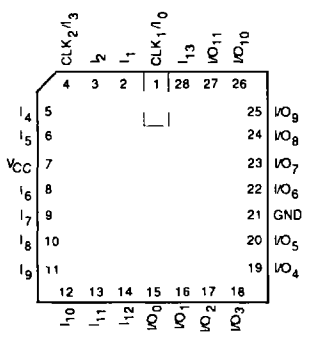
Each super macrocell of the EEPLD 26V12H includes a D-type flip-flop for data storage and synchronization. The flip-flop is loaded on the LOW to HIGH edge of the selected clock input (Clk1 - pin1 or Clk2 - pin4). Any super macrocell can be configured as combinatorial by selecting a multiplexer path that bypasses the flip-flop. Bypass is controlled by bit S_1 (Table1 page 5).

Programmable Clock

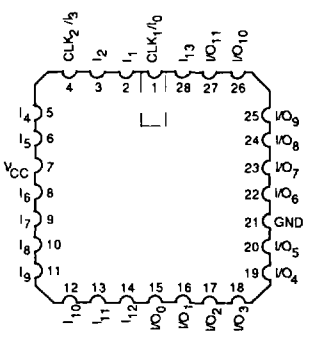
The clock input for any flip-flop can be selected from one of two inputs either pin1 or pin 4. The two individual clock

Pin Configurations (Top View)

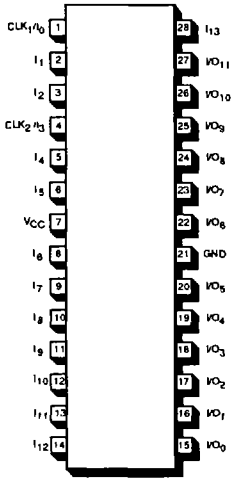
PLCC PINOUT



LCC PINOUT

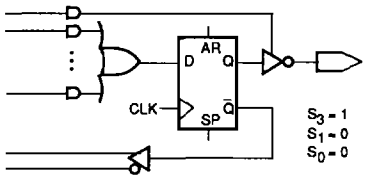


SLIM DIP PINOUT

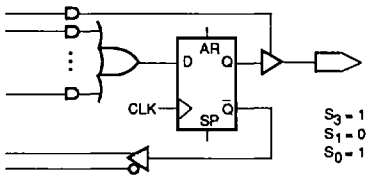


Pin Designations: I = Input
I/O = Input/Output
CLK = Clock Input
V_{CC} = Supply Voltage
GND = Ground

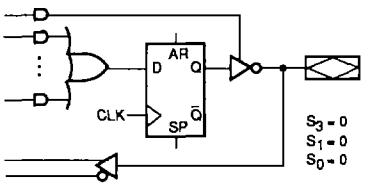
26V12H Macrocell Configuration Options



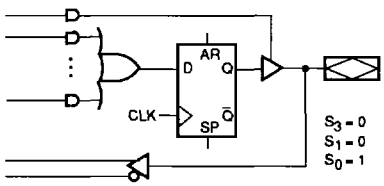
REGISTERED ACTIVE-LOW OUTPUT,
REGISTER FEEDBACK



REGISTERED ACTIVE-HIGH OUTPUT,
REGISTER FEEDBACK

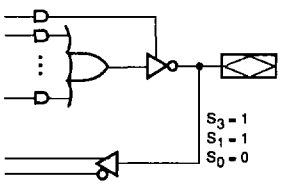


*REGISTERED ACTIVE-LOW I/O,
I/O PIN FEEDBACK

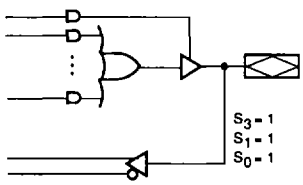


*REGISTERED ACTIVE-HIGH I/O,
I/O PIN FEEDBACK

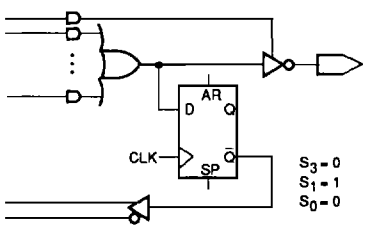
Registered Outputs



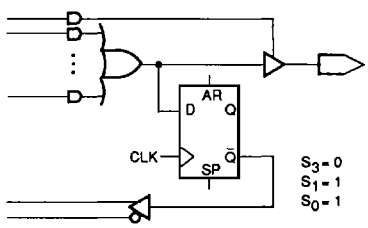
COMBINATORIAL ACTIVE-LOW I/O,
I/O PIN FEEDBACK



COMBINATORIAL ACTIVE-HIGH I/O,
I/O PIN FEEDBACK



*COMBINATORIAL ACTIVE-LOW OUTPUTS,
REGISTER FEEDBACK



*COMBINATORIAL ACTIVE-HIGH OUTPUTS,
REGISTER FEEDBACK

Combinatorial Outputs

* THESE CONFIGURATIONS ARE UNIQUE TO THE 26V12H AND ARE NOT AVAILABLE ON THE 22V10.

NOTES: BIT S_3 IS UNIQUE TO THE 26V12H
1 = UNPROGRAMMED EEBIT
0 = PROGRAMMED

Configuration Table 1

EE Bit			
S_3[1]	S_1	S_0	Output Configuartion
1	0	0	Registered Output and Feedback, Active LOW
1	0	1	Registered Output and Feedback, Active HIGH
1	1	0	Combinatorial I/O, Active LOW
1	1	1	Combinatorial I/O, Active High
0	0	0	Registered I/O, Active LOW
0	0	1	Registered I/O, Active HIGH
0	1	0	Combinatorial Output, Registered Feedback, Active LOW
0	1	1	Combinatorial Output, Registered Feedback, Active HIGH

Configuration Table 2

EE Bit	
S_2[1]	Clock Input
1	CLK_1/I_0
0	CLK_2/I_3

Notes:
1. EE Bits S2,S3 are unique to the 26V12H and are not available in 22V10.
   1 = Unprogrammed EE Bit.
   0 = Programmed EE Bit.

options provide the user flexibility to implement independent registered functions. A 2:1 multiplexer controlled by bit S_2 determines the clock input. This is an unique feature on the 26V12H (Table 2).

Programmable Feedback

The super macrocell in the 26V12H offers additional flexibility over the 22V10 when selecting feedback paths. A 2:1 multiplexer allows the user to select the feedback path from the flip-flop or the I/O pin, independent of whether the output is registered or combinatorial. Thus, registered outputs may have internal buried register feedback for higher speed (t_{CF} spec applies), or I/O feedback for use of the pin as a direct input (t_{CO} spec applies). Combinatorial outputs can be selected to have I/O pin feedback either for use of the signal in other equations or for use as another direct input or use registered feedback.

The feedback multiplexer is controlled by the same EE bit (S_1) that controls selection of registered or combinatorial outputs as on the 22V10. On the 26V12H there is an additional unique EE control bit S_3 that allows the selection of alternative feedback paths. When EE bit S_3 = 1 (unprogrammed or erased), EE bit S_1 selects register feedback for registered outputs (S_1 = 0) and I/O pin feedback for combinatorial outputs (S_1 = 1). When S_3 = 0, the opposite feedback paths are selected; I/O pin feedback for registered outputs and registered feedback for combinatorial outputs.

Programmable Enable and I/O

All super macrocells on the 26V12H have three-state output buffers controlled by individual product terms. Output enable and disable can be a function of any combination of device inputs or feedback. The super macrocell provides a bidirectional I/O pin if the I/O feedback is selected, and may be configured as a dedicated input if the buffer is always disabled. This is accomplished by connecting at least one input and its complement to the enable term, forcing the AND of the complemented inputs to be always LOW. To permanently enable the outputs, all inputs are left disconnected from the term (unprogrammed state "1").

Programmable Output Polarity

The outputs of each super macrocell can be programmed either active HIGH or active LOW to match output signal needs or to reduce product terms. The programmable output polarity feature gives the user a higher degree of flexibility when writing equations. Boolean expressions can be written in their most compact form (true or inverted) and the output can still have the desired polarity. It can also save "DeMorganizing efforts". Polarity selection is controlled by reprogrammable EE bit S_0 and affects both registered and combinatorial outputs. Polarity selection is automatic, based on the design specifications and pin definitions. If pin definition and equation for a particular output have the same polarity, the output is programmed to be active HIGH.

***Note:** Preset and reset control the flip-flop, not the output pin. The output level is determined by the output polarity selected.*

Varied Product Term Distribution

The 26V12H features a "Variable Product Term" mixture. The product terms are distributed among the twelve super macrocells in a varied manner, ranging from eight to

sixteen terms per output. The varied distribution allows optimum use of the device resources. The outputs have 8,8,10,12 or 16 product terms available for the OR gate within each macro cell.

Programmable Preset and Reset

The 26V12 also includes a synchronous preset and an asynchronous reset product term. These product terms are common to all 12 super macrocells and facilitate system initialization. The Q outputs of the registers will go to the logic High state following a Low to High transition of the clock when the synchronous preset (SP) product term is asserted. The two programmable clocks allow for implementation of independent initialization functions. The registers will be forced to the logic Low state independent of the two clocks when the asynchronous reset (AR) product term is asserted. Product term control allows preset and reset to be functions of any combination of device inputs and output feedback. The outputs will be High or Low depending on the polarity option chosen.

Power-Up Reset

All flip-flops on the 26V12H reset automatically to logic Low on power-up for predictable system initialization. Depending on the polarity option chosen, outputs will be active High or active Low. The V_{CC} rise must be monotonic and the reset delay time is 1 us maximum. The required setup and clock widths are listed in the specifications on page 15.

Register Preload

The Register Preload feature on the 26V12H allows any arbitrary state to be loaded into the device output registers. This facilitates functional testing even of complex state machine designs. This feature allows direct loading of arbitrary states that are impossible or impractical to reach otherwise. In addition, transitions from illegal states can be verified by loading illegal states and observing proper recovery. See page 14 for sequence diagram. The procedure is:

1. Raise V_{CC} to 5V +/- 0.5 V.
2. Disable output registers by setting pin 5 to V_{HH} - 10.5 +/- 0.25 V.
3. Apply V_{IL} (logic Low)/V_{IH} (logic High) as desired to all register output pins. Leave combinatorial outputs floating.
4. Clock output registers with Clock 1/Clock 2. (pins 1,4)
5. Remove high Voltage from pin 5.
7. Enable output registers per programmed pattern.
8. Verify for V_{OL}(logic Low)/V_{OH} (logic High) at all registered output pins, according to programmed polarity.

See page14 for further details.

Security Bit

Designs on the 26V12H can be secured by programming the security bit. Once programmed, this bit disables the read verify datapath of the internal programmed pattern, making it impossible to copy the EEPLD design pattern. Since EEPLDs store patterns as electrical charges on floating polysilicon gates (and not in blown fuses like other PLD technologies) it is not possible to determine the pattern by simply examining the die. A copy protected EEPLD can be reused after a block erase, which clears both the security bit and the previously programmed pattern at the same time. If the user wants to erase a secured 26V12H on a PLD programmer, but not program a new pattern, an empty JEDEC file should be loaded into the device programmer.

High Performance Packages

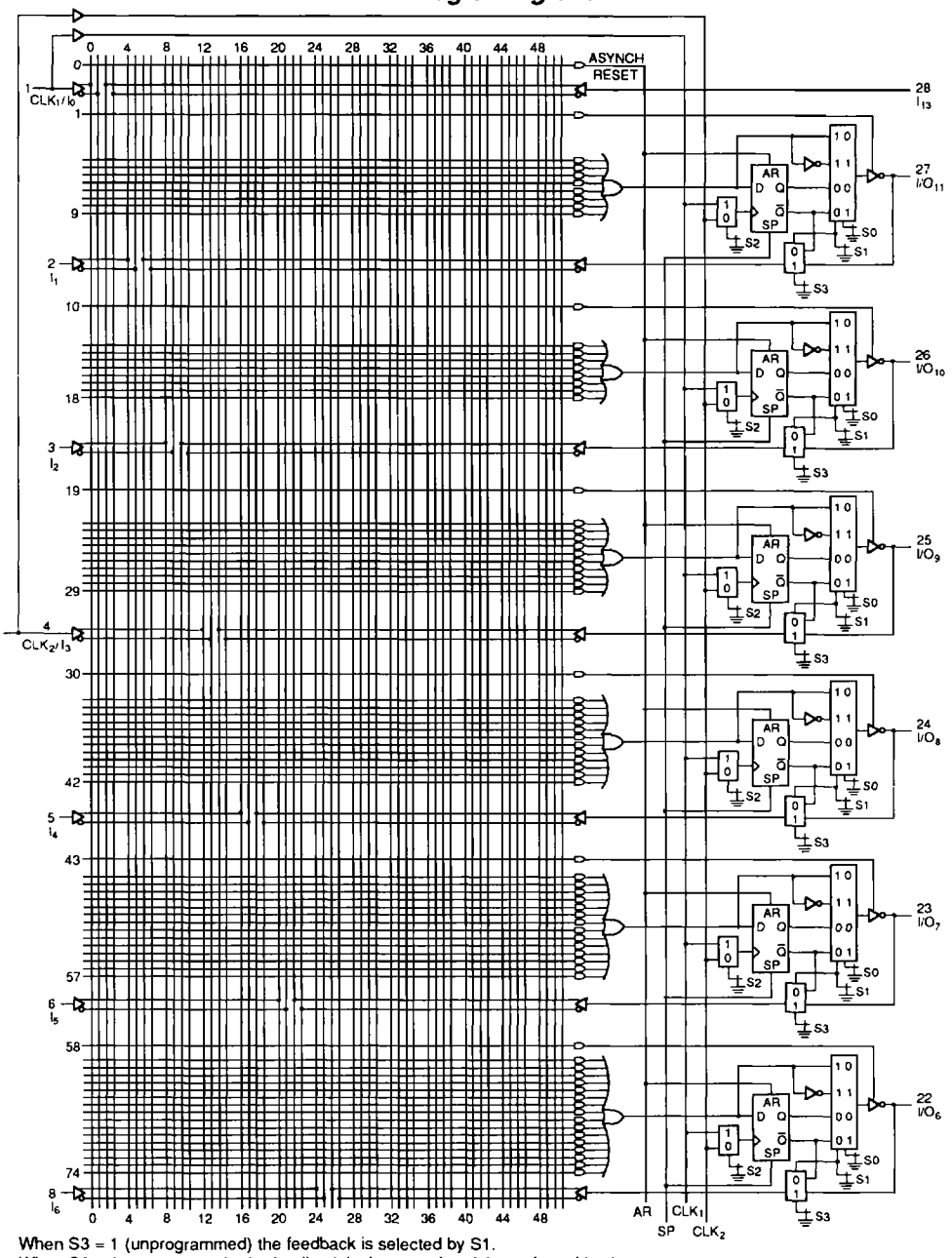
The 26V12H is offered in a 28-pin 0.3" wide slim DIP package with center power and ground. The center-pin package minimizes simultaneous switching noise effects and eases decoupling layout. This pin configuration helps to reduce the effective package inductance which contributes to the voltage noise spike caused especially during simultaneous switching of multiple EEPLD outputs. Traditional PLD pinouts place V_{CC} and GND pins at the opposite ends of the package, resulting in the maximum possible inductance through the leadframe. Placing the V_{CC} and GND pins at the center of the package results in the shortest lead length from the die to the package pin and thus offers the lowest inductance. This results in a significant reduction in the magnitude of voltage noise generated by the high speed CMOS EEPLD 26V12H during simultaneous switching of multiple outputs and enhances system noise performance.

The 26V12H is also offered in 28-pin Ceramic LCC and PLCC surface mount packages. The surface mount package options offer 100% pin utilization (unlike the 22V10).

Quality and Reliability

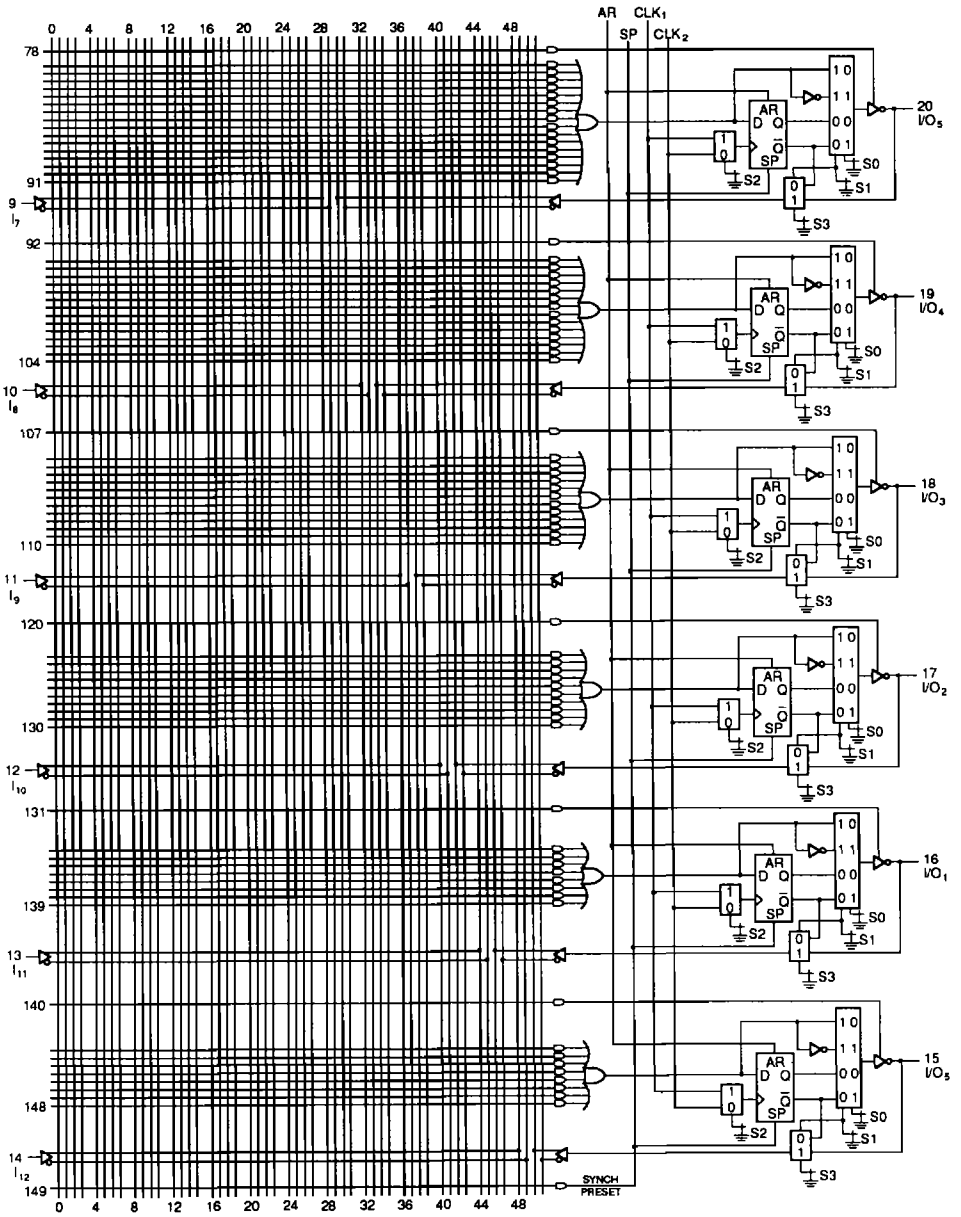
The 26V12H offers a very high level of built-in quality and reliability due to its EE CMOS technology. Its reprogrammable EE cells allow SEEQ to perform complete Cell, AC, DC and Functionality testing during manufacture. It is important to note that the elements tested are the same elements normally programmed by the user to implement a logic function. There are no special test rows, columns or 'Phantom' arrays. EE CMOS technology allows actual device signal paths to be tested prior to shipment from the factory without the need for simulation or correlation. The user gets the benefit of 100% field programming and functionality of SEEQ EEPLDs.

26V12H Logic Diagram



When S3 = 1 (unprogrammed) the feedback is selected by S1.
When S3 = 0 (programmed), the feedback is the opposite of that selected by S1.

26V12H Logic Diagram (cont'd)



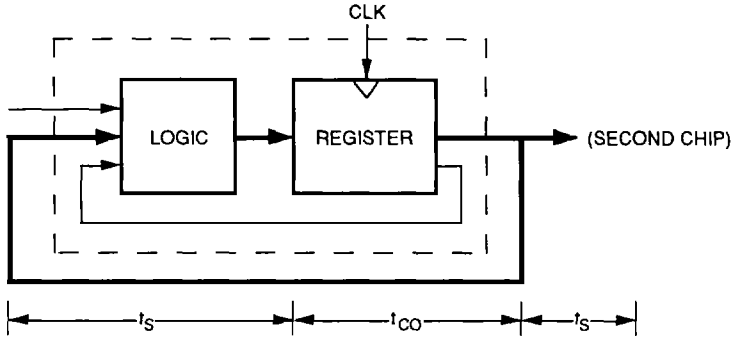
When S3 = 1 (unprogrammed) the feedback is selected by S1.
When S3 = 0 (programmed), the feedback is the opposite of that selected by S1.

f_{MAX} Parameters

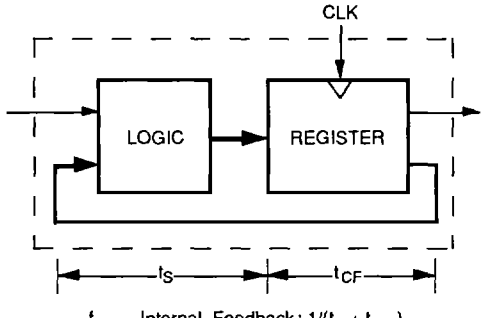
The parameter f_{MAX} is the maximum clock rate at which the device is guaranteed to operate. Because flexibility inherent in programmable logic devices offers a choice of clocked flip-flop designs, f_{MAX} is specified in this case for two types of synchronous designs.

The first type of design is a state machine with feedback signals sent off-chip. This external feedback could go back to the device inputs, or to a second device in a multi-chip state machine. The slowest path defining the period is the sum of the clock-to-output time and input setup time for the external signals ($t_S + t_{CO}$). The reciprocal, f_{MAX}, is the maximum frequency with external feedback or in conjunction with an equivalent speed device. This f_{MAX} is designated "f_{MAX}, External Feedback."

The second type of design is a single-chip state machine with internal feedback only. In this case, flip-flop inputs are defined by the device inputs and flip-flop outputs. Under these conditions, the period is limited by the internal delay from the flip-flop outputs through the internal feedback and logic to the flip-flop inputs ($t_S + t_{CF}$). This f_{MAX} is designated "f_{MAX} internal."



$f_{MAX,\ External\ Feedback}$; $1/(t_S + t_{CO})$



f_{MAX} Internal Feedback; $1/(t_S + t_{CF})$

Absolute Maximum Ratings

Supply voltage, V_{CC} ..... −0.5 V to 7 V
DC input voltage, V_I ..... −0.5 V to V_{CC} + 0.5 V
DC output voltage V_O ..... −0.5 V to V_{CC} + 0.5 V
DC output source/sink current per output pin, I_O ..... ±35 mA
DC V_{CC} or ground current, I_{CC} or I_{GND} ..... ±100 mA
Input diode current, I_{IK}
V_I < 0 ..... −20 mA
V_I > V_{CC} ..... +20 mA
Output diode current, I_{OK}
V_O < 0 ..... −20 mA
V_O > V_{CC} ..... +20 mA
Storage temperature ..... −65°C to 150°C
Static discharge voltage ..... > 2001 V
Latchup current ..... > 100 mA
Ambient temperature under bias ..... −55°C to +125°C

Stresses above those listed under ABSOLUTE MAXIMUM RATING may cause permanent device failure. Functionality at or above these limits is not implied. Exposure to absolute maximum ratings for extended periods may affect device reliability.

Operating Ranges

Commercial (Q) Devices
Temperature (T_A)
Operating Free Air ..... 0°C to +75°C
Supply voltage, V_{CC} ..... 4.75 V to 5.25 V
Industrial (E) Devices
Temperature (T_A)
Operating Free Air ..... −40°C to +85°C
Supply voltage, V_{CC} ..... 4.5 V to 5.5 V

Operating ranges define those limits between which the functionality of the device is guaranteed.

DC Characteristics (over operating conditions unless otherwise specified)

Parameter Symbol	Parameter Description	Test Conditions	Min.	Max.	Unit
V_{OH}	Output HIGH Voltage	V_{CC} = Min., I_{OH} = −3.2 mA V_{IN} = V_{IH} or V_{IL}	2.4		V
V_{OL}	Output LOW Voltage	V_{CC} = Min., I_{OL} = 16 mA V_{IN} = V_{IH} or V_{IL}		0.4	V
V_{IH} (Note 1)	Input HIGH Voltage	Guaranteed Input Logical HIGH Voltage for all Inputs	2.0		V
V_{IL} (Note 1)	Input LOW Voltage	Guaranteed Input Logical LOW Voltage for all Inputs		0.8	V
I_{IZ}	Input Leakage Current	V_{IN} = 0 to 5.5 V, V_{CC} = Max.	−10	10	µA
I_{OZ}	Output Leakage Current	V_{OUT} = 0 to 5.5 V, V_{CC} = Max.	−10	10	µA
I_{SC}	Output Short-Circuit Current	V_{CC} = Max., V_{OUT} = 0.5 V (Note 2)	−30	−130	mA
I_{CC}	Operating Supply Current	V_{IN} = 0 V, Outputs Open (I_O = 0 mA)		105	mA

Notes:
1. These are absolute values with respect to the device ground and all overshoots due to system and tester noise are included.

2. Not more than one output should be tested at a time. Duration of the short-circuit test should not exceed one second. V_{OUT} = 0.5 V has been chosen to avoid test problems caused by tester ground degradation.

Capacitance (Note 1)

Parameter Symbol	Parameter Description	Test conditions	Typ.	Unit
C_{IN}	Input capacitance	V_{CC} = 5.0 V, T = +25°C V_{IN} = 2.0 V at f = 1.0 MHz	5	pF
C_{OUT}	Output capacitance		8	

Note:
1. These parameters are not 100% tested, but are evaluated at initial characterization and at any time the design is modified where capacitance may be affected.

Switching Characteristics (over commercial operating range (Note 1)

Parameter Symbol	Parameter Description		-20		-25		Unit
			Min.	Max.	Min.	Max.	
t_{PD}	Input or Feedback to Combinatorial Output	Active LOW / Active HIGH		20		25	ns
t_S	Setup Time for Input, Feedback, or SP to Clock		13		15		ns
t_H	Hold Time		0		0		ns
t_{CO}	Clock to Output			12		15	ns
t_{CF}	Clock to Feedback			10		13	ns
t_{AR}	Asynchronous RESET to Registered Output			25		30	ns
t_{ARW}	Asynchronous RESET Width		20		25		ns
t_{ARR}	Asynchronous RESET Recovery Time		20		25		ns
t_{SPR}	Synchronous PRESET Recovery Time		13		15		ns
t_{WL}	Width of Clock	LOW	10		13		ns
t_{WH}		HIGH	10		13		ns
f_{MAX}	Maximum Frequency	Extenal Feedback $1/(t_S + t_{CO})$		40		33.3	MHz
		Internal Feedback $1/(t_S + t_{CF})$		43		35	
t_{EA}	Input to Output Enable			20		25	ns
t_{ER}	Input to Output Disable			20		25	ns

Notes:

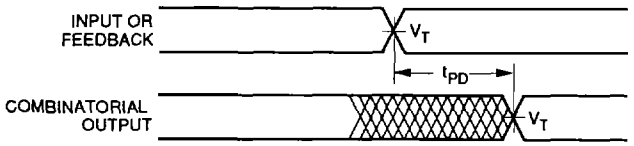
1. Commercial Test Conditions: see Switching Test Load.
2. These parameters are not 100% tested, but are calculated at initial charaterization and at any time the design is modified where frequency may be affected.

Data Retention and Endurance

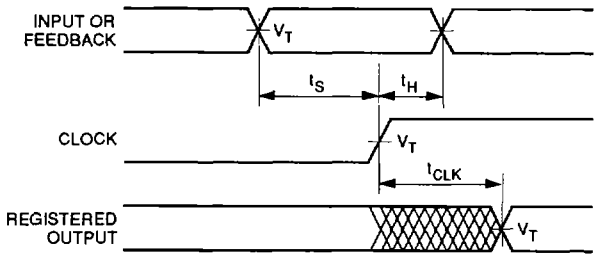
Symbol	Parameter	Value	Unit	Conditions
t_{DR}	Pattern data retention time	> 10	years	Max. storage temperature Mil-STD 883 Test Method 1008
N	Min. reprogramming cycles	100	cycles	Operating conditions

Switching Waveforms

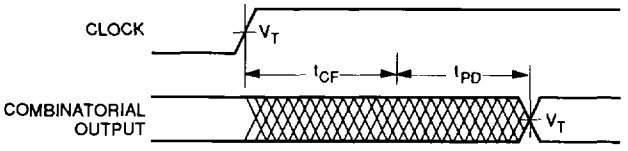
COMBINATORIAL OUTPUT



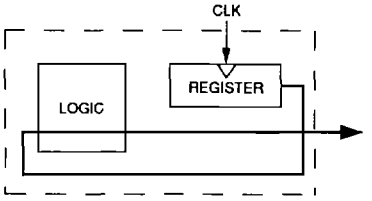
REGISTERED OUTPUT



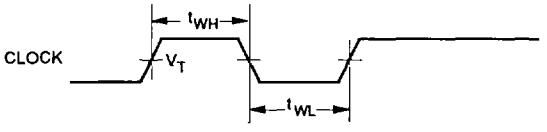
CLOCK TO FEEDBACK TO COMBINATORIAL OUTPUT



(see path below)

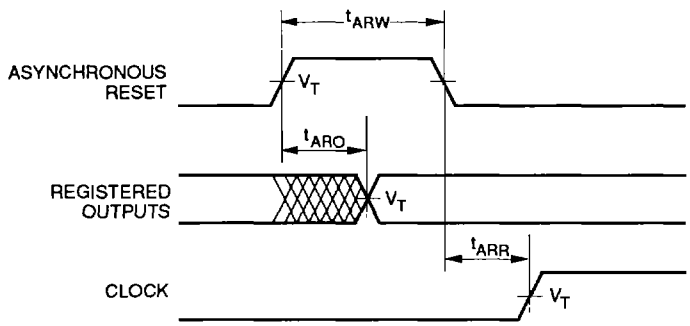


CLOCK WIDTH

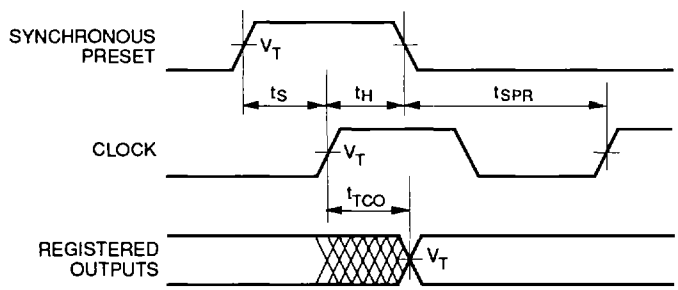


Switching Waveforms (continued)

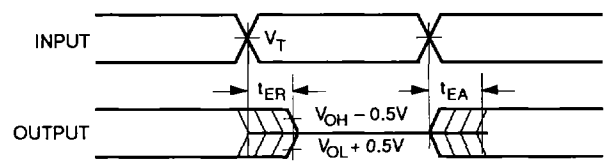
ASYNCHRONOUS RESET



SYNCHRONOUS PRESET



INPUT TO OUTPUT DISABLE/ENABLE

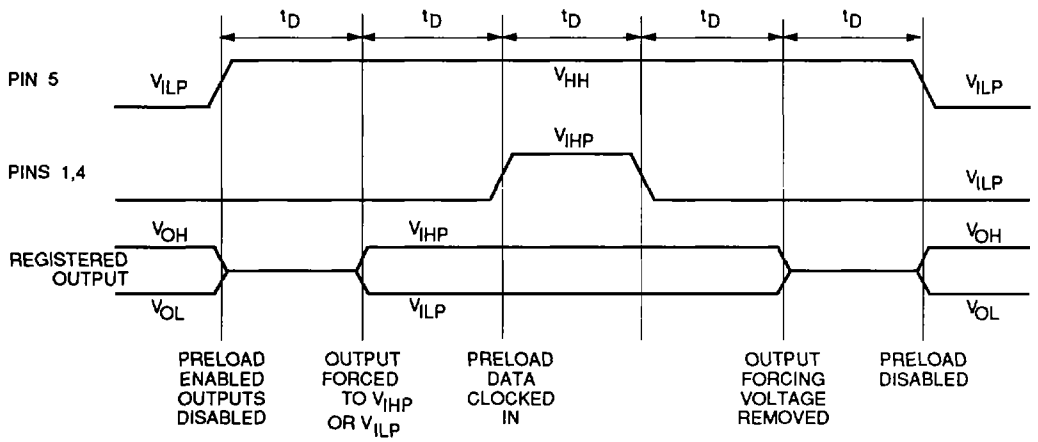


Notes:
1. V_T = 1.5 V.
2. Input pulse amplitude 0 V to 3.0 V.
3. Input rise and fall times 2 – 5 ns typical.

Output Register Preload

The PALCE26V12H registered outputs are provided with circuitry to allow loading each register synchronously with either a HIGH or LOW. This feature will simplify testing since any state can be loaded into the registers to control test sequencing.

The pin levels and timing necessary to preform the PRELOAD function are detailed below.

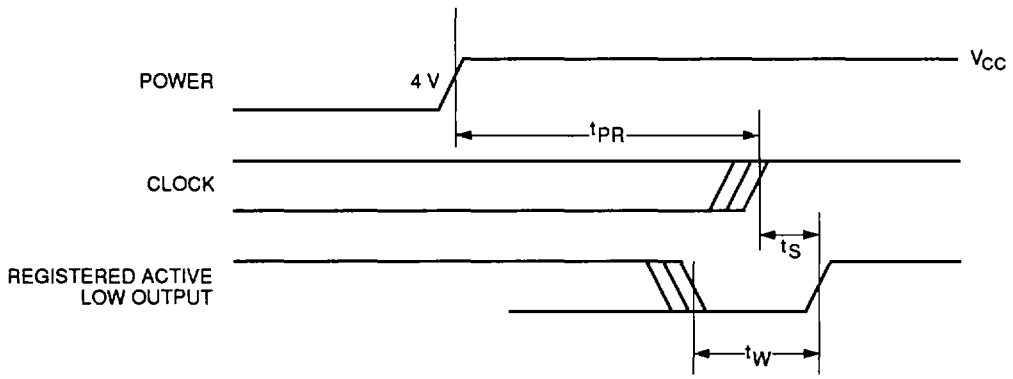


Par.	Min.	Max.	Unit	Level forced on registered output pin during PRELOAD cycle	Registered Q output state after cycle
V_{HH}	10.25	10.75	V		
V_{ILP}	0	0.5	V		
V_{IHP}	2.4	5.5	V	V_{IHP}	High
t_0	10		µs	V_{ILP}	Low

Power-Up Reset

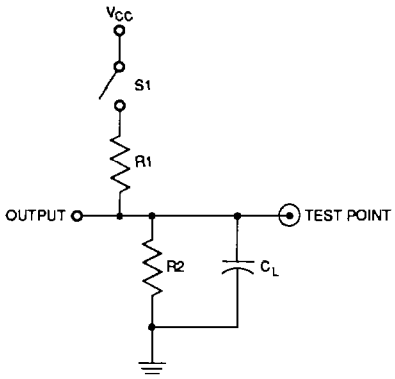
SEEQ 26V12H has been designed with the capability to reset during system power-up. Following power-up, all registers will be reset to LOW. The output state will depend on the polarity of the output buffer. This feature provides extra flexibility to the designer and is especially valuable in simplifying state machine initialization. A timing diagram and parameter table are shown below. Due to the asynchronous operation of the power-up reset, and the wide range of ways V_{CC} can rise to its steady state, two conditions are required to ensure a valid power-up reset. These conditions are:

1. The V_{CC} rise must be monotonic.
2. Following reset, the clock input must not be driven from LOW to HIGH until applicable input and feedback setup times are met.



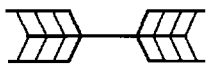
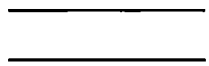
Parameter Symbol	Parameter Description	Min.	Typ.	Max.	Unit
t_{PR}	Power-Up Reset Time		600	1000	ns
t_s	Input or Feedback Setup Time	See Switching Characteristics Table			
t_w	Clock Width				

Switching Test Laod



Specification	Switch S1	C_L	R_1	R_2	Measured Output Value
t_{PD}, t_{CO}, t_{CF}	Closed	50 pF	300 Ω	390 Ω	1.5V
t_{EA}	Z –> H: open Z –> L: closed	50 pF	300 Ω	390 Ω	1.5V
t_{ER}	H –> Z: open L –> Z: closed	5 pF	300 Ω	390 Ω	H –> Z: V_{OH} –0.5 V L –> Z: V_{OL} + 0.5V

Key to Timing Diagrams

WAVEFORM	INPUTS	OUTPUTS
	DON'T CARE: CHANGE PERMITTED	CHANGING: STATE UNKNOWN
	NOT APPLICABLE	CENTER LINE IS HIGH IMPEDANCE STATE
	MUST BE STEADY	WILL BE STEADY

PLD Development

Development software assists the user in implementing a design in one or several PLDs. The software converts the user's input into a device dependent fuse map in JEDEC format. The software package listed below support & the EEPLD 26V12H. For more information about PLD development software contact SEEQ Technology or the software vendor directly:

DATA I/O Corp.
10525 Willows Road, NE, P.O. Box 97046,
Redmont, WA 98073-9746
(800) 247-5700
Software offered: ABEL, PLD Test

PLD Development

Data I/O ABEL version 3.1 release supports the SEEQ EEPLD 26V12H. This section describes ABEL 3.1 release features as applied to the 26V12H. For detailed software documentation refer to ABEL manual from Data I/O.

SEEQ EEPLD 26V12H architecture is a superset of the 22V10. Each super macrocell on the 26V12H allows eight output configurations. See macrocell configuration options (Page 4). Configuration Tables 1 and 2 list the EEbit settings for the various options. The designer can program the 26V12H to operate like a 22V10 by using the following configuration:

- *Combinatorial output, I/O combinatorial feedback.*
- *Registered output, registered feedback.*

When output pin equations alone are used in design specifications, ABEL automatically selects I/O feedback for combinatorial output equations and registered feedback for registered equations (i.e, EEbit S3 defaults to 1). The designer has the flexibility to configure all or some of the 26V12H super macrocells to operate like 22V10 design.

***Example 1** shows the listing of a 22V10 example from Data I/O's ABEL design examples list converted into a 26V12H design. Notice the **new pin assignments** and reset node definition.*

Device nodes:

*The internal nodes on the 26V12H have been assigned specific numbers. See ABEL user documentation for node assignment list. The relevant nodes can also be referred by using the Dot extension notation. See **Example 2**. ABEL user documentation provides detailed description.*

26V12H super macrocell Configuration:

***Example 2** shows the listing of 26V12H from ABEL's design example list. Notice the use of various configuration options.*

***Clk1, Clk2 pins:** The two clock pins 1, 4 on the 26V12H allow the designer flexibility in selecting either one or both of the clock inputs for registered configurations. The ABEL software defaults to Clk1 from pin1 if no clock function is defined for a registered output.*

***Output super macrocell control:** ABEL's 'ISTYPE' statement can be used to explicitly define the super macrocell configuration. Or the ISTYPE statement can be used to define the feedback point only, leaving the polarity and register/combinatorial selection to be determined by ABEL from the equations.*

The following four output configurations are unique to the 26V12H and cannot be implemented on the 22V10.

- *Combinatorial output, registered feedback with active-low or active-high outputs.*
- *Registered output, I/O registered feedback with active-low or active-high.*

For example, to configure an output macrocell as combinatorial with registered feedback, the following 'ISTYPE' statement can be used:

```
Q15 istype 'com,feed_reg';
```

Output polarity can be controlled by entering "pos" or "neg" in the ISTYPE statement. In which case the statement would be:

```
Q15 istype 'pos,com,feed_reg';
```

***Example 2** uses ABEL's Dot extension notation for accessing internal nodes. ABEL will automatically choose whether to bypass or select a register based on the form of equation written for the output. The ISTYPE statement is used to explicitly declare an output configuration. Also, notice the use of registered feedback as input for output Q18.*

For a more complete description on ABEL features refer to the ABEL user documentation.

EXAMPLE 1

```
module _MuxAdd flag '-r3'
title '5-bit ripple adder with input multiplex
Michael Holley   FutureNet Division, Data I/O Corp.
Redmond WA   14 July 1987'

  MuxAdd device 'P26V12';

  AddClk,Clr,Add10,Sub10,is_Ace pin  1, 9, 8, 10,20;
         V4,V3,V2,V1,V0   pin  6, 5, 4, 3, 2;
         S4,S3,S2,S1,S0                  pin 15,16,17,18,19;
         C4,C3,C2,C1                     pin 26,27,22,23;

         Reset                           node 29;

         X,C,L,H     = .X., .C.,  0,   1;

         Card        = [ V4, V3, V2, V1, V0 ];
         Score       = [ S4, S3, S2, S1, S0 ];
         CarryIn     = [ C4, C3, C2, C1,  0 ];
         CarryOut    = [  X, C4, C3, C2, C1 ];
         ten         = [  0,  1,  0,  1,  0 ];
         minus_ten   = [  1,  0,  1,  1,  0 ];

" Input Multiplexer
         Data       =  Add10  &  Sub10   &   Card
                    # !Add10  &  Sub10   &   ten
                    #  Add10  & !Sub10   &   minus_ten;
equations
         Score      := Data   $ Score    $ CarryIn;

         CarryOut   = Data    & Score    # (Data # Score) & CarryIn;

         Reset      = !Clr;               "Async reset node for registers

         is_Ace     = Card == 1;

test_vectors
         ([AddClk,Clr,Add10,Sub10,Card] -> [Score,is_Ace])
         [   L  , L ,  H  ,  H  ,  X ] -> [  0  ,   L  ]; "Clear
         [   C  , H ,  H  ,  H  ,  7 ] -> [  7  ,   L  ];
         [   C  , H ,  H  ,  H  , 10 ] -> [ 17  ,   L  ];
         [   L  , L ,  H  ,  H  ,  X ] -> [  0  ,   L  ]; "Clear
         [   C  , H ,  H  ,  H  ,  1 ] -> [  1  ,   H  ];
         [   C  , H ,  L  ,  H  ,  1 ] -> [ 11  ,   H  ]; "Add 10
         [   C  , H ,  H  ,  H  ,  4 ] -> [ 15  ,   L  ];
         [   C  , H ,  H  ,  H  ,  8 ] -> [ 23  ,   L  ];
         [   C  , H ,  H  ,  L  ,  8 ] -> [ 13  ,   L  ]; "Subtract 10
         [   C  , H ,  H  ,  H  ,  5 ] -> [ 18  ,   L  ];
end _MuxAdd
```

EXAMPLE 2

```
module P26V12
title 'Bob Hamilton     Data I/O     Dec. 1988'

        p26v12              device 'P26V12';

        Clk1,Clk2                   pin 1,4;
        I2,I3,I5                    pin 2,3,5;
        Q15,Q16,Q17,Q18             pin 15,16,17,18;

LIBRARY 'constant';

        Q15 istype 'com,feed_reg'; " Combinatorial with registered feedback
        Q16 istype 'reg,feed_pin'; " Registered with pin feedback
        Q17 istype 'reg,feed_reg'; " Registered with registered feedback
        Q18 istype 'com,feed_pin'; " Combinatorial with pin feedback

equations
        [Q15.OE,Q16.OE,Q17.OE,Q18.OE] = ^b1111; " All outputs enabled

        Q15.C = Clk2; " Clock pin 15 register with pin 4
        Q16.C = Clk1; " Clock pin 16 register with pin 1
        Q17.C = Clk2; " Clock pin 17 register with pin 4
        Q16 := I2;    " Registered output, input is pin 2
        Q17 := I3;    " Registered output, input is pin 3
        Q15  = I5;    " Combinatorial output, input is pin 5
        Q18  = Q15.Q; " Combinatorial output, input is pin I5 reg. feedback

test_vectors
        ([Clk1,Clk2,I2,I3,I5] -> [Q15,Q16,Q17,Q18])
        [ C,   0,  1, 1, 1 ] -> [ H , H , L,  L ];
        [ 0,   C,  0, 1, 1 ] -> [ H , H , H,  H ];
        [ C,   0,  0, 0, 0 ] -> [ L , L , H,  H ];
        [ 0,   C,  0, 0, 0 ] -> [ L , L , L,  L ];

end P26V12
```

PLD Programming

The 26V12H can be programmed on standard logic programmers. Previously programmed devices can be reprogrammed easily, using exactly the same procedure as required for blank EEPLDs. If the user wants to erase a 26V12H, but not program it to a new pattern, an empty JEDEC file should be loaded into the device programmer.

PLD Programmer Vendors

Adams MacDonald
800 Airport Road, Monterey, CA 93940
(408) 373-3607

DATA I/O Corp.
10525 Willows Road NE, P.O. Box 97046
Redmont, WA 98073-9746
(800) 247-5700

PLD Programming Equipment:
Unisite V 2.5

PROMAC
see Adams MacDonald

Stag Microsystems Inc.
1600 Wyatt Dr., Santa Clara CA 95054
(408) 988-1118

For more information about PLD programmers contact SEEQ Technology or the programmer vendor directly.

Sprint
see Adams MacDonald

Ordering Information