Precision Clock Synthesizer for Mobile PCs

Features

- Two copies of CPU clock
- 100 MHz or 66.6 MHz operation
- Six copies of PCI clock, (synchronous with CPU clock)
- Two copies of REF clock @ 14.31818 MHz
- One copy of 48 MHz
- One copy of selectable 48/24 MHz
- Power management control input pins
- Isolated core V_{DD}, V_{SS} pins for noise reduction
- 28-pin SSOP (H28) and TSSOP (L28) packages
- SSC Options:

Device	66 MHz	100 MHz
PI6C103	–0.67%	–0.65%
PI6C103-05	–1.35%	–1.35%
PI6C103-06	–1.79%	–1.79%

Description

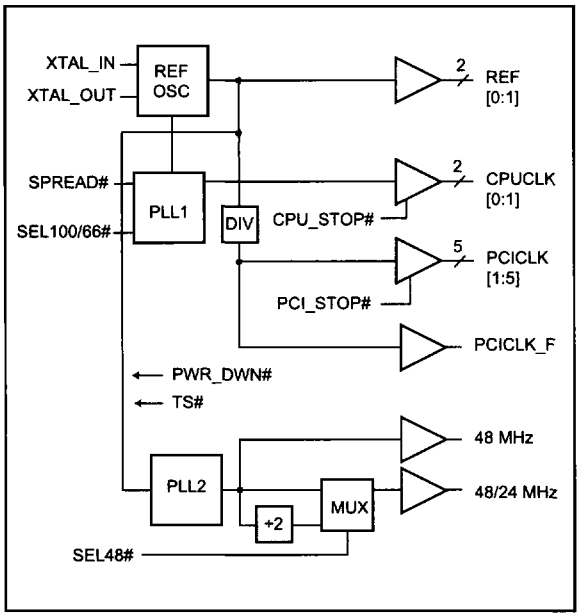
The PI6C103 is a high-speed, low-noise clock generator designed to work with the PI6C18X clock buffer to meet all clock needs for Mobile Intel Architecture platforms. System clock frequencies of 66.6 MHz and 100 MHz are supported.

Split supplies of 3.3V and 2.5V are used. The 3.3V power supply powers everything except the CPU clock. The 2.5V power supply is used to power the CPUCLK outputs. 2.5V signaling follows JEDEC standard 8-X. Power sequencing of the 3.3V and 2.5V supplies is not required.

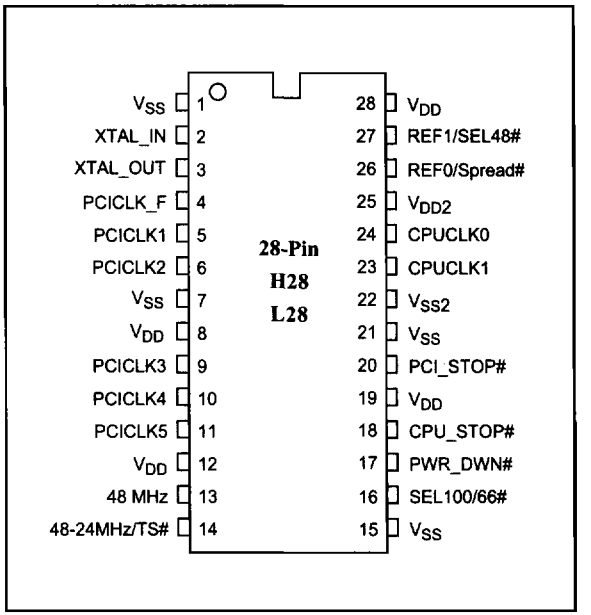
An asynchronous PWR_DWN# signal may be used to orderly power down (or up) the system. CPU and PCI clocks may also be stopped by the CPU_STOP# and PCI_STOP# signals.

The PI6C103 contains the Spread Spectrum function for only those clocks that synchronize to the CPU clocks (CPU and PCI clocks).

Block Diagram



Pin Configuration



Pin Description

28-Pin Package		Type	Symbol	Description
Pin	Qty.			
2	1	Input	XTAL_IN	14.318 MHz crystal input
3	1	Output	XTAL_OUT	14.318 MHz crystal output
4	1	Output	PCICLK_F	3.3V free running PCI clock output
5,6,9,10,11	5	Output	PCICLK[1-5]	3.3V PCI Clock outputs
13	1	Output	48MHz	3.3V 48MHz clock output
14	1	Output	48-24MHz/TS#	3.3V 48 or 24MHz output and Hi-Z state strapping option(2,5) Strap Low = Enter Hi-Z state mode for testing, Strap High = Normal operation
16	1	Input	SEL100/66#	Select for enabling 100 MHz or 66 MHz CPU clock(5) H = 100 MHz, L = 66 MHz
17	1	Input	PWR_DWN#	Device enters power down mode when LOW5
18	1	Input	CPU_STOP#	When Low, stop CPU clocks in LOW state
20	1	Input	PCI_STOP#	When signal LOW, stops all PCI clocks in LOW state except for PCICLK_F output(5)
23,24	2	Output	CPUCLK[1-0]	2.5V CPU clock outputs
26	1	Output	REF0/Spread#	3.3V 14.318 MHz reference clock output and power-on spread spectrum enable strap option(3,5) Strap Low = Spread spectrum clocking enable Strap High = Spread spectrum clocking disable
27	1	Output	REF1/SEL48#	3.3V 14.318 MHz reference clock output and power-on 48/24 MHz select strap option4,5 Pin 14 output = 48 MHz when straped LOW Pin 14 output = 24 MHz when strapped HIGH
8,12,19,28	1	Power	V_{DD}	3.3V Power
1,7,15,21		Power	V_{SS}	3.3V Ground
25	1	Power	V_{DD2}	2.5V Power
22	1	Power	V_{SS2}	2.5V Ground

Notes:

1. V_{DD} and V_{SS} names in the above table reflect a likely internal power and ground partition to reduce the effects of internal noise on the performance of the device. In reality, the platform will be configured with the same voltage V_{DD} pins tied to a common supply and all V_{SS} pins being common. The V_{DD}/V_{SS} naming convention above is done to show how the pinout is dominated by the need to isolate all the signals.
2. The output frequency at this pin is dependent on the power on strapping option at pin 27. A 48 MHz output when power-on strapped LOW, and 24 MHz output when strapped HIGH. This pin also serves as Hi-Z state strapping option during power-on configuration. During power-on, the PI6C103 will sample the value at this pin. Strapped LOW for Hi-Z state mode and HIGH for normal operation.
3. This is a dual function pin. During power-on, all clock outputs are disabled, and the PI6C103 will sample the spread spectrum enable/disable strapping option. After the strapped value latches, all clock outputs will be enabled simultaneously and this pin will become a 14.318 MHz reference clock output. The Power-on latency needs to be less than 3ms after the supply voltage stabilized.
4. This is a dual function pin. During power-on, all clocks are disabled, and PI6C103 will sample the SEL48# strapping option. After the strapped value latches, all clock outputs will be enabled simultaneously and this pin will become another 14.318 MHz reference clock output. The power-on latency needs to be less than 3ms after the supply voltage stabilized.
5. Internally pulled up with resistor min.value of 50kΩ.

Select Functions

SEL100/66#	CPUCLK[0:1]
0	66 MHz
1	100 MHz

Function Description

TS#	Function Description	Outputs				
		CPU	PCI, PCI_ F	REF	48/24M	48M
0	Hi-Z	Hi-Z	Hi-Z	Hi-Z	Hi-Z	Hi-Z
1	Normal	100/66 MHz	33 MHz	14.318 MHz	48/24 MHz	48 MHz

Clock Enable Configuration

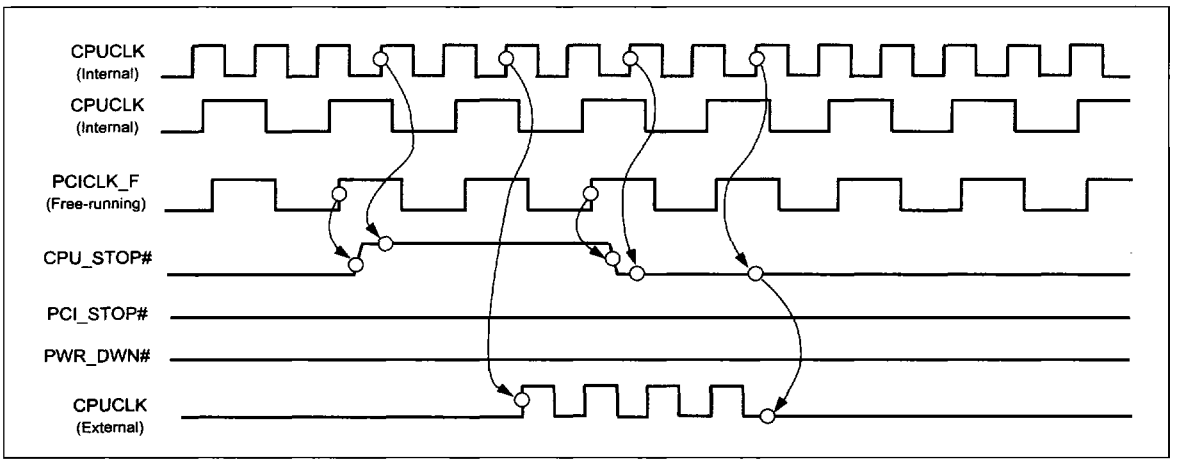
CPU_STOP#	PCI_STOP#	PWR_DWN#	CPUCLK [0:1]	PCICLK [1:5]	PCICLK_F	Other Clocks	Crystal	VCO's	48MHz
X	X	0	low	low	low	stopped	off	off	off
0	0	1	low	low	33 MHz	running	running	running	running
0	1	1	low	33 MHz	33 MHz	running	running	running	running
1	0	1	100/66 MHz	low	33 MHz	running	running	running	running
1	1	1	100/66 MHz	33 MHz	33 MHz	running	running	running	running

Power Management Timing

Signal	Signal State	Latency
		No. of rising edges of free running PCICLK
CPU_STOP#	0 (disabled)	1
	1 (enabled)	1
PCI_STOP#	0 (disabled)	1
	1 (enabled)	1
PWR_DWN#	1 (normal operation)	3ms
	0 (power down)	2 max.

Notes:
1. Clock on/off latency is defined as the number of rising edges of free running PCICLKs between when the clock disable goes low/high to when the first valid clock comes out of the device.
2. Power-up latency is from when PWR_DWN# goes inactive (HIGH) to when the first valid clocks are driven from the device.

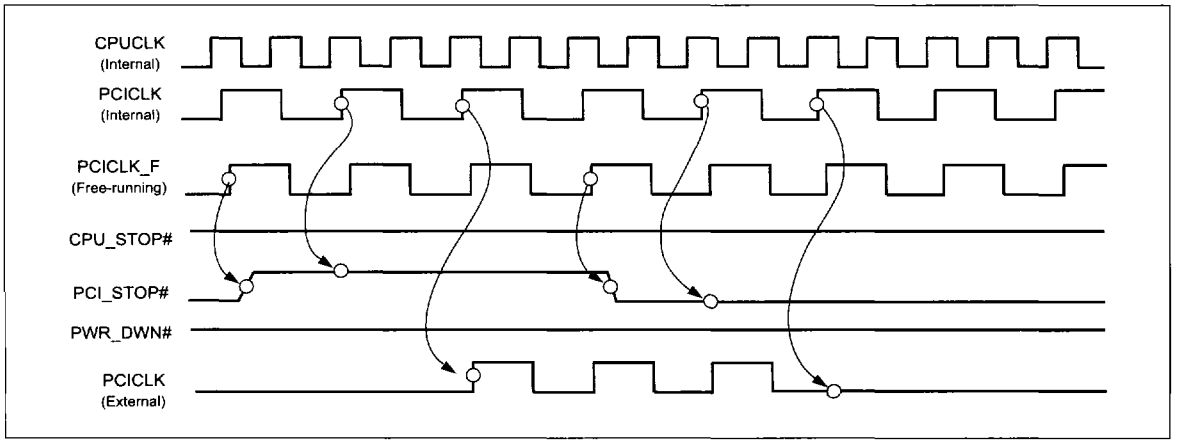
CPU_STOP# is an input signal used to turn off the CPU clocks for low power operation. CPU_STOP# is asserted asynchronously by the external clock control logic with the rising edge of free running PCI clock and is internally synchronized to the external PCICLK_Foutput. All other clocks continue to run while the CPU clocks are disabled. The CPU clocks are always stopped in a low state and started guaranteeing that the high pulse width is a full pulse. CPU clock on latency is 2 or 3 CPU clocks and CPU clock off latency is 2 or 3 CPU clocks.



CPU_STOP# Timing Diagram

Notes:
1. All timing is referenced to the CPUCLK.
2. The Internal label means inside the chip and is a reference only. This in fact may not be the way that the control is designed.
3 CPU_STOP# is an input signal that must be made synchronous to the free running PCI_F.
4. ON/OFF latency shown in the diagram is 2 CPU clocks.
5. All other clocks continue to run undisturbed.
6. PWR_DWN# , PCI_STOP# are shown in a high state.
7. Diagrams shown with respect to 66 MHz. Similar operation as CPU = 100 MHz.

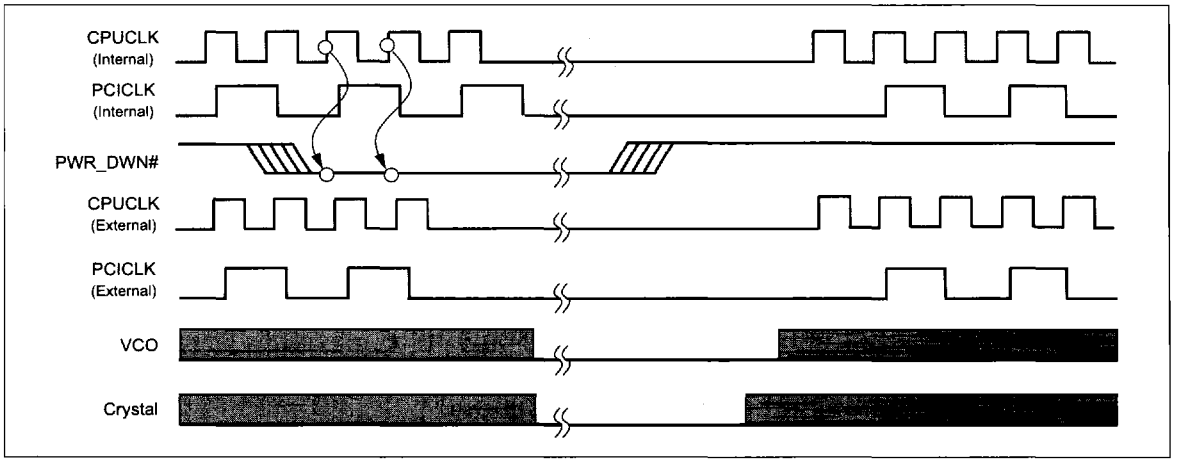
PCI_STOP# is an input signal used to turn off PCI clocks for low power operation. PCI clocks are stopped in the low state and started with a guaranteed full high pulse width. There is ONLY one rising edge of external PCICLK after the clock control logic.



PCI_STOP# Timing Diagram

Notes:
1. All timing is referenced to the CPUCLK.
2. PCI_STOP# signal is an input signal which must be made synchronous to PCI_F output.
3 Internal means inside the chip.
4. All other clocks continiue to run undisturbed.
5. PWR_DWN# CPU_STOP# are shown in a high state.
6. Diagrams shown with respect to 66 MHz. Similar operation as CPU = 100 MHz.

The PWR_DWN# is used to place the device in a very low power state. PWR_DWN# is an asynchronous active low input. Internal clocks are stopped after the device is put in power-down mode. The power-on latency is less than 3ms. PCI_STOP# and CPU_STOP# are "don't cares" during the power-down operations. The REF clock is stopped in the LOW state as soon as possible.



PWR_DWN# Timing Diagram

Notes:
1. All timing is referenced to the CPUCLK.
2. The Internal label means inside the chip and is a reference only.
3. PWR_DWN# is an asynchronous input and metastable conditions could exist. The signal is synchronized inside the part.
4. The Shaded sections on the VCO and the Crystal signals indicate an active clock.
5. Diagrams shown wth respect to 66 MHz. Similar operations as CPU = 100 MHz.

Maximum Ratings

(Above which the useful life may be impaired. For user guidelines, not tested.)

Storage Temperature	–65°C to +150°C
Ambient Temperature with Power Applied	–0°C to +70°C
3.3V Supply Voltage to Ground Potential	–0.5V to +4.6V
2.5V Supply Voltage to Ground Potential	–0.5V to +3.6V
DC Input Voltage	–0.5V to +4.6V

Note:

Stresses greater than those listed under MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

DC Electrical Characteristics

(V_{DDQ3} = +3.3V ± 5%, V_{DDQ2} = +2.5V ± 5%, T_A = 0°C to +70°C)

PI6C102-16 Condition	**Max. 2.5V Supply Consumption Max. discrete cap loads, V_{DDQ2} = 2.625V All static inputs = V_{DDQ3} or V_{SS}**	**Max. 3.3V Supply Consumption Max. discrete cap loads, V_{DDQ3} = 3.465V All static inputs = V_{DDQ3} or V_{SS}**
Powerdown Mode (PWRDWN# =0)	100µA	500µA
Active 66 MHz SEL 100/66# = 0	72mA	170mA
Active 100 MHz SEL 100/66# = 1	100mA	170mA

DC Operating Specifications

Symbol	Parameters	Conditions	Min.	Max.	Units
V_{DD} = 3.3V ± 5%					
V_{IH}	Input high voltage	V_{DD}	2.0	V_{DD} +0.3	V
V_{IL}	Input low voltage		V_{SS} -0.3	0.8	
I_{IL}	Input leakage current	$0 < V_{IN} < V_{DD}$	-5	+5	
V_{DD} = 2.5V ± 5%					
V_{OH}	Output high voltage	I_{OH} = -1mA	2.0		V
V_{OL}	Output low voltage	I_{OL} = 1mA		0.4	
V_{DD} = 3.3V ± 5%					
V_{OH}	Output high voltage	I_{OH} = -1mA	2.0		V
V_{OL}	Output low voltage	I_{OL} = 1mA		0.4	
V_{DD} = 3.3V ± 5%					
V_{POH}	PCI Bus output high voltage	I_{OH} = -1mA	2.4		V
V_{POL}	PCI Bus output low voltage	I_{OL} = 1mA		0.55	
C_{IN}	Input pin capacitance			5	pF
C_{XTAL}	Xtal pins capacitance		13.0	22.5	
C_{OUT}	Output pin capacitance			6	
L_{PIN}	Pin Inductance			7	nH
T_A	Ambient Temperature	No airflow	0	70	°C

Buffer Specifications

Buffer Name	V_{DD} Range(V)	Impedance (Ω)	Buffer Type
CPU	2.375 -2.625	6.8 ~ 17.3	Type 1
REF, 48/24 MHz	3.135 - 3.465	20 - 60	Type 3
PCI/REF	3.135 - 3.465	12 - 55	Type 5

Type 1: CPU Clock Buffers (2.5V)

Symbol	Parameters	Conditions	Min.	Typ.	Max.	Units
I_{OHMIN}	Pull-up current	V_{OUT} = 1.0V	-78			mA
I_{OHMAX}	Pull-up current	V_{OUT} = 2.375V			-67	
I_{OLMIN}	Pull-down current	V_{OUT} = 1.2V	81			
I_{OLMAX}	Pull-down current	V_{OUT} = 0.3V			60	
t_{RH}	2.5V Type 1 output rise edge rate	2.5V ± 5% @ 0.4V-2.0V	1		4	V/ns
t_{FH}	2.5V Type 1 output fall edge rate	2.5V ± 5% @ 2.0V-0.4V	1		4	

Type 3: REF Buffers (3.3V)

Symbol	Parameters	Conditions	Min.	Typ.	Max.	Units
I_{OHMIN}	Pull-up current	V_{OUT} = 1.0V	-29			mA
I_{OHMAX}	Pull-up current	V_{OUT} = 2.375V			-23	
I_{OLMIN}	Pull-down current	V_{OUT} = 1.2V	29			
I_{OLMAX}	Pull-down current	V_{OUT} = 0.3V			27	
t_{RH}	3.3V Type 3 output rise edge rate	3.3V ± 5% @ 0.4V-2.4V	0.5		2	V/ns
t_{FH}	3.3V Type 3 output fall edge rate	3.3V ± 5% @ 2.4V-0.4V	0.5		2	

Type 5: PCI Clock Buffers (3.3V)

Symbol	Parameters	Conditions	Min.	Typ.	Max.	Units
I_{OHMIN}	Pull-up current	V_{OUT} = 1.0V	-33			mA
I_{OHMAX}	Pull-up current	V_{OUT} = 3.135V			-33	
I_{OLMIN}	Pull-down current	V_{OUT} = 1.95V	30			
I_{OLMAX}	Pull-down current	V_{OUT} = 0.4V			38	
t_{RH}	3.3V Type 5 output rise edge rate	3.3V ± 5% @ 0.4V-2.4V	1		4	V/ns
t_{FH}	3.3V Type 5 output fall edge rate	3.3V ± 5% @ 2.4V-0.4V	1		4	

AC Timing

Figure 1. Host Clock to PCI CLK Offset	Parameters	66 MHz		100 MHz		Units
		Min.	Max.	Min.	Max.	
t_{HKP} (2.5V)	Host CLK period	15.0	15.5	10.0	10.5	ns
t_{HKH} (2.5V)	Host CLK high time	5.2		3.0		
t_{HKL} (2.5V)	Host CLK low time	5.0		2.8		
t_{HRISE} (2.5V)	Host CLK rise time	0.4	1.6	0.4	1.6	
t_{HFALL} (2.5V)	Host CLK fall time	0.4	1.6	0.4	1.6	
t_{JITTER} (2.5V)	Host CLK Jitter		250		250	ps
Duty Cycle (2.5V)	Measured at 1.25V	45	55	45	55	%
t_{HSKW} (2.5V)	Host Bus CLK Skew		175		175	ps
t_{PZL}, t_{PZH}	Output enable delay	1.0	8.0	1.0	8.0	ns
t_{PLZ}, t_{PHZ}	Output disable delay	1.0	8.0	1.0	8.0	
t_{HSTB}	Host CLK Stabilization from power-up		3		3	ms
t_{PKP}	PCI CLK period	30.0	∝	30.0	∝	ns
t_{PKPS}	PCI CLK period stability		500		500	ps
t_{PKH}	PCI CLK high time	12.0		12.0		ns
t_{PKL}	PCI CLK low time	12.0		12.0		
t_{PSKW}	PCI Bus CLK Skew		500		500	ps
$t_{HPOFFSET}$	Host to PCI Clock Offset	1.5	4.0	1.5	4.0	ns
t_{PSTB}	PCI CLK Stabilization from power-up		3		3	ms

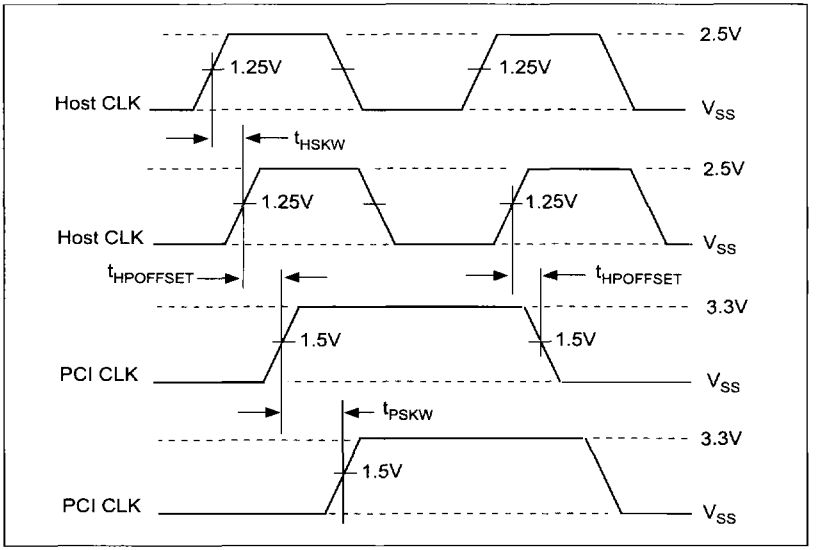


Figure 1. Host Clock and PCI CLK Timing

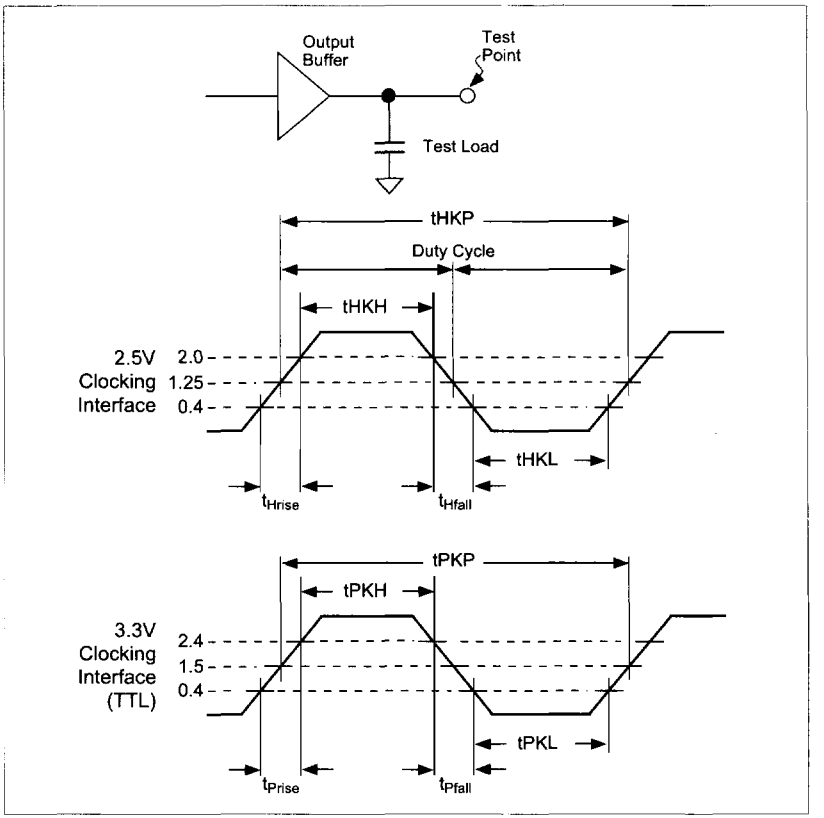
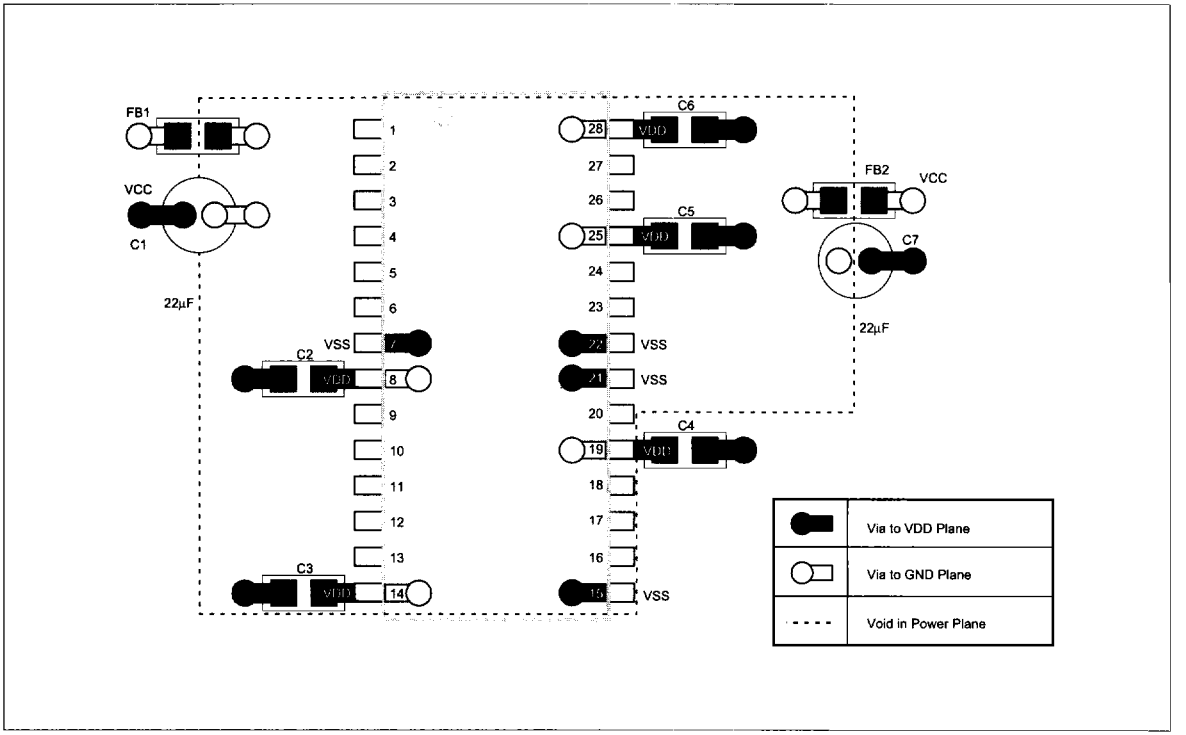


Figure 2. Clock Output Waveforms

PCB Layout Suggestion



Note:

This is only a suggested layout. There may be alternate solutions depending on actual PCB design and layout.

As a general rule, C2-C6 should be placed as close as possible to their respective V_{DD}.

Recommended capacitor values:

C2-C6 ..... 0.1µF, ceramic

C1, C7 ..... 22µF

Minimum and Maximum Expected Capacitive Loads

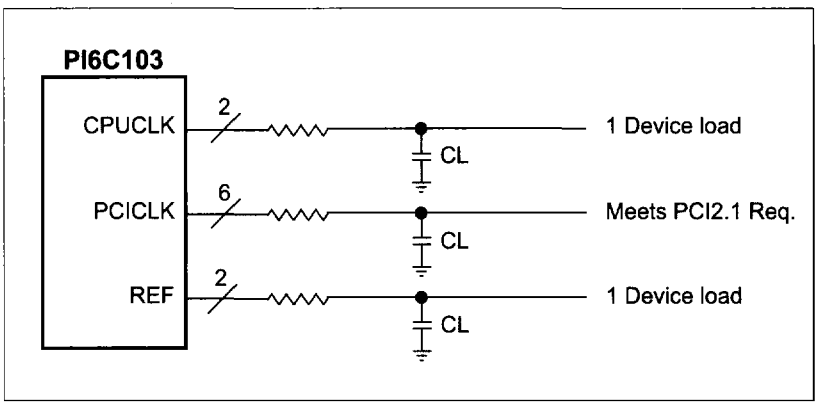
Clock	Min. Load	Max. Load	Units	Notes
CPU Clocks (HCLK)	10	20	pF	1 device load, possible 2 loads
PCI Clocks (PCLK)	30	30		Meets PCI 2.1 requirements
REF, 48MHz	10	20		1 device load

Notes:

1. Maximum rise/fall times are guaranteed at maximum specified load for each type of output buffer.
2. Minimum rise/fall times are guaranteed at minimum specified load for each type of output buffer.
3. Rise/fall times are specified with pure capacitive load as shown. Testing is done with an additional 500Ω resistor in parallel.

Design Guidelines to Reduce EMI

1. Place series resistors and CI capacitors as close as possible to the respective clock pins. Typical value for CI is 10pF. Series resistor value can be increased to reduce EMI provided that the rise and fall time are still within the specified values.
2. Minimize the number of "vias" of the clock traces.
3. Route clock traces over a continuous ground plane or over a continuous power plane. Avoid routing clock traces from plane to plane (refer to rule #2).
4. Position clock signals away from signals that go to any cables or any external connectors.



Ordering Information

P/N	Description
PI6C103H	28-pin SSOP Package
PI6C103-xxL	28-pin TSSOP Package