

# MC145445

**CMOS**

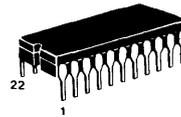
**300 BAUD  
 FSK MODEM**

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### 0-300 BAUD FSK MODEM

The MC145445 is a silicon-gate CMOS frequency shift keying (FSK) modem intended for use in Bell 103/113 and CCITT V. 21 applications. Features of the device include:

- Bell 103/113 Answer and Originate Compatible, 0-300 Baud
- CCITT V. 21 Modes 1 and 2 Compatible, 0-300 Baud
- Eight Selectable RTS to CTS Delay Options
- Answer-Back Tone Generator (U.S. and CCITT Tones)
- Carrier Detect Input
- TTL Compatible
- 22 Pin Package
- Compatible to the MC145440 Bell 103 or MC145441 CCITT V. 21 Modem Filter

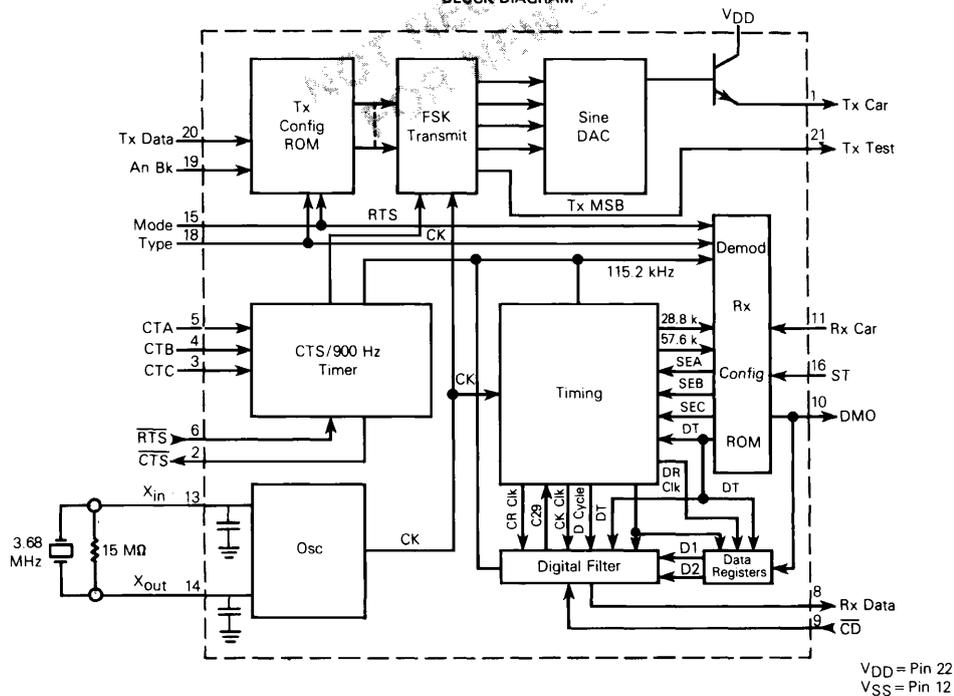


**L SUFFIX**  
 CERAMIC PACKAGE  
 CASE 736



**P SUFFIX**  
 PLASTIC PACKAGE  
 CASE 708

**MC145445 300 BAUD FSK MODEM  
 BLOCK DIAGRAM**



## ABSOLUTE MAXIMUM RATINGS

Rating	Symbol	Value	Unit
DC Supply Voltage	$V_{DD}$	10	V
Input Voltages, All Inputs	$V_{in}$	$V_{SS} - 0.5$ to $V_{DD} + 0.5$	V
DC Current Drain per Pin Pin 3-6, 9, 15, 16, 18, 19, 20 Pins 2, 8	$I_{out}$	10 35	mA
Operating Temperature Range	$T_A$	0 to +70	°C
Storage Temperature Range	$T_{stg}$	-55 to +150	°C

## RECOMMENDED OPERATING CONDITIONS

Parameter	Symbol	Min	Typ	Max	Unit
DC Supply Voltage	$V_{DD} - V_{SS}$	4.5	5.0	6.5	V

## PIN ASSIGNMENTS

Tx Car	1	22	$V_{DD}$
$\overline{CTS}$	2	21	Tx Test
CTC	3	20	Tx Data
CTB	4	19	An Bk
CTA	5	18	Type
RTS	6	17	N.C.
N.C.	7	16	ST
Rx Data	8	15	Mode
$\overline{CD}$	9	14	$X_{out}$
DMO	10	13	$X_{in}$
Rx Car	11	12	$V_{SS}$

DC ELECTRICAL CHARACTERISTICS ( $V_{DD} = 5.0 \text{ V} \pm 5\%$ ,  $V_{SS} = 0$ ,  $0^\circ\text{C} \leq T_A \leq 70^\circ\text{C}$ )

Characteristics	Symbol	Min	Typ	Max	Unit
Input High Voltage Pins 3-6, 9, 15, 16, 18, 19, 20 Pin 13, 11	$V_{IH}$	— 2.8 4.0	— — —	— — —	V
Input Low Voltage Pin 3-6, 9, 15, 16, 18, 19, 20 Pin 13, 11	$V_{IL}$	— — —	— — —	— 0.5 0.6	V
Input Current All Inputs ( $V_{IL} = 0 \text{ V}$ ) All Inputs Except Pins 11, 13, ( $V_{IH} > 2.8 \text{ V}$ ) (Note 1)	$I_{in}$	— — —	— — —	— — -5.0 500	$\mu\text{A}$
Output High Current ( $V_{OH} = 2.4 \text{ V}$ ) Pins 2, 8 (Test Load A) Pins 10, 21 (Test Load B)	$I_{OH}$	— 0.75 0.75	— — —	— — —	mA
Output Low Current ( $V_{OL} = 0.4 \text{ V}$ ) Pins 2, 8 (Test Load A) Pins 10, 21 (Test Load B)	$I_{OL}$	— 1.2 0.6	— — —	— — —	mA
Operating Current	$I_{DD}$	—	2.5	6	mA
Input Capacitance All Except Pin 13 Pin 13 ( $X_{in}$ )	$C_{in}$	— — —	— — 8	— 12 —	pF
Output Capacitance All Except Pin 14 Pin 14 ( $X_{out}$ )	$C_{out}$	— — —	— — 13	— 12 —	pF
Transmit Audio Signal Level (Pin 1 $R_L = 10 \text{ k}\Omega$ ) (Note 2) Total Harmonic Distortion (2nd to 14th) (Note 2)	— THD	0.428 —	0.5 -50	0.578 -40	V <sub>p-p</sub> dB

AC ELECTRICAL CHARACTERISTICS ( $V_{DD} = 5.0 \text{ V} \pm 5\%$ ,  $V_{SS} = 0$ ,  $0^\circ\text{C} \leq T_A \leq 70^\circ\text{C}$ )

Characteristics	Symbol	Min	Typ	Max	Unit
Output Rise Time (Test Load A) (Pins 2, 8)	$t_r$	—	20	100	ns
Output Rise Time (Test Load B) (Pins 10, 14, 21)	$t_r$	—	20	100	ns
Output Fall Time (Test Load A) (Pins 2, 8)	$t_f$	—	20	100	ns
Output Fall Time (Test Load B) (Pins 10, 14, 21)	$t_f$	—	20	100	ns
Input Rise and Fall Times (Except Pin 13)	$t_r, t_f$	—	—	1000	$\mu\text{s}$
Delay From $\overline{RTS}$ to $\overline{CTS}$	$t_d$	—	1	—	$\mu\text{s}$

## NOTES:

- Active pull-up devices are used on these inputs to allow interfacing to TTL devices. The  $I_{in}$  specified is a transitional load (not steady state) which is drawn when the input is brought up to 2.8 V until the internal pull-up device has raised the signal to the  $V_{DD}$  level.
- Measured in any mode using HP-3555B dB meter (or equivalent) with 3 kHz flat filtering.

## PIN DESCRIPTIONS

**V<sub>DD</sub>, POSITIVE POWER SUPPLY (PIN 22)**

This is nominally 5.0 V.

**V<sub>SS</sub>, NEGATIVE POWER SUPPLY (PIN 12)**

This is usually 0 volts.

**Tx Car, TRANSMIT CARRIER (PIN 1)**

The transmit carrier output is a 16 step digitally-synthesized sine wave with an amplitude of  $0.1 V_{DD}$  (p-p) ( $\pm 10\%$ ) and offset by a dc bias of  $0.5 V_{DD}$  ( $\pm 10\%$ ). The output load should be 10 kilohms or greater.

 **$\overline{CTS}$ , CLEAR TO SEND (PIN 2)**

The clear to send output goes low in response to a high-to-low transition of  $\overline{RTS}$  following a selected delay (see CTA, CTB, CTC pin description). This output goes high immediately after loss of  $\overline{RTS}$ . During the time following activation of  $\overline{RTS}$  and before the activation of  $\overline{CTS}$ , Tx Data should be held in the mark condition.

**CTA, CLEAR TO SEND SELECT A (PIN 5)****CTB, CLEAR TO SEND SELECT B (PIN 4)****CTC, CLEAR TO SEND SELECT C (PIN 3)**

For delay times for clear to send delay select inputs, see Table 1.

 **$\overline{RTS}$ , REQUEST TO SEND (PIN 6)**

The request to send input controls data transmission from the modulator. A low level enables the modulator output and a high level will disable the modulator. See Figure 1.

**N.C., NO CONNECTION (PINS 7 AND 17)**

These pins are not bonded internally. They should be left open in normal operation.

**Rx Data, RECEIVE DATA (PIN 8)**

The receive data output is the serial data output from the demodulator. Rx Data is clamped high when  $\overline{CD}$  is not active.

 **$\overline{CD}$ , CARRIER DETECT (PIN 9)**

When carrier detect input is high (1), the Rx Data output will be clamped to a high state. When carrier detect is low (0), Rx Data output demodulates the Rx carrier input signal.

**DMO, DEMODULATOR OUTPUT (PIN 10)**

The demodulator output is the output of the differential delay detector. It is used for production testing of the demodulator. In normal operation, this pin should be left open.

**Rx Car, RECEIVER CARRIER (PIN 11)**

The receiver carrier input is the FSK input to the

demodulator. This signal should be the hard-limited output of the receive filter, nominally 50%.

**X<sub>in</sub>, OSCILLATOR INPUT (PIN 13)****X<sub>out</sub>, OSCILLATOR OUTPUT (PIN 14)**

X<sub>in</sub> should be driven from either an AT-cut crystal or a digital signal source at  $3.6864 \text{ MHz} \pm 0.01\%$ . When driven by a crystal, a 15 megohm resistor should be connected from X<sub>in</sub> to X<sub>out</sub> in parallel with the crystal.

**MODE (PIN 15)**

The mode pin selects the pair of frequencies used during modulation and demodulation. A "0" on this pin selects answer mode when Bell type is selected or channel 2 when CCITT type is selected. A "1" on this pin selects originate mode when Bell type is selected or channel 1 when CCITT type is selected.

**ST, SELF TEST (PIN 16)**

When a high level is placed on this pin, the demodulator is switched to the modulator frequencies (as determined by Mode and Type pins). The modulator should be looped back through the receive filter to the demodulator for self test (echo back). Loopback can be done using a hardwire scheme, or automatically using the internal loopback feature of the filter, such as found on the MC145440/41.

**TYPE (PIN 18)**

This pin is used to select between Bell 103/113 type operation and CCITT V.21 operation. When the type input pin is a "1", Bell operation is selected. When the type input pin is a "0", the CCITT standard is selected.

**An Bk, ANSWER BACK (PIN 19)**

The answer back input causes the answer back tone to be transmitted. The answer back tone is 2025 Hz for the Bell mode and 2100 Hz for the CCITT modes. When a high level is placed on the An Bk input pin, the Tx Car pin will output an answer back tone and  $\overline{CTS}$  will go to a high state, regardless of the state of  $\overline{RTS}$  (see Figure 1).

**Tx Data, TRANSMIT DATA (PIN 20)**

The transmit data input is the serial input to the modulator. A high level causes a mark frequency to be transmitted, a low level causes a space frequency to be transmitted.

**Tx Test, TRANSMIT TEST (PIN 21)**

The transmit test output is a square wave representation of the modulator transmit frequency. It is used for test purposes and should be left open in normal operation.

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FIGURE 1 — An Bk AND RTS-CTS TIMING

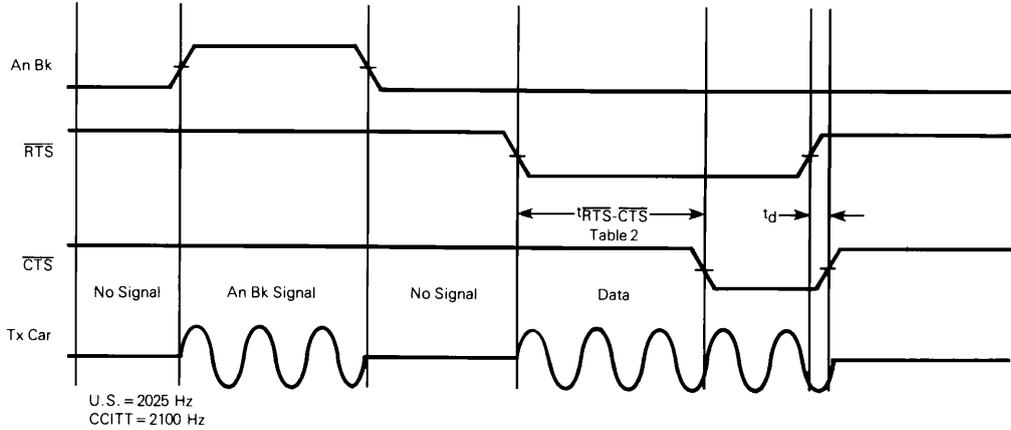


TABLE 1 — RTS-CTS DELAY TIMES

CTC	CTB	CTA	Delay*
0	0	0	0 ms
0	0	1	26.7 ms
0	1	0	40.0 ms
0	1	1	60.0 ms
1	0	0	133.3 ms
1	0	1	213.3 ms
1	1	0	266.7 ms
1	1	1	426.6 ms

\* All delays are  $\pm 1.7$  ms.

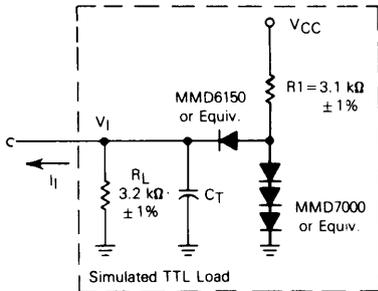
TABLE 2 — OPERATING MODES

Type	Mode	Transmit Data	Transmit Frequency		Application
			Spec	Actual	
0	0	0	1850	1850.6	CCITT V. 21 0-300 Baud, Channel 2
		1	1650	1650.13	
0	1	0	1180	1180.03	CCITT V.21 0-300 Baud, Channel 1
		1	980	979.9	
1	0	0	2025	2025.5	Bell 103 0-300 Baud, Answer Mode
		1	2225	2226.09	
1	1	0	1070	1069.76	Bell 103 0-300 Baud, Originate Mode
		1	1270	1270.3	

Data = 0 = Space  
= 1 = Mark

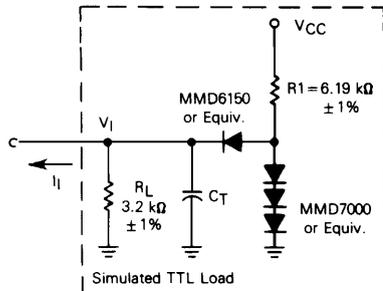
Crystal Frequency = 3.6864 MHz

FIGURE 2 — OUTPUT TEST LOAD A



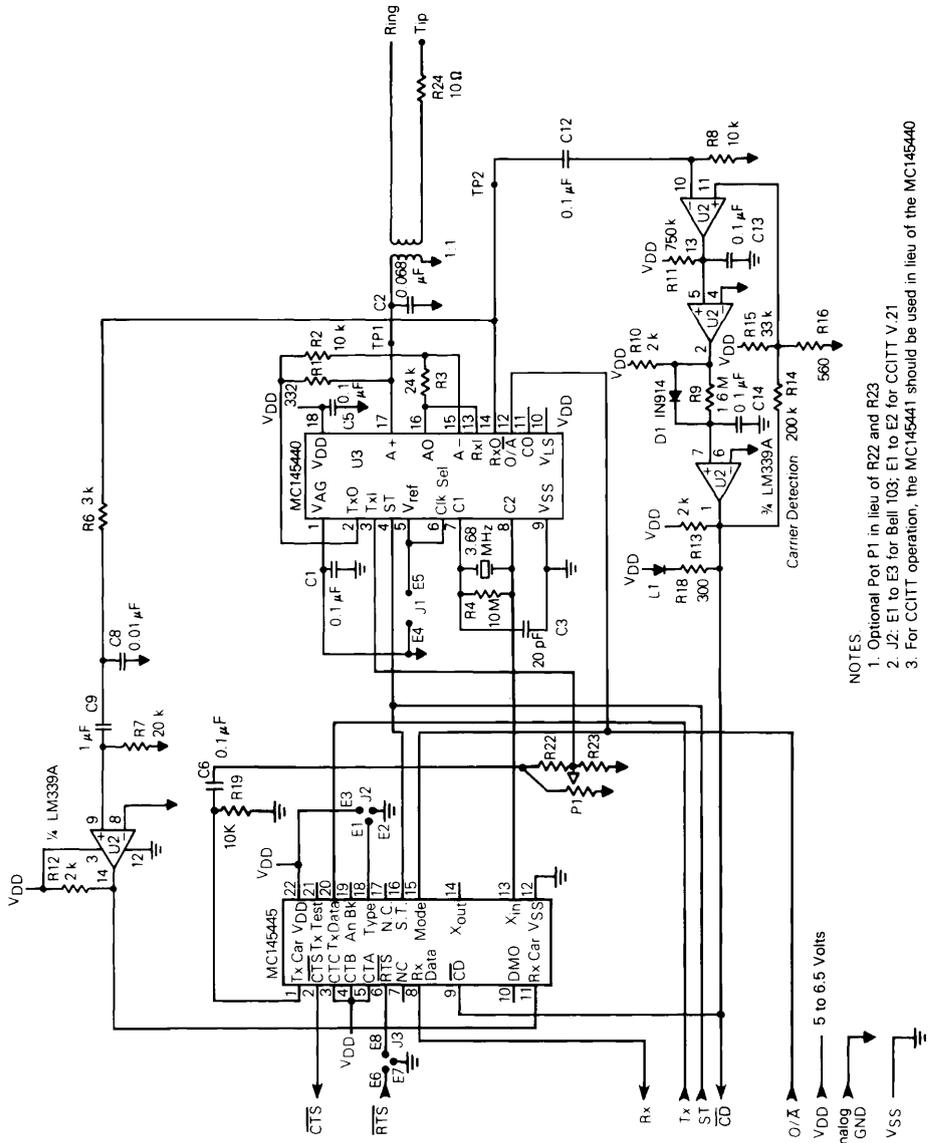
$C_T = 20$  pF = total parasitic capacitance, which includes probe, wiring, and load capacitances.

FIGURE 3 — OUTPUT TEST LOAD B



$C_T = 20$  pF = total parasitic capacitance, which includes probe, wiring, and load capacitances.

FIGURE 4 - TYPICAL BELL 103/113 ORIGINATE/ANSWER MODEM



- NOTES
1. Optional Pot P1 in lieu of R22 and R23
  2. J2: E1 to E3 for Bell 103; E1 to E2 for CCITT V.21
  3. For CCITT operation, the MC145441 should be used in lieu of the MC145440