

**32K X 36 BURST SRAM**

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**Features**

- 32K x 36 Organization
- 0.5 $\mu$  CMOS Technology
- Supports PowerPC™ Processor Operation
- Single +3.3V  $\pm$  5% Power Supply and Ground
- 5V Tolerant I/O
- LVTTTL I/O Compatible
- Fast  $\overline{OE}$  times: 4, 5, 6ns
- Common I/O
- Registered Addresses, Data Ins and Control Signals
- Asynchronous Output Enable
- Self-Timed Write Operation and Byte Write Capability
- Low Power Dissipation
  - 960 mW Active at 66MHz
  - 90 mW Standby
- 100 Pin Thin Quad Flat Pack

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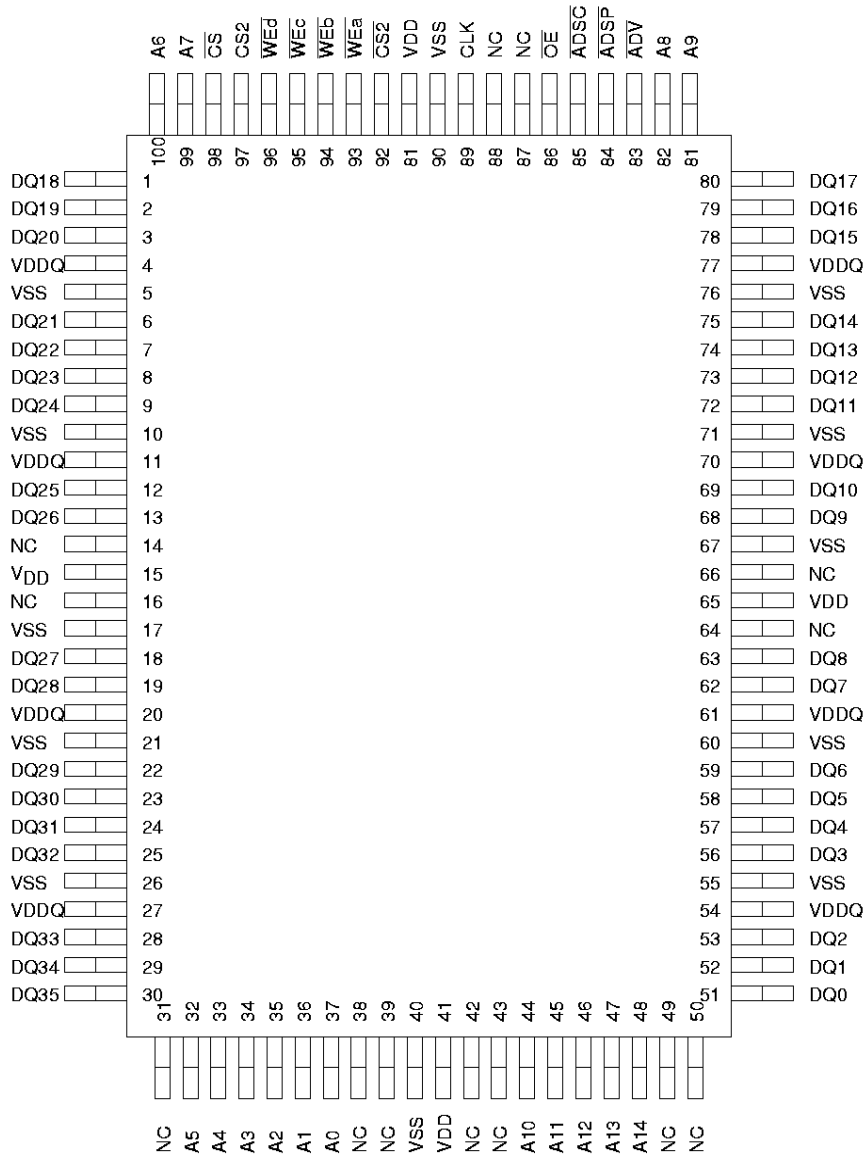
**Description**

IBM Microelectronics 1M SRAM is a Synchronous Burstable, high performance CMOS Static RAM that is versatile, wide I/O, and achieves 8 nsec access. A single clock is used to initiate the read/write operation and all internal operations are self-timed. At the rising edge of the Clock, all Addresses, Data Ins and Control Signals are registered internally. Burst mode operation, is accomplished by integrating input registers, internal 2-bit burst counter and high speed SRAM in a single chip. Burst reads are initiated with either  $\overline{ADSP}$  or  $\overline{ADSC}$  being LOW with a valid address during the rising edge of clock. Data from this address plus the three subsequent addresses will be output. The chip is operated with a single +3.3 V power supply and is compatible with LVTTTL I/O interfaces.



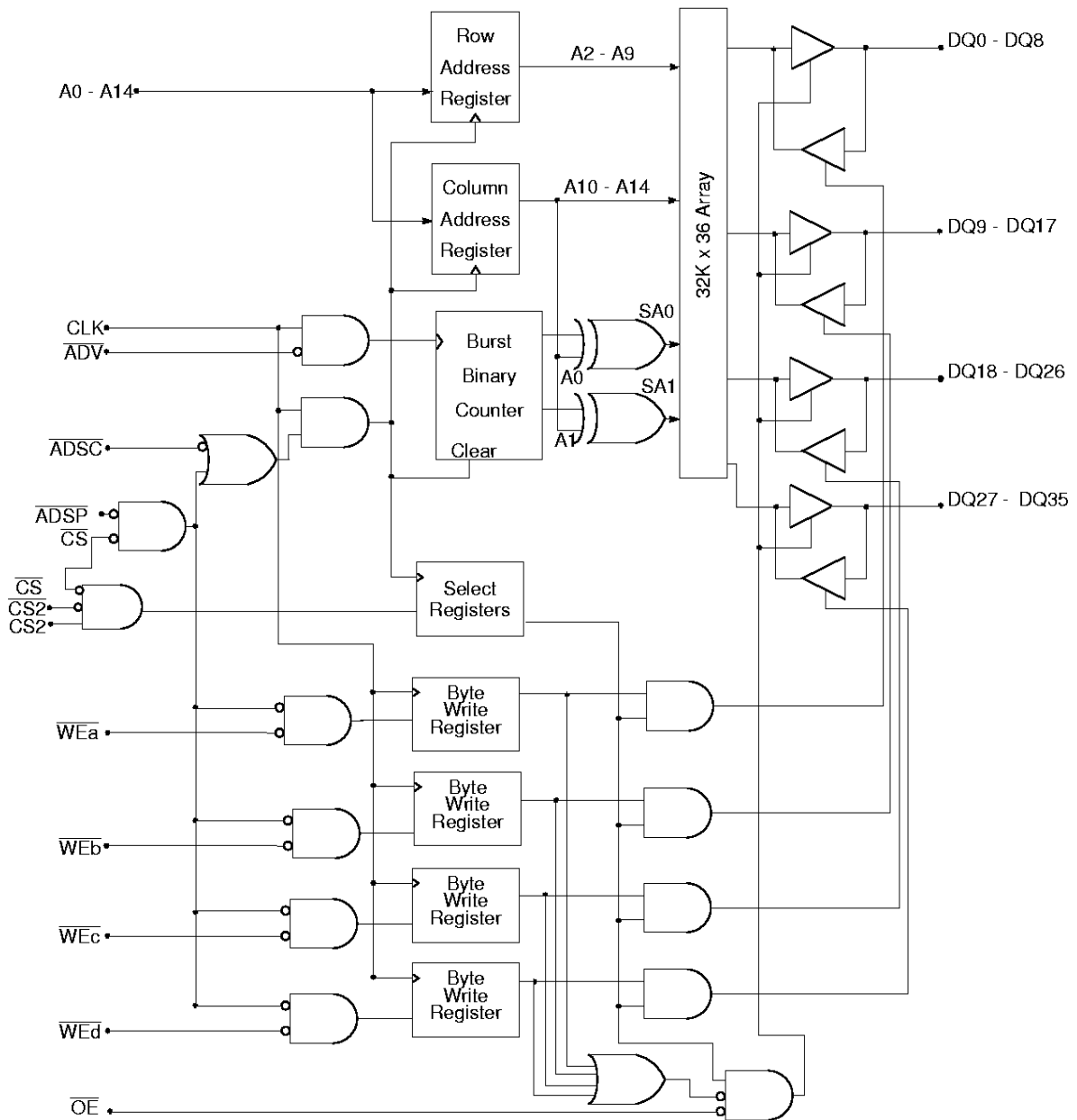
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**X36 TQFP Pin Array Layout**



**Pin Description**

|           |  |                  |                             |
|-----------|--|------------------|-----------------------------|
| A0-A14    | Address input                            | ADSP             | Address Status Processor    |
| DQa - DQd | Data Input/Output (0-8,9-17,18-26,27-35) | ADSC             | Address Status Controller   |
| CLK       | Clock                                    | ADV              | Burst Advance Control       |
| WEa       | Write Enable, Byte a (0 to 8)            | CS               | ADSP Gated Chip Select      |
| WEb       | Write Enable, Byte b (9 to 17)           | V <sub>DD</sub>  | Power Supply (+3.3V)        |
| WEc       | Write Enable, Byte c (18 to 26)          | V <sub>SS</sub>  | Ground                      |
| WEd       | Write Enable, Byte d (27 to 35)          | V <sub>DDQ</sub> | Output Power Supply (+3.3V) |
| OE        | Output Enable                            | NC               | No Connect                  |
| CS2, CS2  | Chip Selects                             |                  |                             |

**Block Diagram**

**Ordering Information**

| Part Number     | Organization | Speed                      | Leads        | Notes |
|-----------------|--------------|----------------------------|--------------|-------|
| IBM043614PQK-8  | 32K x 36     | 8 ns Access / 15 ns Cycle  | 100 pin TQFP |       |
| IBM043614PQK-9  | 32K x 36     | 9 ns Access / 15 ns Cycle  | 100 pin TQFP |       |
| IBM043614PQK-10 | 32K x 36     | 10 ns Access / 15 ns Cycle | 100 pin TQFP |       |
| IBM043614PQK-11 | 32K x 36     | 11 ns Access / 15 ns Cycle | 100 pin TQFP |       |



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**Burst SRAM Clock Truth Table**

| CLK | $\overline{CS}2$ | CS2 | $\overline{CS}$ | ADSP | ADSC | ADV | WE | $\overline{OE}$ | DQ     | Operation                               |
|-----|------------------|-----|-----------------|------|------|-----|----|-----------------|--------|---|
| L→H | H                | X   | L               | L    | X    | X   | X  | X               | High-Z | Deselected Cycle                        |
| L→H | X                | L   | L               | L    | X    | X   | X  | X               | High-Z | Deselected Cycle                        |
| L→H | H                | X   | X               | X    | L    | X   | X  | X               | High-Z | Deselected Cycle                        |
| L→H | X                | L   | X               | X    | L    | X   | X  | X               | High-Z | Deselected Cycle                        |
| L→H | L                | H   | L               | L    | X    | X   | X  | L               | Q      | Read from External Address, Begin Burst |
| L→H | L                | H   | L               | L    | X    | X   | X  | H               | High-Z | Read from External Address, Begin Burst |
| L→H | L                | H   | L               | H    | L    | X   | H  | L               | Q      | Read from External Address, Begin Burst |
| L→H | L                | H   | L               | H    | L    | X   | L  | X               | D      | Write to External Address, Begin Burst  |
| L→H | X                | X   | X               | H    | H    | L   | H  | L               | Q      | Read from next Add., Continue Burst     |
| L→H | X                | X   | X               | H    | H    | L   | L  | X               | D      | Write to next Add., Continue Burst      |
| L→H | X                | X   | X               | H    | H    | H   | H  | L               | Q      | Read from Current Add., Suspend Burst   |
| L→H | X                | X   | X               | H    | H    | H   | L  | X               | D      | Write to Current Add., Suspend Burst    |
| L→H | X                | X   | H               | X    | L    | X   | X  | X               | High-Z | Deselect Cycle                          |
| L→H | X                | X   | H               | X    | H    | L   | H  | L               | Q      | Read from next Add., Continue Burst     |
| L→H | X                | X   | H               | X    | H    | L   | L  | X               | D      | Write to next Add., Continue Burst      |
| L→H | X                | X   | H               | X    | H    | H   | H  | L               | Q      | Read from current Add., Suspend Burst   |
| L→H | X                | X   | H               | X    | H    | H   | L  | X               | D      | Write to current Add., Suspend Burst    |

1. For a write operation preceded by a read cycle,  $\overline{OE}$  must be HIGH early enough to allow Input Data Setup, and must be kept HIGH through Input Data Hold Time.
2.  $\overline{WE}$  refers to  $\overline{WEa}$ ,  $\overline{WEb}$ ,  $\overline{WEc}$ ,  $\overline{WEd}$ .
3. ADSP is gated by  $\overline{CS}$ , and  $\overline{CS}$  is used to block ADSP when  $\overline{CS} = V_{IH}$ , as required in applications using Processor Address Pipelining.
4. All Addresses, Data In and Control signals are registered on the rising edge of CLK.

**Burst Sequence Truth Table**

| External Address | A14-A2 | (A1,A0) |       |       |       | Notes |
|------------------|--------|---------|-------|-------|-------|-------|
|                  |        | (0,0)   | (0,1) | (1,0) | (1,1) |       |
| 1st Access       | A14-A2 | (0,0)   | (0,1) | (1,0) | (1,1) |       |
| 2nd Access       | A14-A2 | (0,1)   | (1,0) | (1,1) | (0,0) |       |
| 3rd Access       | A14-A2 | (1,0)   | (1,1) | (0,0) | (0,1) |       |
| 4th Access       | A14-A2 | (1,1)   | (0,0) | (0,1) | (1,0) |       |

### Write Enable Truth Table

| $\overline{WEa}$ | $\overline{WEb}$ | $\overline{WEc}$ | $\overline{WEd}$ | Byte Written                           | Notes |
|------------------|------------------|------------------|------------------|--|-------|
| H                | H                | H                | H                | Read All Bytes                         |       |
| L                | L                | L                | L                | Write All Bytes                        |       |
| L                | H                | H                | H                | Write Byte A (D <sub>IN</sub> 0 - 8)   |       |
| H                | L                | H                | H                | Write Byte B (D <sub>IN</sub> 9 - 17)  |       |
| H                | H                | L                | H                | Write Byte C (D <sub>IN</sub> 18 - 26) |       |
| H                | H                | H                | L                | Write Byte D (D <sub>IN</sub> 27 - 35) |       |

### Absolute Maximum Ratings

| Parameter                    | Symbol           | Rating                       | Units | Notes |
|------------------------------|------------------|------------------------------|-------|-------|
| Power Supply Voltage         | V <sub>DD</sub>  | -0.5 to 4.6                  | V     | 1     |
| Input Voltage                | V <sub>IN</sub>  | -0.5 to 6.0                  | V     | 1     |
| Output Voltage               | V <sub>OUT</sub> | -0.5 to V <sub>DD</sub> +0.5 | V     | 1     |
| Operating Temperature        | T <sub>OPR</sub> | 0 to +70                     | °C    | 1     |
| Storage Temperature          | T <sub>STG</sub> | -55 to +125                  | °C    | 1     |
| Power Dissipation            | P <sub>D</sub>   | 2.0                          | W     | 1     |
| Short Circuit Output Current | I <sub>OUT</sub> | 50                           | mA    | 1     |

1. Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

### Recommended DC Operating Conditions (T<sub>A</sub>=0 to 70°C)

| Parameter          | Symbol           | Min.  | Typ. | Max.  | Units | Notes   |
|--------------------|------------------|-------|------|-------|-------|---------|
| Supply Voltage     | V <sub>DD</sub>  | 3.135 | 3.3  | 3.465 | V     | 1, 4    |
| Input High Voltage | V <sub>IH</sub>  | 2.2   | —    | 5.5   | V     | 1, 2, 4 |
| Input Low Voltage  | V <sub>IL</sub>  | -0.3  | —    | 0.8   | V     | 1, 3, 4 |
| Output Current     | I <sub>OUT</sub> | —     | 5    | 8     | mA    | 4       |

1. All voltages referenced to GND. All V<sub>DD(Q)</sub> and V<sub>SS(Q)</sub> pins must be connected.
2. V<sub>IH</sub>(Max)DC = 5.5 V, V<sub>IH</sub>(Max)AC = 6.0 V (pulse width ≤ 4.0ns).
3. V<sub>IL</sub>(Min)DC = -0.3 V, V<sub>IL</sub>(Min)AC = -1.5 V (pulse width ≤ 4.0ns).
4. Input voltage levels are tested to the following DC conditions: 1 microsecond cycle and 200 ns set-up and hold times.

**32K X 36 BURST SRAM****Capacitance** ( $T_A=0$  to  $+70^\circ\text{C}$ ,  $V_{DD}=3.3\text{V} \pm 5\%$ ,  $f=1\text{MHz}$ )

| Parameter                       | Symbol    | Test Condition        | Max | Units | Notes |
|---------------------------------|-----------|-----------------------|-----|-------|-------|
| Input Capacitance               | $C_{IN}$  | $V_{IN} = 0\text{V}$  | 5   | pF    |       |
| Data I/O Capacitance (DQ0-DQ35) | $C_{OUT}$ | $V_{OUT} = 0\text{V}$ | 5   | pF    |       |

**DC Electrical Characteristics** ( $T_A=0$  to  $+70^\circ\text{C}$ ,  $V_{DD}=3.3\text{V} \pm 5\%$ )

| Parameter  | Symbol     | Min. | Max. | Units         | Notes |
|--|------------|------|------|---------------|-------|
| Operating Current<br>Average Power Supply Operating Current<br>( $\overline{OE} = V_{IH}$ , $I_{OUT} = 0$ )  | $I_{DD15}$ | —    | 275  | mA            | 2, 3  |
| Standby Current<br>Power Supply Standby Current<br>( $CS2 = V_{IH}$ or $CS2 = V_{IL}$ or $\overline{CS} = V_{IH}$<br>All other inputs = $V_{IH}$ or $V_{IL}$ , $I_{OUT} = 0$ , Clock @ 66 MHz) | $I_{SB}$   | —    | 25   | mA            | 1, 3  |
| Input Leakage Current<br>Input Leakage Current, any input<br>( $V_{IN} = 0$ & $V_{DD}$ )   | $I_{LI}$   | —    | +1   | $\mu\text{A}$ | 4     |
| Output Leakage Current<br>( $V_{OUT} = 0$ & $V_{DD}$ , $\overline{OE} = V_{IH}$ )  | $I_{LO}$   | —    | +1   | $\mu\text{A}$ |       |
| Output High Level<br>Output "H" Level Voltage ( $I_{OH} = -8\text{mA}$ @ 2.4V)   | $V_{OH}$   | 2.4  | —    | V             |       |
| Output Low Level<br>Output "L" Level Voltage ( $I_{OL} = +8\text{mA}$ @ 0.4V)  | $V_{OL}$   | —    | 0.4  | V             |       |

- $I_{SB}$  = Stand-by Current.
- $I_{DD}$  = Selected Current.
- $I_{OUT}$  = Chip Output Current.
- The input leakage current for 5.5V inputs is 200  $\mu\text{A}$  for Clk, Chip Selects, and Output Enable. Other inputs have 100  $\mu\text{A}$  of leakage current at 5.5V.

**AC Test Conditions** ( $T_A=0$  to  $+70^\circ\text{C}$ ,  $V_{DD}=3.3\text{V} \pm 5\%$ )

| Parameter                               | Symbol   | Conditions | Units | Notes |
|---|----------|------------|-------|-------|
| Input Pulse High Level                  | $V_{IH}$ | 3.0        | V     |       |
| Input Pulse Low Level                   | $V_{IL}$ | 0.0        | V     |       |
| Input Rise Time                         | $T_R$    | 2.0        | ns    |       |
| Input Fall Time                         | $T_F$    | 2.0        | ns    |       |
| Input and Output Timing Reference Level |          | 1.5        | V     |       |
| Output Load Conditions                  |          |            |       | 1     |

- See AC Test Loading figure 1 on page 8.



**AC Characteristics** ( $T_A=0$  to  $+70^\circ\text{C}$ ,  $V_{DD}=3.3\text{V} \pm 5\%$ , Units in nsec)

| Parameter                            | Symbol             | -8   |      | -9   |      | -10  |      | -11  |      | Notes   |
|--------------------------------------|--------------------|------|------|------|------|------|------|------|------|---------|
|                                      |                    | Min. | Max. | Min. | Max. | Min. | Max. | Min. | Max. |         |
| Cycle Time                           | $t_{\text{CYCLE}}$ | 15.0 | —    | 15.0 | —    | 15.0 | —    | 15.0 | —    |         |
| Clock Pulse High                     | $t_{\text{CH}}$    | 3.0  | —    | 3.0  | —    | 3.0  | —    | 3.0  | —    |         |
| Clock Pulse Low                      | $t_{\text{CL}}$    | 3.0  | —    | 3.0  | —    | 3.0  | —    | 3.0  | —    |         |
| Clock to Output Valid                | $t_{\text{CQ}}$    | —    | 8.0  | —    | 9.0  | —    | 10.0 | —    | 11.0 | 3       |
| Address Status Controller Setup Time | $t_{\text{ADSCS}}$ | 2.5  | —    | 2.5  | —    | 2.5  | —    | 2.5  | —    |         |
| Address Status Controller Hold Time  | $t_{\text{ADSCH}}$ | 0.5  | —    | 0.5  | —    | 0.5  | —    | 0.5  | —    |         |
| Address Status Processor Setup Time  | $t_{\text{ADSPS}}$ | 2.5  | —    | 2.5  | —    | 2.5  | —    | 2.5  | —    |         |
| Address Status Processor Hold Time   | $t_{\text{ADSPH}}$ | 0.5  | —    | 0.5  | —    | 0.5  | —    | 0.5  | —    |         |
| Advance Setup Time                   | $t_{\text{ADVS}}$  | 2.5  | —    | 2.5  | —    | 2.5  | —    | 2.5  | —    |         |
| Advance Hold Time                    | $t_{\text{ADVH}}$  | 0.5  | —    | 0.5  | —    | 0.5  | —    | 0.5  | —    |         |
| Address Setup Time                   | $t_{\text{AS}}$    | 2.5  | —    | 2.5  | —    | 2.5  | —    | 2.5  | —    |         |
| Address Hold Time                    | $t_{\text{AH}}$    | 0.5  | —    | 0.5  | —    | 0.5  | —    | 0.5  | —    |         |
| Chip Selects Setup Time              | $t_{\text{CSS}}$   | 2.5  | —    | 2.5  | —    | 2.5  | —    | 2.5  | —    |         |
| Chip Selects Hold Time               | $t_{\text{CSH}}$   | 0.5  | —    | 0.5  | —    | 0.5  | —    | 0.5  | —    |         |
| Write Enables Setup Time             | $t_{\text{WES}}$   | 2.5  | —    | 2.5  | —    | 2.5  | —    | 2.5  | —    |         |
| Write Enables Hold Time              | $t_{\text{WEH}}$   | 0.5  | —    | 0.5  | —    | 0.5  | —    | 0.5  | —    |         |
| Data In Setup Time                   | $t_{\text{DS}}$    | 2.5  | —    | 2.5  | —    | 2.5  | —    | 2.5  | —    |         |
| Data In Hold Time                    | $t_{\text{DH}}$    | 0.5  | —    | 0.5  | —    | 0.5  | —    | 0.5  | —    |         |
| Data Out Hold Time                   | $t_{\text{CQX}}$   | 3.0  | —    | 3.0  | —    | 3.0  | —    | 3.0  | —    | 3       |
| Clock High to Output High-Z          | $t_{\text{CHZ}}$   | —    | 5.0  | —    | 5.0  | —    | 5.5  | —    | 5.5  | 1, 2, 4 |
| Clock High to Output Active          | $t_{\text{CLZ}}$   | 2.5  | —    | 2.5  | —    | 2.5  | —    | 2.5  | —    | 1, 2, 4 |
| Output Enable to High-Z              | $t_{\text{OHZ}}$   | 2.0  | 5.0  | 2.0  | 5.5  | 2.0  | 6.0  | 2.0  | 6.5  | 1, 4    |
| Output Enable to Low-Z               | $t_{\text{OLZ}}$   | 0.25 | —    | 0.25 | —    | 0.25 | —    | 0.25 | —    | 1, 4    |
| Output Enable to Output Valid        | $t_{\text{OQ}}$    | —    | 4.0  | —    | 5.0  | —    | 5.0  | —    | 6.0  | 3       |

1. Transitions are measured  $\pm 200$  mV from steady state voltage.
2. At any given voltage and temperature,  $T_{\text{CHZ}}$  (max) is always less than  $T_{\text{CLZ}}$  (min) for a given device and from device to device. For any read cycle preceded by a write or deselect cycle, the data bus will transition glitch-free from High-Z to new RAM data.
3. See AC Test Loading figure 1 on page 8.
4. See AC Test Loading figure 2 on page 8.

**32K X 36 BURST SRAM**

**AC Test Loading**

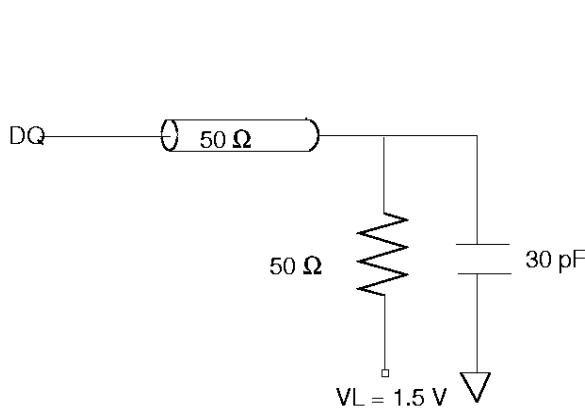


Fig. 1 Test Equivalent Load

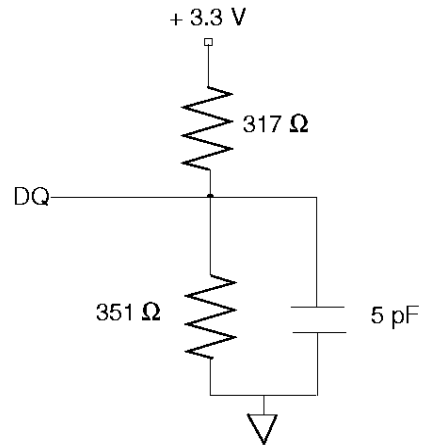
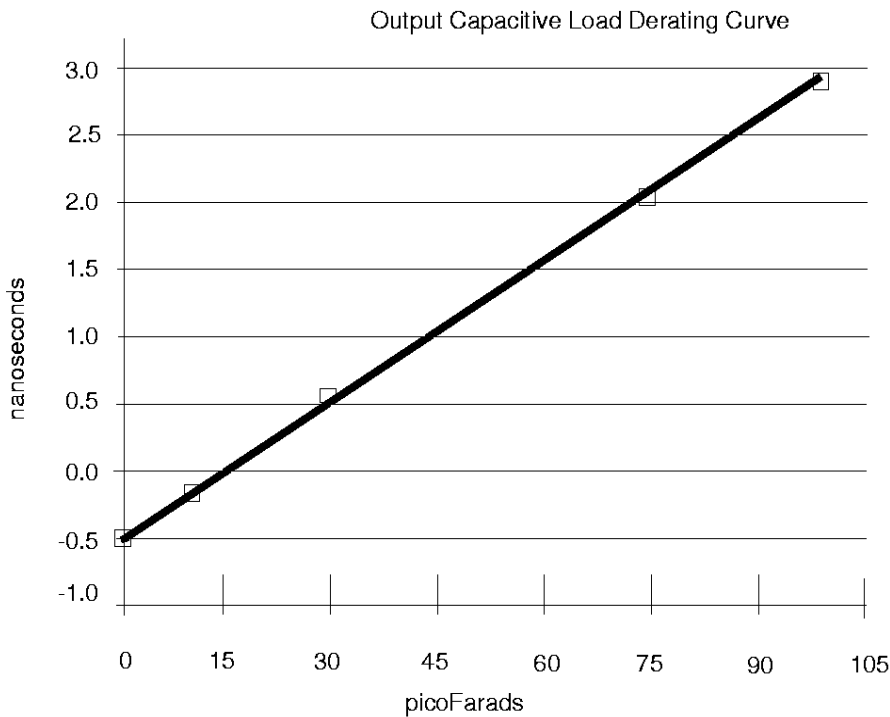
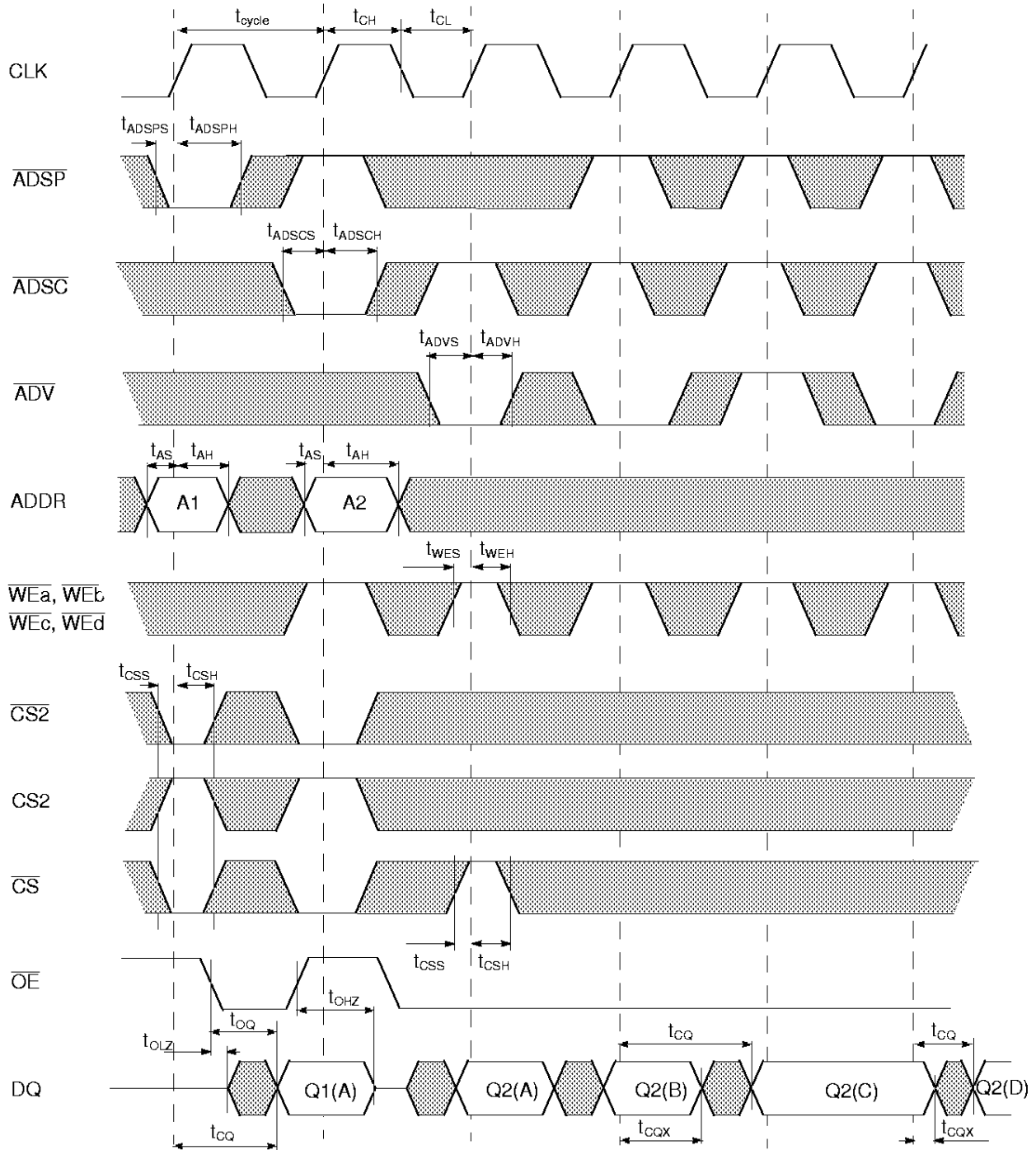


Fig. 2 Test Equivalent Load



The derating curve above is for a purely capacitive load on the output driver. For example, a part specified at 8 ns access time will behave as though it has an 8.5 ns access time if a 30 pF load with no DC component was attached to the output driver. The access times guaranteed in the datasheets are based on a 50 ohm terminated test load. For unterminated loads the derating curve should be used. This curve is based on nominal process conditions with worst case parameters  $V_{DD} = 3.14 \text{ V}$ ,  $T_A = 70^\circ \text{ C}$ .

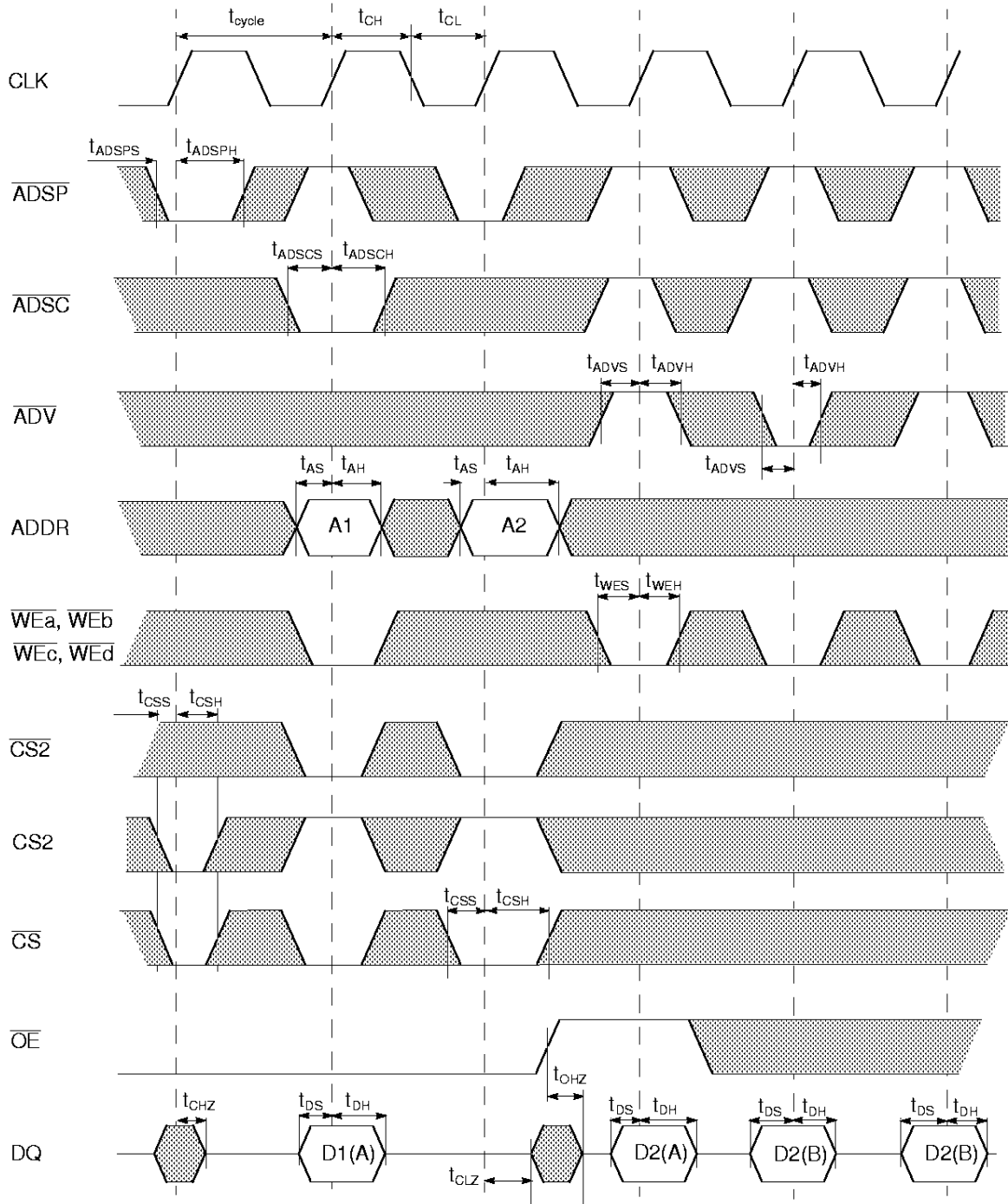


**Timing Diagram (Burst Read)**

**Notes:**

1. Q1(A) and Q2(A) refer to data read from address A1 and A2.
2. Q2(B), Q2(C) and Q2(D) refer to read from subsequent internal burst counter addresses.

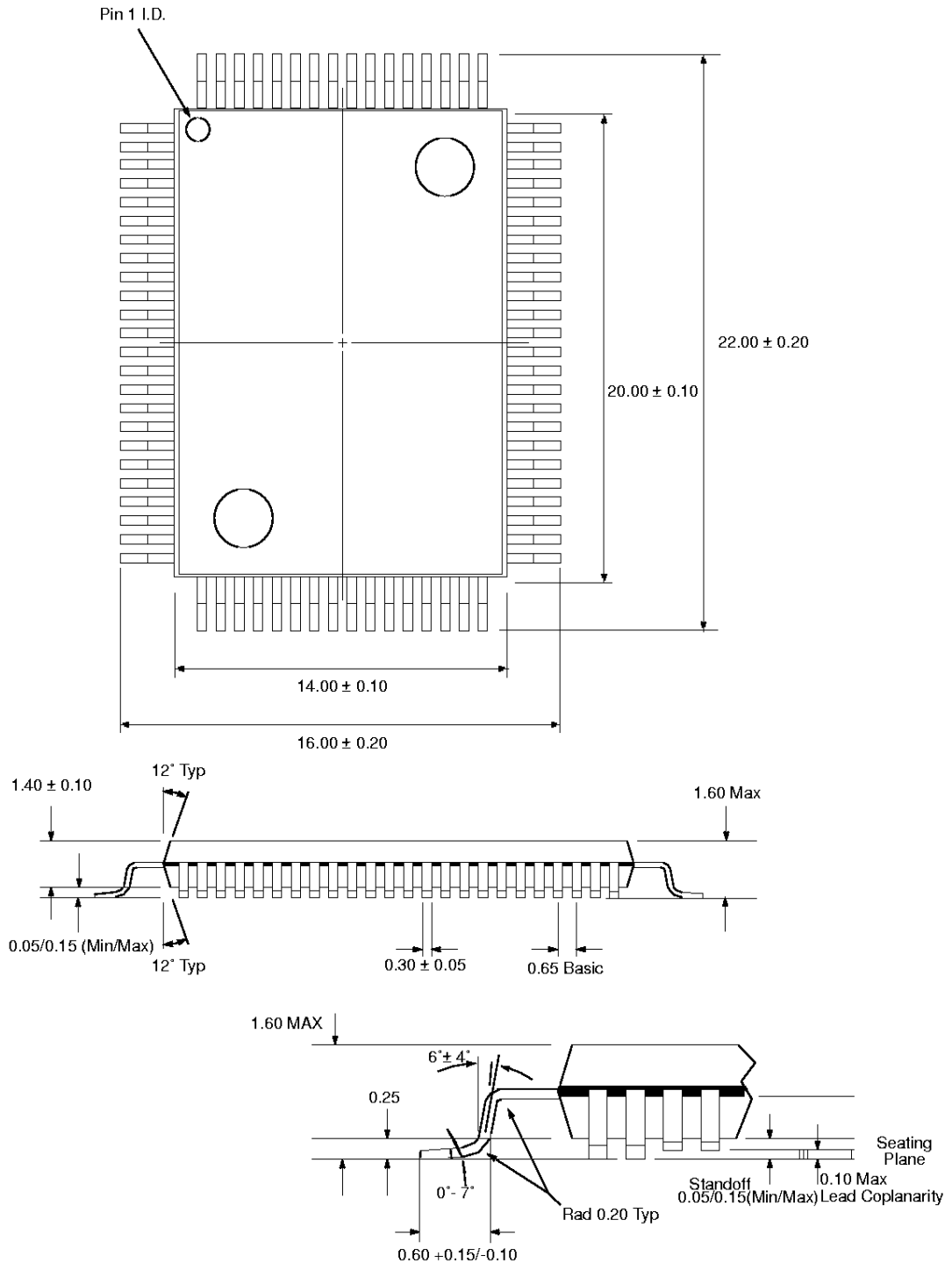
**32K X 36 BURST SRAM**

**Timing Diagram (Burst Write)**



**Notes:**

1. D1(A) and D2(A) refer to data written to address A1 and A2.
2. D2(B) refers to data written to a subsequent internal burst counter address.
3.  $\overline{WEa}$ ,  $\overline{WEb}$ ,  $\overline{WEc}$  and  $\overline{WEd}$  are don't cares when ADSP is sampled LOW.

**100 Pin TQFP Package Diagram**




**32K X 36 BURST SRAM**

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**Revision Log**

| Rev  | Contents of Modification   |
|------|--|
| 5/94 | Initial Release of the 32K x 36 (8/9/11) TQFP BURST MODE Application Spec. |
| 3/95 | Updated -8, -9, -11; Added -10 Specifications.                             |
| 7/95 | Removed Preliminary classification.  |



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