

**512M bits DDR3 SDRAM****EDJ5304AASE (128M words × 4 bits)****EDJ5308AASE (64M words × 8 bits)****EDJ5316AASE (32M words × 16 bits)****Description**

The EDJ5304AASE is a 512M bits DDR3 SDRAM organized as 16,777,216 words × 4 bits × 8 banks.

The EDJ5308AASE is a 512M bits DDR3 SDRAM organized as 8,388,608 words × 8 bits × 8 banks.

They are packaged in 78-ball FBGA ( $\mu$ BGA<sup>®</sup>) package.

The EDJ5316AASE is a 512M bits DDR3 SDRAM organized as 4,194,304 words × 16 bits × 8 banks.

It is packaged in 96-ball FBGA ( $\mu$ BGA<sup>®</sup>) package.

**Features**

- Power supply: VDD, VDDQ = 1.5V ± 0.075V
- Data rate: 1333Mbps/1066Mbps (max.)
- Double-data-rate architecture: two data transfers per clock cycle
- Bi-directional, differential data strobe (DQS and /DQS) is transmitted/received with data, to be used in capturing data at the receiver
- DQS is edge aligned with data for READs: center-aligned with data for WRITEs
- Differential clock inputs (CK and /CK)
- DLL aligns DQ and DQS transitions with CK transitions
- Commands entered on each positive CK edge: data and data mask referenced to both edges of DQS
- 8 internal banks for concurrent operation
- Data mask (DM) for write data
- Burst lengths (BL): 4, 8 and 4 with burst chop
- /CAS latency (CL): 5, 6, 7, 8, 9, 10
- /CAS write latency (CWL): 5, 6, 7, 8
- Auto precharge operation for each burst access
- Auto refresh and self refresh modes
- Average refresh period: 7.8 $\mu$ s
- 1.5V I/O
- Posted CAS by programmable additive latency for better command and data bus efficiency
- On-Die-Termination for better signal quality
- Programmable Partial Array Self Refresh
- ZQ calibration for DQ drive and On-Die-Termination
- RESET-pin for Power-up sequence and reset-function
- FBGA ( $\mu$ BGA) package with lead free solder (Sn-Ag-Cu)
- RoHs compliant

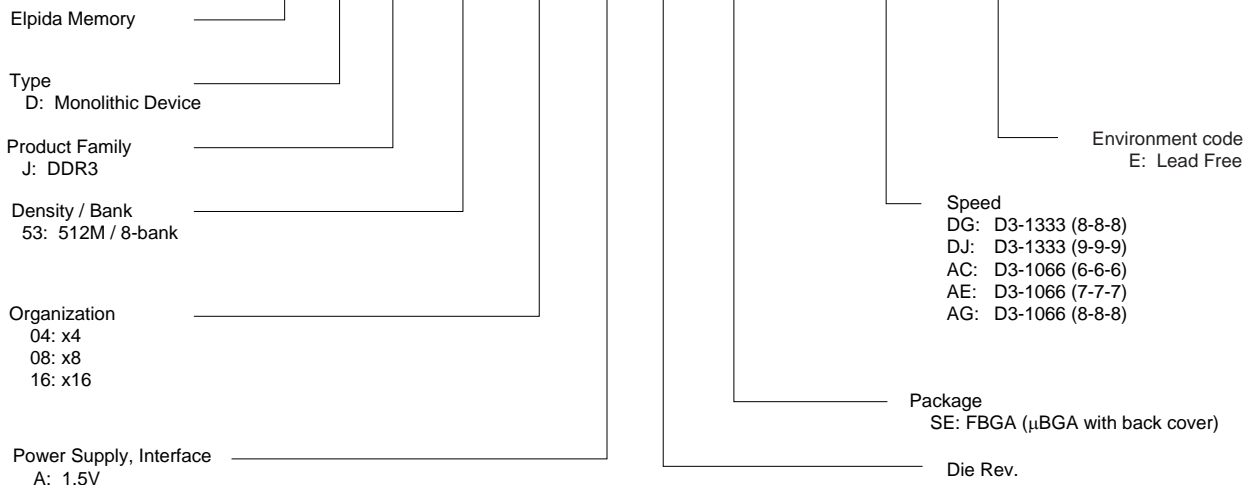
# EDJ5304AASE, EDJ5308AASE, EDJ5316AASE

## Ordering Information

Part number	Mask version	Organization (words × bits)	Internal Banks	Speed bin (CL-tRCD-tRP)	Package
EDJ5304AASE-DG-E	A	128M × 4	8	D3-1333 (8-8-8)	78-ball FBGA (μBGA)
EDJ5304AASE-DJ-E				D3-1333 (9-9-9)	
EDJ5304AASE-AC-E				D3-1066 (6-6-6)	
EDJ5304AASE-AE-E				D3-1066 (7-7-7)	
EDJ5304AASE-AG-E				D3-1066 (8-8-8)	
EDJ5308AASE-DG-E		64M × 8		D3-1333 (8-8-8)	
EDJ5308AASE-DJ-E				D3-1333 (9-9-9)	
EDJ5308AASE-AC-E				D3-1066 (6-6-6)	
EDJ5308AASE-AE-E				D3-1066 (7-7-7)	
EDJ5308AASE-AG-E				D3-1066 (8-8-8)	
EDJ5316AASE-DG-E		32M × 16		D3-1333 (8-8-8)	96-ball FBGA (μBGA)
EDJ5316AASE-DJ-E				D3-1333 (9-9-9)	
EDJ5316AASE-AC-E				D3-1066 (6-6-6)	
EDJ5316AASE-AE-E				D3-1066 (7-7-7)	
EDJ5316AASE-AG-E				D3-1066 (8-8-8)	

## Part Number

# E D J 53 04 A A S E - D G - E



**NOTES FOR CMOS DEVICES****① PRECAUTION AGAINST ESD FOR MOS DEVICES**

Exposing the MOS devices to a strong electric field can cause destruction of the gate oxide and ultimately degrade the MOS devices operation. Steps must be taken to stop generation of static electricity as much as possible, and quickly dissipate it, when once it has occurred. Environmental control must be adequate. When it is dry, humidifier should be used. It is recommended to avoid using insulators that easily build static electricity. MOS devices must be stored and transported in an anti-static container, static shielding bag or conductive material. All test and measurement tools including work bench and floor should be grounded. The operator should be grounded using wrist strap. MOS devices must not be touched with bare hands. Similar precautions need to be taken for PW boards with semiconductor MOS devices on it.

**② HANDLING OF UNUSED INPUT PINS FOR CMOS DEVICES**

No connection for CMOS devices input pins can be a cause of malfunction. If no connection is provided to the input pins, it is possible that an internal input level may be generated due to noise, etc., hence causing malfunction. CMOS devices behave differently than Bipolar or NMOS devices. Input levels of CMOS devices must be fixed high or low by using a pull-up or pull-down circuitry. Each unused pin should be connected to  $V_{DD}$  or GND with a resistor, if it is considered to have a possibility of being an output pin. The unused pins must be handled in accordance with the related specifications.

**③ STATUS BEFORE INITIALIZATION OF MOS DEVICES**

Power-on does not necessarily define initial status of MOS devices. Production process of MOS does not define the initial operation status of the device. Immediately after the power source is turned ON, the MOS devices with reset function have not yet been initialized. Hence, power-on does not guarantee output pin levels, I/O settings or contents of registers. MOS devices are not initialized until the reset signal is received. Reset operation must be executed immediately after power-on for MOS devices having reset function.

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