DENSE-PAC MICROSYSTEMS

3 Megabit High Speed CMOS SRAM

DPS128X24Bn3

DESCRIPTION:

The DPS128X24Bn3 High Speed SRAM "STACK" modules are a revolutionary new memory subsystem using Dense-Pac Microsystems' ceramic Stackable Leadless Chip Carriers (SLCC). Available in straight leaded, "J" leaded or gullwing leaded packages, or mounted on a 50-pin PGA co-fired ceramic substrate. The module packs 3-Megabits of low-power CMOS static RAM in an area as small as 0.463 in^2, while maintaining a total height as low as 0.332 inches.

The DPS128X24Bn3 STACK modules contain three individual 128K x 8 SRAMs, each packaged in a hermetically sealed SLCC, making the modules suitable for commercial, industrial and military applications.

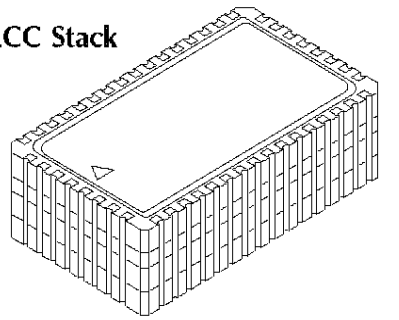
By using SLCCs, the "Stack" family of modules offer a higher board density of memory than available with conventional through-hole, surface mount or hybrid techniques.

FEATURES:

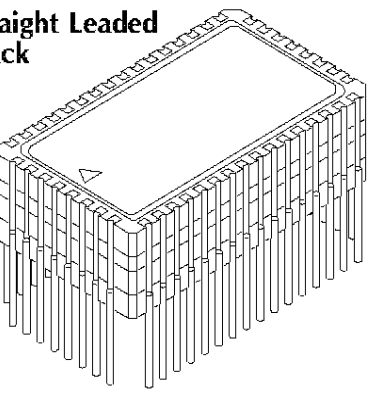
- Organizations Available: 128Kx24, 384Kx8
- Access Times: 20*, 25, 30, 35, 45ns
- Fully Static Operation - No clock or refresh required
- Single +5V Power Supply, ±10% Tolerance
- TTL Compatible
- Common Data Inputs and Outputs
- Low Data Retention Voltage: 2.0V min.
- Packages Available:
  - 48 - Pin SLCC Stack
  - 48 - Pin Straight Leaded Stack
  - 48 - Pin "J" Leaded Stack
  - 48 - Pin Gullwing Leaded Stack
  - 50 - Pin PGA Dense-Stack

* Commercial only.

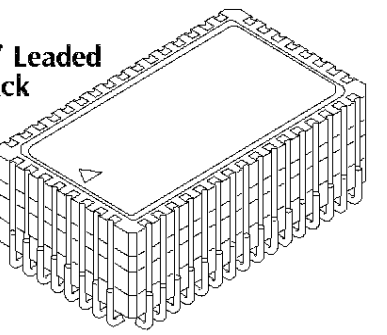
SLCC Stack



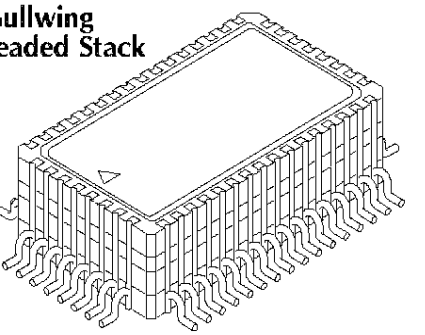
Straight Leaded Stack



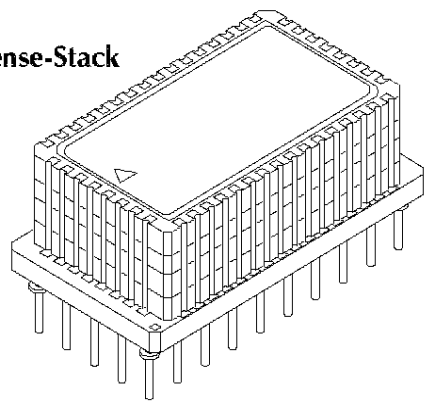
"J" Leaded Stack



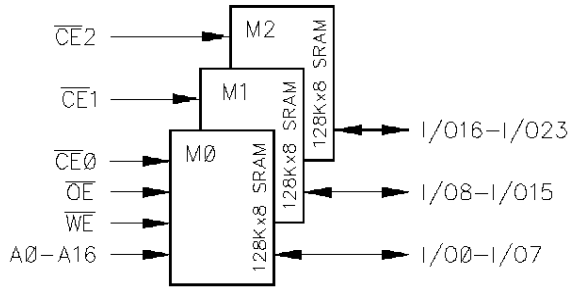
Gullwing Leaded Stack



Dense-Stack



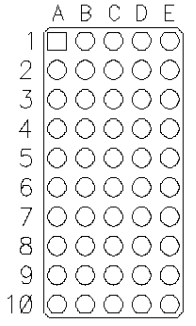
FUNCTIONAL BLOCK DIAGRAM



PIN NAMES	
A0 - A16	Address Inputs
I/O0 - I/O23	Data Input/Output
$\overline{CE}$0 - $\overline{CE}$2	Low Chip Enables
$\overline{WE}$	Write Enable
$\overline{OE}$	Output Enable
V_{DD}	Power (+5V)
V_{SS}	Ground

PIN-OUT DIAGRAM

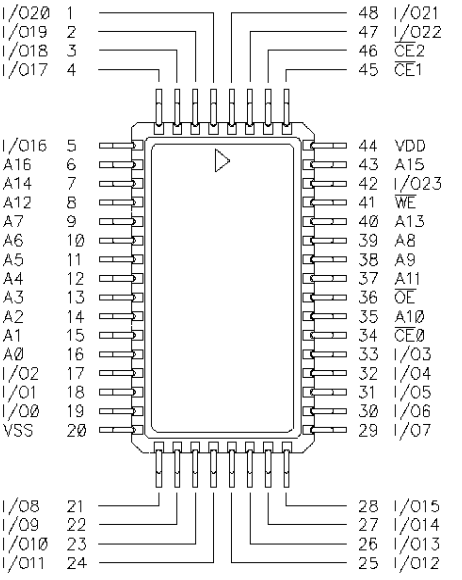
(TOP VIEW)



50 - PIN PGA
DENSE-STACK

	A	B	C	D	E
1	I/017	I/019	I/021	$\overline{CE}$2	$\overline{CE}$1
2	VSS	I/018	I/02Ø	I/022	VDD
3	I/016	A16	$\overline{WE}$	I/023	A15
4	A14	A12	A7	A8	A13
5	A6	A5	$\overline{OE}$	A11	A9
6	A4	A3	A2	$\overline{CE}$Ø	A1Ø
7	A1	AØ	I/05	I/04	I/03
8	I/02	I/01	I/0Ø	I/07	I/06
9	VSS	I/09	I/011	I/013	VDD
1Ø	I/08	I/01Ø	I/012	I/014	I/015

48 - PIN LEADLESS STACK
48 - PIN STRAIGHT LEADED STACK
48 - PIN "J" LEADED STACK
48 - PIN GULLWING LEADED STACK



ABSOLUTE MAXIMUM RATINGS [3]			
Symbol	Parameter	Value	Unit
T_{STC}	Storage Temperature	-65 to +150	°C
T_{BIAS}	Temperature Under Bias	-55 to +125	°C
V_{DD}	Supply Voltage [1]	-0.5 to +7.0	°C
$V_{I/O}$	Input/Output Voltage [1]	-0.5 to V_{DD}+0.5	V

TRUTH TABLE					
Mode	$\overline{CE}$	$\overline{WE}$	$\overline{OE}$	I/O Pin	Supply Current
Not Selected	H	X	X	High-Z	Standby
D_{OUT} Disable	L	H	H	High-Z	Active
Read	L	H	L	D_{OUT}	Active
Write	L	L	X	D_{IN}	Active

H = HIGH L = LOW X = Don't Care

DC OUTPUT CHARACTERISTICS					
Symbol	Parameter	Conditions	Min.	Max.	Unit
V_{OH}	HIGH Voltage	I_{OH} = -4.0mA	2.4		V
V_{OL}	LOW Voltage	I_{OL} = 8.0mA		0.4	V

RECOMMENDED OPERATING RANGE [3]						
Symbol	Characteristic		Min.	Typ.	Max.	Unit
V_{DD}	Supply Voltage		4.5	5.0	5.5	V
V_{IH}	Input HIGH Voltage		2.2		V_{DD}+0.3	V
V_{IL}	Input LOW Voltage		-0.5[2]		0.8	V
T_A	Operating Temperature	M/B	-55	+25	+125	°C
		I	-40	+25	+85	
		C	0	+25	+70	

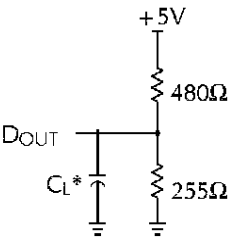
CAPACITANCE [4]: T_A = 25°C, F = 1.0MHz				
Symbol	Parameter	Max.	Unit	Condition
C_{ADR}	Address Input	35	pF	V_{IN}[2] = 0V
C_{CE}	Chip Enable	15		
C_{WE}	Write Enable	35		
C_{OE}	Output Enable	35		
$C_{I/O}$	Data Input/Output	15		

DC OPERATING CHARACTERISTICS: Over operating ranges											
Symbol	Characteristics	Test Conditions		Typ.*	C		I		M/B		Unit
					Min.	Max.	Min.	Max.	Min.	Max.	
I_{IN}	Input Leakage Current	V_{IN} = 0V to V_{DD}		-	-15	+15	-15	+15	-15	+15	µA
I_{OUT}	Output Leakage Current	$V_{I/O}$ = 0V to V_{DD}, $\overline{CE}$ or $\overline{OE}$ = V_{IH}, or $\overline{WE}$ = V_{IL}		-	-10	+10	-10	+10	-10	+10	µA
I_{CC}	Operating Supply Current	Cycle=min., Duty=100% I_{OUT} = 0mA	x8	150		200		210		230	mA
			x24	300		420		420		480	
I_{SB1}	Full Standby Supply Current	$V_{IN} \geq V_{DD}$ -0.2V or $V_{IN} \leq V_{SS}$ +0.2V		1.2		15		15		30	mA
I_{SB2}	Standby Current (TTL)	$\overline{CE}$ = V_{IH}		75		90		105		105	mA
I_{DR3}	Data Retention Supply Current (3V)	V_{DR} = 3V, $\overline{CE} \geq V_{DR}$ -0.2V		0.21		1.2		1.8		6.0	mA
I_{DR2}	Data Retention Supply Current (2V)	V_{DR} = 2V, $\overline{CE} \geq V_{DR}$ -0.2V		.105		0.75		1.2		5.4	mA
V_{OL}	Output Low Voltage	I_{OUT} = 8.0mA		-		0.4		0.4		0.4	V
V_{OH}	Output High Voltage	I_{OUT} = -4.0mA		-	2.4		2.4		2.4		V

† Typical measurements made at +25°C, Cycle = min., V_{DD} = 5.0V.

OUTPUT LOAD		
Load	**C_L**	**Parameters Measured**
1	30pF	except t_{LZ},t_{HZ}, t_{OHZ}, t_{OLZ}, and t_{WHZ}
2	5pF	t_{LZ}, t_{HZ}, t_{OHZ}, t_{OLZ}, and t_{WHZ}

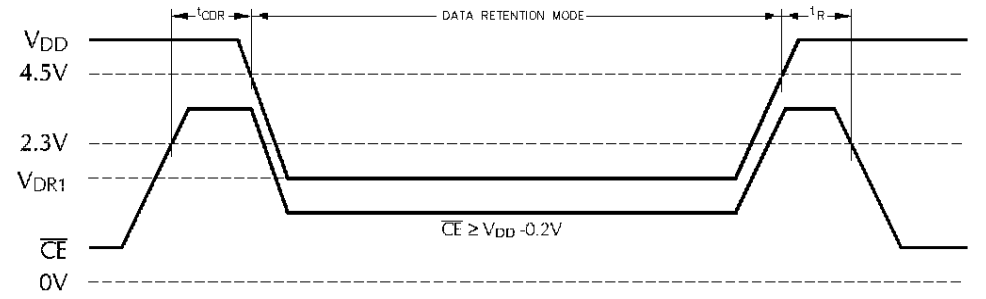
Figure 1. Output Load
* Including Probe and Jig Capacitance.



AC TEST CONDITIONS	
Input Pulse Levels	0V to 3.0V
Input Pulse Rise and Fall Times	5ns
Input and Output Timing Reference Levels	1.5V

Data Retention AC Characteristics [8]						
Symbol	**Parameter**	**Test Conditions**	**Min.**	**Typ.**	**Max.**	**Unit**
V_{DR}	V_{DD} for Data Retention	$\overline{CE} \geq V_{DR}$ -0.2V	2.0	-	-	V
V_{CDR}	Chip Disable to Data Retention Time	See Data Retention Waveform	0	-	-	ns
t_R	Operation Recovery Time	See Data Retention Waveform	5	-	-	ms

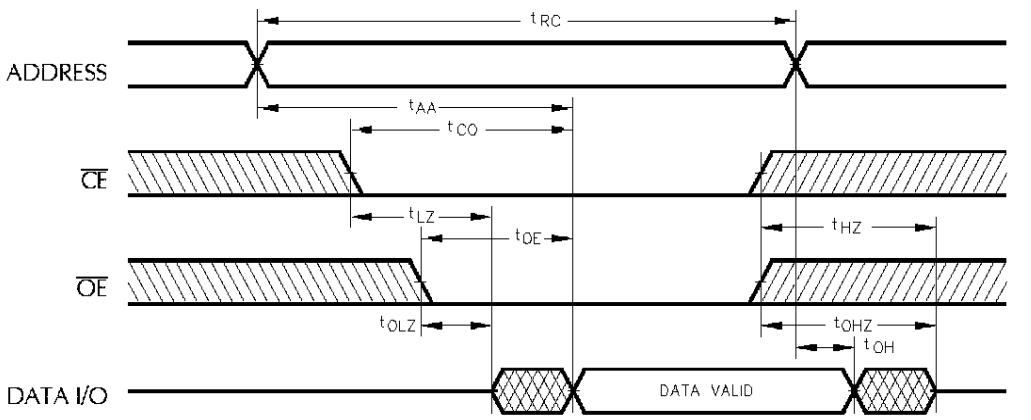
DATA RETENTION WAVEFORM: $\overline{CE}$ Controlled.



AC OPERATING CONDITIONS AND CHARACTERISTICS - READ CYCLE: Over operating ranges													
No.	Symbol	Parameter	20ns*		25ns		30ns		35ns		45ns		Unit
			Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
1	t_{RC}	Read Cycle Time	20		25		30		35		45		ns
2	t_{AA}	Address Access Time		20		25		30		35		45	ns
3	t_{CO}	$\overline{CE}$ to Output Valid		20		25		30		35		45	ns
4	t_{OE}	Output Enable to Output Valid		8		10		15		20		25	ns
5	t_{LZ}	$\overline{CE}$ to Output in LOW-Z [4, 5]	3		3		3		3		3		ns
6	t_{OLZ}	Output Enable to Output in LOW-Z [4, 5]	0		0		0		0		0		ns
7	t_{HZ}	$\overline{CE}$ to Output in HIGH-Z [4, 5]		10		12		15		20		25	ns
8	t_{OHZ}	Output Enable to Output in HIGH-Z [4, 5]		8		10		15		20		25	ns
9	t_{OH}	Output Hold from Address Change	3		3		3		3		3		ns

* Available in Commercial Only.

READ CYCLE

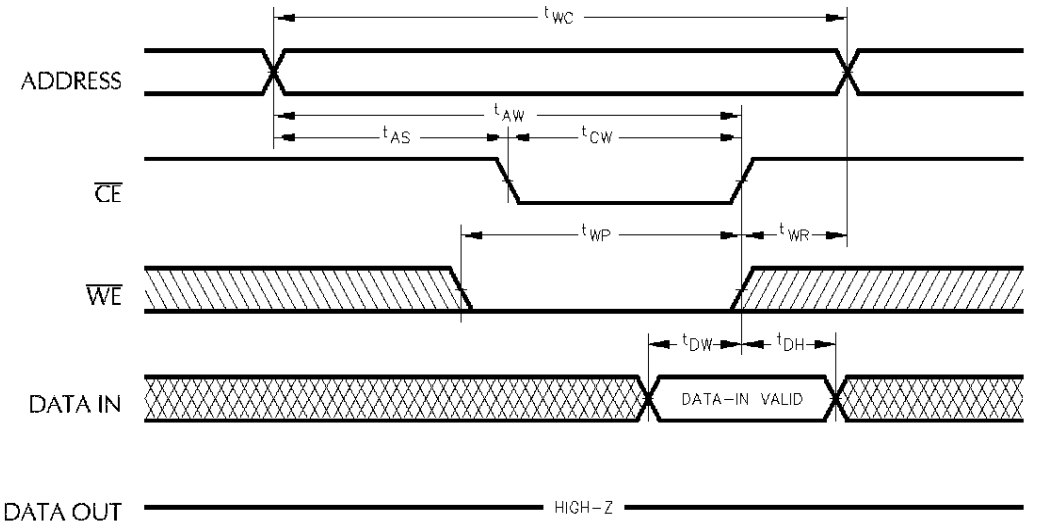


WAVEFORM KEY

AC OPERATING CONDITIONS AND CHARACTERISTICS - WRITE CYCLE [6,7]: Over operating ranges													
No.	Symbol	Parameter	20ns*		25ns		30ns		35ns		45ns		Unit
			Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
10	t_{WC}	Write Cycle Time	20		25		30		35		45		ns
11	t_{AW}	Address Valid to End of Write	15		20		25		30		40		ns
12	t_{CW}	Chip Enable to End of Write	15		20		25		30		40		ns
13	t_{AS}	Address Set-Up Time **	0		0		0		0		0		ns
14	t_{WP}	Write Pulse Width	15		20		25		30		35		ns
15	t_{WR}	Write Recovery Time	0		0		0		0		0		ns
16	t_{WHZ}	Write Enable to Output in HIGH-Z [4,5]		8		10		12		15		20	ns
17	t_{DW}	Data to Write Time Overlap	12		15		15		20		25		ns
18	t_{DH}	Data Hold from Write Time	0		0		0		0		0		ns
19	t_{OW}	Output Active from End of Write	3		3		3		3		3		ns

* Available in Commercial Only.

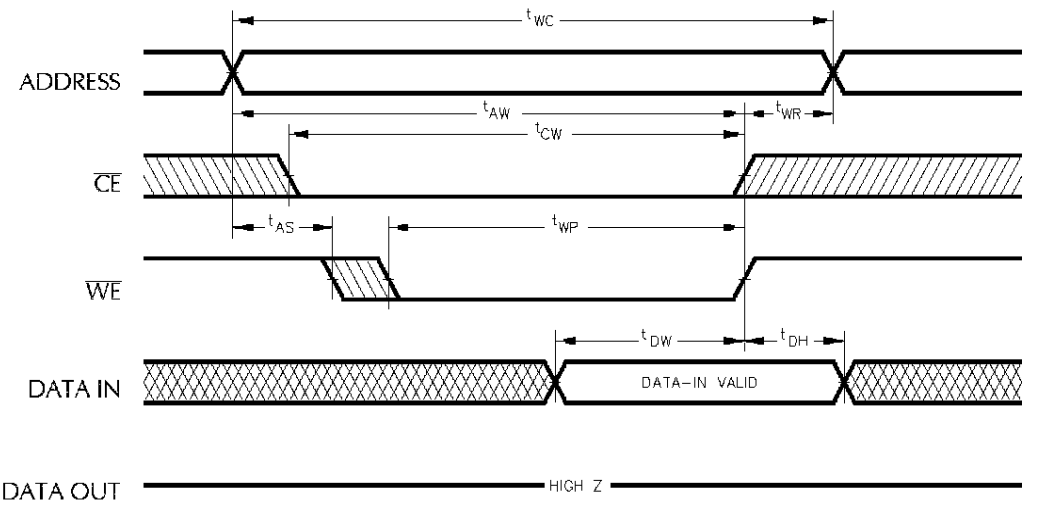
WRITE CYCLE 1: $\overline{CE}$ Controlled.



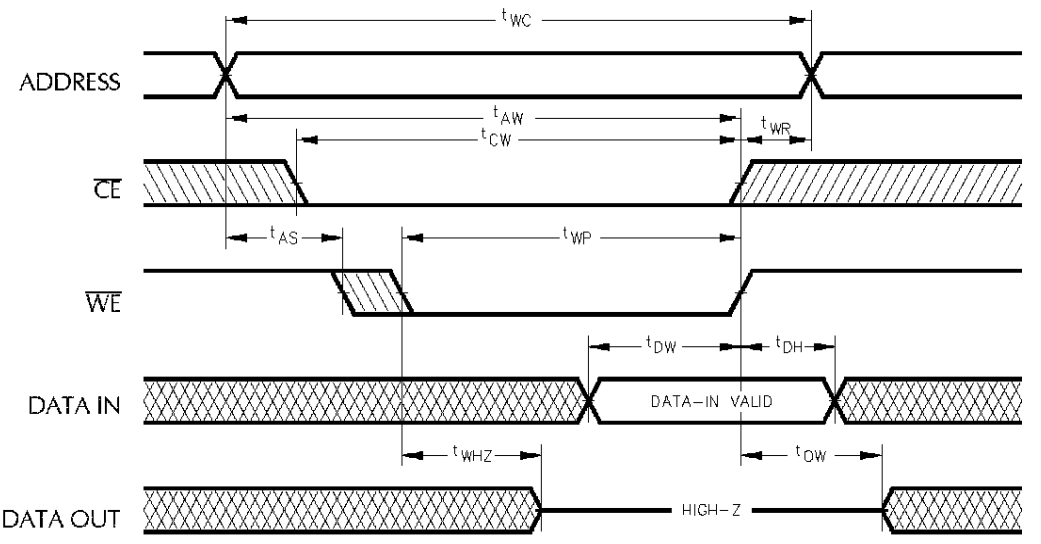
NOTES:

1. All voltages are with respect to V_{SS}.
2. -2.0V min. for pulse width less than 20ns (V_{IL} min. = -0.5V at DC level).
3. Stresses greater than those under **ABSOLUTE MAXIMUM RATINGS** may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.
4. This parameter is guaranteed and not 100% tested.
5. Transition is measured at the point of ±500mV from steady state voltage.
6. When $\overline{OE}$ and $\overline{CE}$ are LOW and $\overline{WE}$ is HIGH, I/O pins are in the output state,and input signals of opposite phase to the outputs must not be applied.
7. The outputs are in a high impedance state when $\overline{WE}$ is LOW.
8. Chip Enable and Write Enable can initiate and terminate WRITE Cycle.

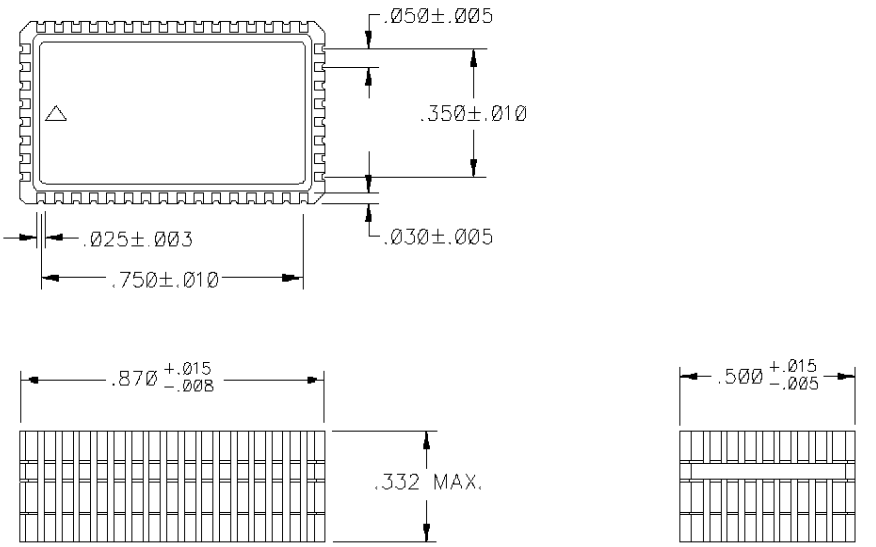
WRITE CYCLE 2: $\overline{WE}$ Controlled. $\overline{OE}$ is HIGH. [8]



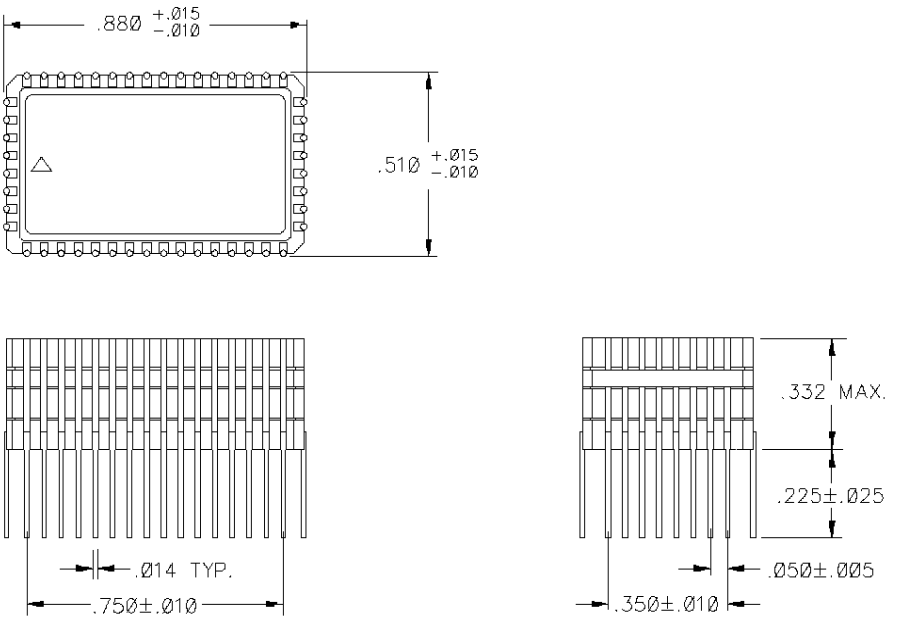
WRITE CYCLE 3: $\overline{WE}$ Controlled. $\overline{OE}$ is LOW. [8]



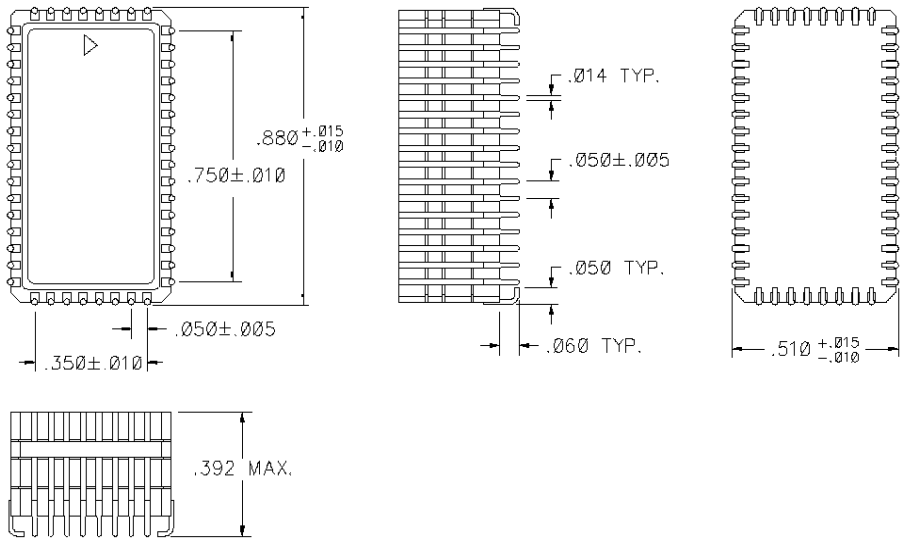
(48 - PIN LEADLESS STACK) MECHANICAL DRAWING



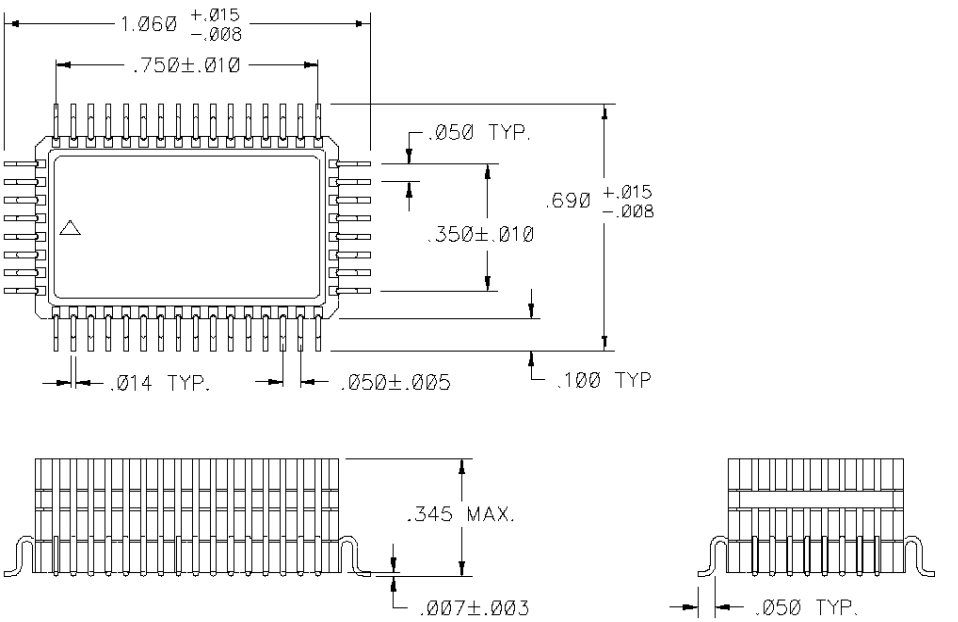
(48 - PIN STRAIGHT LEADED STACK) MECHANICAL DRAWING



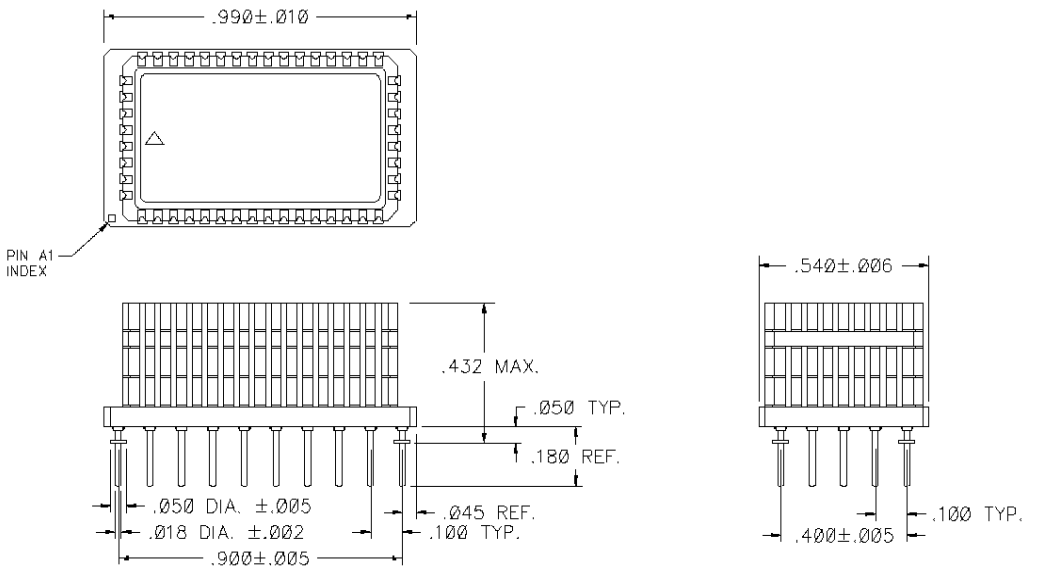
(48 - PIN "J" LEADED STACK) MECHANICAL DRAWING



(48 - PIN GULLWING LEADED STACK) MECHANICAL DRAWING



(50 - PIN PGA) MECHANICAL DRAWING



ORDERING INFORMATION

DP S 128 X 24 B X3 – XX X

PREFIX | TYPE | MEMORY DEPTH | DESIG | MEMORY WIDTH | DESIG. | PACKAGE | SPEED | GRADE

C	COMMERCIAL	0°C to +70°C
I	INDUSTRIAL	–40°C to +85°C
M	MILITARY	–55°C to +125°C
B	MIL–PROCESSED	–55°C to +125°C

20	20ns (COMMERCIAL ONLY)
25	25ns
30	30ns
35	35ns
45	45ns

A3	DENSE–STACK PGA (PIN GRID ARRAY)
H3	GULLWING LEADED SLCC STACK
I3	THRU–HOLE LEADED SLCC STACK
J3	"J" LEADED SLCC STACK
Y3	LEADLESS SLCC STACK

B HIGH SPEED / SINGLE CHIP ENABLE

MODULE WITHOUT SUPPORT LOGIC

CMOS SRAM DEVICES

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