15. ELECTRICAL SPECIFICATIONS

Available Electrical Specifications

		μPD70236A-10	μPD70236A-12	μPD70236A-16	μPD70236A-20
Vᴅᴅ = 5 V ±10%	Tᴀ = −40 to +85 °C	√ (10 MHz)	√ (12.5 MHz)	√ (16 MHz)	√ (20 MHz)
	Tᴀ = −10 to +70 °C	—	—	√ (16 MHz)	√ (20 MHz)
Vᴅᴅ = 3.6 to 4.5 V	Tᴀ = −40 to +85 °C	—	—	√ (12.5 MHz)	√ (16 MHz)
Vᴅᴅ = 2.7 to 3.6 V	Tᴀ = −40 to +85 °C	—	—	√ (8 MHz)	√ (10 MHz)

Remarks 1. √ : Electrical specification available   − : No electrical specification

2. Figures in parentheses show the maximum operating frequency fx.

15.1 SPECIFICATIONS WHEN Vᴅᴅ = 5 V ± 10%

Absolute Maximum Ratings (Tᴀ = 25 °C)

PARAMETER	SYMBOL	TEST CONDITIONS	RATING	UNIT
Supply voltage	Vᴅᴅ		−0.5 to +7.0	V
Input voltage	Vɪ	Except X1, Vᴅᴅ = 5 V ±10%	−0.5 to Vᴅᴅ+0.3	V
Clock input voltage	Vᴋ	X1, Vᴅᴅ = 5 V ±10%	−0.5 to Vᴅᴅ+1.0	V
Output short current	Iᴏs		50	mA
Output voltage	Vᴏ	Vᴅᴅ = 5 V ±10%	−0.5 to Vᴅᴅ+0.3	V
Operating ambient temperature	Tᴀ		−40 to +85	°C
Storage temperature	Tₛₜg		−65 to +150	°C

Cautions 1. Do not connect output pin (or I/O pin) of IC product directly to other output pins, Vᴅᴅ, Vᴄᴄ or GND. Open drain output pins or open collector output pins, however, can be connected each other. Output pins having high impedance capability can be also connected each other in an external circuit designed the timing to prevent output conflict.

2. Exposure to Absolute Maximum Ratings for extended periods may affect device reliability; exceeding the ratings could cause permanent damage. The parameters apply independently.
The device should be operated within the limits specified under DC and AC Characteristics.

DC Characteristics (μPD70236A-10/-12/-16/-20 : T_A = −40 to +85 °C, V_{DD} = 5 V ± 10 %)
(μPD70236A-16/-20 : T_A = −10 to +70 °C, V_{DD} = 5 V ± 10 %)

PARAMETER	SYMBOL	TEST CONDITIONS	MIN.	TYP.	MAX.	UNIT
Input voltage, high	V_{IH}	Except $\overline{RESET}$	2.2		V_{DD}+0.3	V
		$\overline{RESET}$	0.8 V_{DD}		V_{DD}+0.3	V
Input voltage, low	V_{IL}	Except $\overline{RESET}$	−0.5		+0.8	V
		$\overline{RESET}$	−0.5		0.2 V_{DD}	V
Clock input voltage, high	V_{KH}	X2, X1	0.8 V_{DD}		V_{DD}+0.5	V
Clock input voltage, low	V_{KL}	X2, X1	−0.5		+0.6	V
Output voltage, high	V_{OH}	I_{OH} = −2.5 mA	0.7 V_{DD}			V
		I_{OH} = −100 μA	V_{DD}−0.4			V
Output voltage, low	V_{OL}	Except $\overline{TC}$, I_{OL} = 2.5 mA			0.45	V
		$\overline{TC}$, I_{OL} = 5.0 mA			0.45	V
Input leak current, high	I_{LIH}	V_I = V_{DD}			10	μA
Input leak current, low	I_{LIL}	V_I = 0 V			−10	μA
Output leak current, high	I_{LOH}	V_O = V_{DD}			10	μA
Output leak current, low	I_{LOL}	V_O = 0 V			−10	μA
High-level latch leakage current	I_{LLH}	V_I = 3.0 V	−20		−200	μA
Low-level latch leakage current	I_{LLL}	V_I = 0.8 V	20		200	μA
Latch inversion current (L → H)	I_{ILH}				200	μA
Latch inversion current (H → L)	I_{ILL}				−200	μA
Supply current[Note]	I_{DD}	In operation (f_X = 2 to 20 [MHz])		3.9f_X + 3	6f_X + 5	mA
		HALT (f_X=2 to 20 MHz)		0.025f_X+0.5	0.35f_X+3	mA
		STOP		5.0	200	μA

Note Setting condition : The CPU clock is used for the TCLK0 to TCLK2 with refreshing enabled.
The units of the constants 3.9, 6, 0.025 and 0.35 are mA/MHz.

Remark The TYP. values are the reference values when T_A = 25 °C and V_{DD} = 5.0 V.

Capacitance (T_A = 25 °C, V_{DD} = 0 V)

PARAMETER	SYMBOL	TEST CONDITIONS	MIN.	TYP.	MAX.	UNIT
Input capacitance	C_I	f_C = 1 MHz Unmeasured pins returned to 0 V.			15	pF
Input output capacitance	C_{IO}				15	pF
Output capacitance	C_O				15	pF

Recommended Oscillator Circuit

(a)   Ceramic resonator connection (T$_A$ = –40 to +85 °C, V$_{DD}$ = 5 V ± 10 %)

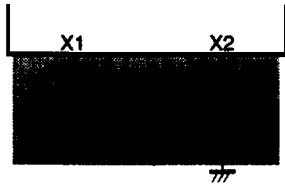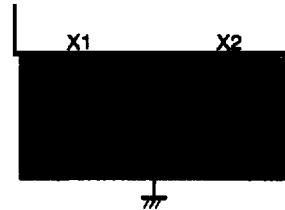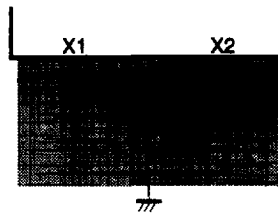**Fig. 1**   **Fig. 2**

MANUFACTURER	OSCILLATOR FREQUENCY f$_{xx}$ [MHz]	PRODUCT NAME	RECOMMENDED CONSTANT			CIRCUIT DIAGRAM
			C1 [pF]	C2 [pF]	Rd [Ω]	
Murata Mfg. Co., Ltd.	40	CSA40.00MXZ040	—	5	33	Fig.1
	32	CSA32.00MXZ040	—	5	33	
	25	CSA25.00MXZ040	—	5	33	
	20	CSA20.00MXZ040	7	15	33	Fig. 2

Cautions 1.   The oscillation circuit should be located as close as possible to the X1 and X2 pins.
2.   No other signal lines should cross the shaded area.
3.   Sufficient evaluation is required for matching between the μPD70236A and the resonator.

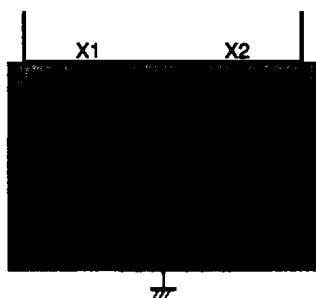(b)   Crystal resonator connection (T$_A$ = –40 to +85 °C, V$_{DD}$ = 5 V ± 10 %)
  (i)   Recommended conditions of oscillation with basic wave

MANUFACTURER	OSCILLATOR FREQUENCY f$_{xx}$ [MHz]	PRODUCT NAME	RECOMMENDED CONSTANT	
			C1 [pF]	C2 [pF]
Kinseki, Ltd.	20	HC-49/U	10	10

Cautions 1.   The oscillation circuit should be located as close as possible to the X1 and X2 pins.
2.   No other signal lines should cross the shaded area.
3.   Sufficient evaluation is required for matching between the μPD70236A and the resonator.

(II) **Recommended conditions with third overtone**

MANUFACTURER	OSCILLATOR FREQUENCY fxx [MHz]	PRODUCT NAME	RECOMMENDED CONSTANT			
			C1 [pF]	C2 [pF]	C3 [pF]	L [μH]
Kinseki, Ltd.	40	HC-49/U	5	1000	5	3.3
	32		5	1000	5	5.6
	25		5	1000	10	4.7

Cautions 1. The oscillation circuit should be located as close as possible to the X1 and X2 pins.
2. No other signal lines should cross the shaded area.
3. Sufficient evaluation is required for matching between the μPD70236A and the resonator.
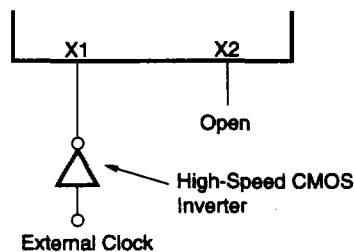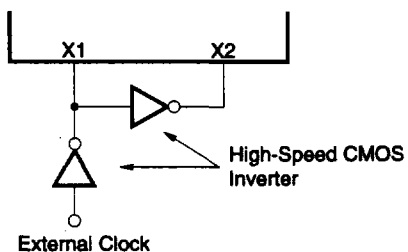
(c) **External clock Input**

Cautions 1. The high-speed CMOS Inverter should be located as close as possible to the X1 and X2 pins.
2. Ensure that matching between the μPD70236A and the high-speed CMOS Inverter is fully evaluated.

AC Characteristics (V_{DD} = 5 V ± 10 %, Output pin load capacitance : C_L = 100 pF)

(1) μPD70236A-10 (V_{DD} = 5 V ± 10 %)

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PARAMETER	SYMBOL		FIG.No.	TEST CONDITIONS	T_A = −40 to +85 °C		UNIT
					MIN.	MAX.	
External clock input cycle	①	t_{CYX}	15–1		50	250	ns
External clock input high-level width	②	t_{XKH}	15–1		15		ns
External clock input low-level width	③	t_{XKL}	15–1		15		ns
External clock input rise time	④	t_{XKR}	15–1			10	ns
External clock input fall time	⑤	t_{XKF}	15–1			10	ns
CPU operating frequency	–	f_X	–		2	10	MHz
CLKOUT output frequency	⑥	t_{CYK}	15–1		100	500	ns
CLKOUT high-level width	⑦	t_{KKH}	15–1		0.5t_{CYK}–12		ns
CLKOUT low-level width	⑧	t_{KKL}	15–1		0.5t_{CYK}–12		ns
CLKOUT rise time	⑨	t_{KR}	15–1	1.0 V → 3.5 V		12	ns
CLKOUT fall time	⑩	t_{KF}	15–1	3.5 V → 1.0 V		12	ns
CLKOUT delay time (from external clock)	⑪	t_{DXK}	15–1		4	30	ns
PCLKOUT output frequency	⑫	t_{CYPK}	15–1		4t_{CYX}	1000	ns
PCLKOUT high-level width	⑬	t_{PKH}	15–1		2t_{CYX}–12		ns
PCLKOUT low-level width	⑭	t_{PKL}	15–1		2t_{CYX}–12		ns
PCLKOUT output rise time	⑮	t_{PKR}	15–1	1.0 V → 3.5 V		12	ns
PCKLOUT output fall time	⑯	t_{PKF}	15–1	3.5 V → 1.0 V		12	ns
Input rise time[Note 1]	⑰	t_{IR}		0.8 V → 2.2 V		15	ns
Input fall time[Note 1]	⑱	t_{IF}		2.2 V → 0.8 V		10	ns
Output rise time[Note 2]	⑲	t_{OR}		0.8 V → 2.2 V		15	ns
Output fall time[Note 2]	⑳	t_{OF}		2.2 V → 0.8 V		10	ns
$\overline{RESET}$ setup time (to CLKOUT↓)	㉑	t_{SRSTK}	15–2		30		ns
$\overline{RESET}$ hold time (from CLKOUT↓)	㉒	t_{HKRST}	15–2		15		ns
RESOUT output delay time (from CLKOUT↓)	㉓	t_{DKRO}	15–2		0	40	ns
$\overline{RESET}$ low-level width	㉔	t_{WRSTL}	15–2		6t_{CYK}		ns
READY setup time (to CLKOUT↑)	㉕	t_{SRYK}	15–3, etc.		10		ns
READY hold time (from CLKOUT↑)	㉖	t_{HKRY}	15–3, etc.		20		ns
$\overline{BCYST}$ high-level width	㉗	t_{BCBCH}	15–5, etc.		t_{CYK}(n+1)–10[Note 3]		ns
$\overline{BCYST}$ low-level width	㉘	t_{BCBCL}	15–5, etc.		t_{CYK}–10		ns
$\overline{BCYST}$ delay time from CLKOUT↓	㉙	t_{DKBC}	15–5, etc.		3	35	ns
$\overline{MRD}$ delay time from CLKOUT	㉚	t_{DKMR}	15–5, etc.		0	40	ns

Notes 1. Except external clock and $\overline{RESET}$
       2. Except CLKOUT and PCLKOUT
       3. n indicates the number of wait clock cycles inserted in the bus cycle. In a co-processor cycle, 1 (=TC cycle) must be added to n.

Remark   The number in the symbol column correspond to the numbers in the timing charts.

μPD70236A-10 (V_DD = 5 V ± 10 %)

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PARAMETER	SYMBOL		FIG.No.	TEST CONDITIONS	T_A = −40 to +85 °C		UNIT
					MIN.	MAX.	
$\overline{MRD}\downarrow$, $\overline{IORD}\downarrow$ delay time from address/status output	③	t_DARL	15–5, etc.		0.5t_CYK−15		ns
Data hold time (from $\overline{MRD}\uparrow$, from $\overline{IORD}\uparrow$)	③	t_HRD	15–5, etc.		0		ns
Address delay time from CLKOUT↓[Note 1]	③	t_DKA	15–5, etc.		2	35	ns
Data hold time (from R/$\overline{W}\downarrow$)	③	t_HRWD	15–5		0		ns
Status delay time from CLKOUT↓	③	t_DKST	15–5, etc.		3	35	ns
$\overline{DSTB}\downarrow$ output delay time from CLKOUT↑	③	t_DKDS	15–5, etc.		5	40	ns
$\overline{DSTB}\uparrow$ output delay time from CLKOUT	③	t_DKDSH	15–5, etc.		3	40	ns
$\overline{DSTB}\downarrow$ delay time from address/status output	③	t_DADSL	15–5, etc.		0.5t_CYK−15		ns
$\overline{DSTB}$ high-level width	③	t_DSDSH	15–5, etc.		0.5t_CYK−10		ns
$\overline{DSTB}$ low-level width	④	t_DSDSL	15–6, etc.		t_CYK(n+1)−10[Note 4]		ns
Data hold time (from $\overline{DSTB}\uparrow$)	④	t_HDSD	15–5, etc.		0		ns
Data hold time (from address/status change point)	④	t_HASD	15–5		0		ns
Control 1[Note 2] delay time from CLKOUT	④	t_DKCT1	15–21		0	40	ns
Control 2[Note 3] delay time from CLKOUT	④	t_DKCT2	15–5, etc.		0	40	ns
Data setup time (to CLKOUT↓)	④	t_SDK	15–5, etc.		10		ns
Data hold time (from CLKOUT↓)	④	t_HKD	15–5, etc.		10		ns
Output floating time from $\overline{DSTB}\downarrow$	④	t_DHZ	15–5, etc.			0	ns
Address/status hold time from $\overline{MWR}\uparrow$	④	t_HMWHA	15–6		0.5t_CYK−15		ns
$\overline{MWR}$ delay time from CLKOUT	④	t_DKMW	15–6, etc.		0	40	ns
$\overline{MWR}\downarrow$, $\overline{IOWR}\downarrow$ delay time from address/status output	⑤	t_DAWL	15–6, etc.		0.5t_CYK−15		ns
$\overline{MWR}$, $\overline{IOWR}$ low-level width	⑤	t_WWL	15–6, etc.		t_CYK(n+1)−10[Note 4]		ns
Address/status hold time from $\overline{DSTB}\uparrow$	⑤	t_HDSHA	15–6, etc.		0.5t_CYK−15		ns
Data output delay time from $\overline{DSTB}\uparrow$	⑤	t_DDSHD	15–6, etc.		0.5t_CYK−15		ns
Data delay time from address/status output	⑤	t_DAD	15–6, etc.		0.5t_CYK−15		ns
Output setting time from $\overline{DSTB}\uparrow$	⑤	t_DLZ	15–6, etc.		0.5t_CYK−15		ns

★   **Notes**   1. These specifications apply to the following delay times from the falling edge of the CLKOUT signal.

      (1) Address delay time

      (2) $\overline{BUSLOCK}$ delay time

      (3) Delay time of signals below immediately after release of bus hold:

         A23-A0, D15-D0, M/$\overline{IO}$, BUSST1, BUSST0, $\overline{UBE}$, $\overline{BCYST}$, $\overline{DSTB}$.

   2. Control 1 applies to the $\overline{MWR}$ and $\overline{IOWR}$ signals in a DMA cycle.

   3. Control 2 applies to the $\overline{BUFEN}$, $\overline{INTAK}$ and $\overline{REFRQ}$ setups.

   4. n indicates the number of wait clock cycles inserted in the bus cycle. In a co-processor cycle, 1 (=TC cycle) must be added to n.

Remarks   1. The number in the symbol column correspond to the numbers in the timing charts.

   2. Regarding the five specifications ③② t_HRD, ③④ t_HRWD, ④① t_HDSD, ④② t_HASD, and ④⑥ t_HKD, at least one should be observed.

μPD70236A-10 (V_{DD} = 5 V ± 10 %)

μPD70236A-10 (V$_{DD}$ = 5 V ± 10 %)

PARAMETER	SYMBOL	FIG.No.	TEST CONDITIONS	T$_A$ = −40 to +85 °C MIN.	T$_A$ = −40 to +85 °C MAX.	UNIT
Data output delay time from CLKOUT↑	56 t$_{DKD}$	15–6, etc.		3	40	ns
Float delay time from CLKOUT	57 t$_{FK}$	15–6, etc.		0	35	ns
IORD delay time from CLKOUT	58 t$_{DKIR}$	15–7		0	40	ns
IOWR delay time from CLKOUT	59 t$_{DKIW}$	15–8		0	40	ns
NMI, INTPn (n = 0 to 7), CPBUSY setup time (to CLKOUT↓)	60 t$_{SIK}$	15–11		10		ns
NMI, INTPn(n = 0 to 7), CPBUSY hold time (from CLKOUT↓)	61 t$_{HKI}$	15–11		10		ns
BS8/BS16 setup time (to CLKOUT↑)	62 t$_{SBSK}$	15–13		10		ns
BS8/BS16 hold time (from CLKOUT↑)	63 t$_{HKBS}$	15–13		10		ns
HLDRQ setup time (to CLKOUT↑)	64 t$_{SHQK}$	15–14		10		ns
HLDRQ hold time (from CLKOUT↑)	65 t$_{HKHQ}$	15–14		15		ns
HLDAK delay time from CLKOUT↑	66 t$_{DKHA}$	15–14		3	40	ns
HLDAK delay time from output float	67 t$_{DFHA}$	15–14		0.5t$_{CYK}$−15		ns
INTPn(n = 0 to 7) low-level width	68 t$_{IPIPL}$	15–17		80		ns
TCTLn (n = 0 to 2) setup time (to CLKOUT↓)	69 t$_{SGK}$	15–18		40		ns
TCTLn (n = 0 to 2) hold time (from CLKOUT↓)	70 t$_{HKG}$	15–18		80		ns
TCTLn (n = 0 to 2) high-level width	71 t$_{GGH}$	15–18, etc.		40		ns
TCTLn (n = 0 to 2) low-level width	72 t$_{GGL}$	15–18, etc.		40		ns
TOUTn (n = 0 to 2) output delay time (from TCTLn(n = 0 to 2)↓)	73 t$_{DGTO}$	15–18, etc.			90	ns
TOUTn (n = 0 to 2) output delay time (from CLKOUT↓)	74 t$_{DKTO}$	15–18			50	ns
TCLK cycle	75 t$_{CYTK}$	15–19		100	DC	ns
TCLK high-level width	76 t$_{TKTKH}$	15–19		30		ns
TCLK low-level width	77 t$_{TKTKL}$	15–19		45		ns
TCLK rise time	78 t$_{TKR}$	15–19			15	ns
TCLK fall time	79 t$_{TKF}$	15–19			15	ns
TCTLn (n = 0 to 2) hold time (from TCLK↑)	80 t$_{HTKG}$	15–19		40		ns
TCTLn (n = 0 to 2) setup time (to TCLK↑)	81 t$_{SGTK}$	15–19		40		ns
TOUTn (n = 0 to 2) output delay time (from TCLK↓)	82 t$_{DTKTO}$	15–19			100	ns
RxD setup time (to SCU internal clock↓)	83 t$_{SRX}$	15–20		500		ns
RxD hold time (from SCU internal clock↓)	84 t$_{HRX}$	15–20		500		ns
TxD delay time from TOUT1↑	85 t$_{DTX}$	15–20			200	ns
DMAAKn (n = 0 to 3) delay time from CLKOUT↑	86 t$_{DKHDA}$	15–21		0	45	ns
MRD, IORD↓ delay time from CLKOUT↓	87 t$_{DKRL}$	15–21		0	45	ns
MRD, IORD↑ delay time from CLKOUT↓	88 t$_{DKRH}$	15–21		0	45	ns
DMAAKn (n = 0 to 3)↑ delay time (from IORD↑)	89 t$_{DRHDAH}$	15–21		0.5t$_{CYK}$−15		ns
IORD↓,IOWR↓ delay time (from DMAAKn (n = 0 to 3)↓)	90 t$_{DDARW}$	15–21		0.5t$_{CYK}$−15		ns

Remark The number in the symbol column correspond to the numbers in the timing charts.

μPD70236A-10 (V$_{DD}$ = 5 V ± 10 %)

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PARAMETER	SYMBOL	FIG.No.	TEST CONDITIONS	T$_A$ = −40 to +85 °C MIN.	MAX.	UNIT
$\overline{\text{IORD}}$↑ delay time (from $\overline{\text{MWR}}$↑) $\overline{\text{MRD}}$↑ delay time (from $\overline{\text{IOWR}}$↑)	⑨① t$_{DWHRH}$	15–21		0		ns
$\overline{\text{IORD}}$, $\overline{\text{MRD}}$ low-level width	⑨② t$_{RR}$	15–21		t$_{CYK}$(n+2)−40[Note 1]		ns
$\overline{\text{IOWR}}$, $\overline{\text{MWR}}$ low-level width (extended write)	⑨③ t$_{WW1}$	15–21	Extended write	t$_{CYK}$(n+2)−40[Note 1]		ns
$\overline{\text{IOWR}}$, $\overline{\text{MWR}}$ low-level width (normal write)	⑨④ t$_{WW2}$	15–21	Normal write	t$_{CYK}$(n+1)−40[Note 1]		ns
$\overline{\text{TC}}$ output delay time (from CLKOUT↑)	⑨⑤ t$_{DKTCL}$	15–22		0	40	ns
$\overline{\text{TC}}$ OFF output delay time (from CLKOUT↑)	⑨⑥ t$_{DKTCF}$	15–22		0	40	ns
$\overline{\text{TC}}$ pull-up delay time (from CLKOUT↑)[Note 2]	⑨⑦ t$_{DKTCH}$	15–22	R$_{TC}$ = 2.2 kΩ	0	2t$_{CYK}$−20	ns
$\overline{\text{TC}}$ low-level width	⑨⑧ t$_{TCTCL}$	15–22		t$_{CYK}$(n+1)−15[Note 1]		ns
$\overline{\text{END}}$ setup time (to CLKOUT↑)	⑨⑨ t$_{SEDK}$	15–22		20		ns
$\overline{\text{END}}$ low-level width	⑩⓪ t$_{EDEDL}$	15–22		100		ns
DMARQn (n = 0 to 3) setup time (to CLKOUT↑)	⑩① t$_{SDQK}$	15–22, etc.		20		ns
$\overline{\text{DMAAKn}}$ (n = 0 to 3) delay time from CLKOUT↓	⑩② t$_{DKLDA}$	15–23		0	40	ns
$\overline{\text{MRD}}$ high-level width	⑩③ t$_{MRMRH}$	15–5		0.5t$_{CYK}$−10		ns
Data set time from $\overline{\text{MRD}}$↑	⑩④ t$_{DMRHLZ}$	15–6, etc.		0.5t$_{CYK}$−15		ns
Data output delay time from $\overline{\text{MRD}}$↑	⑩⑤ t$_{DMRHD}$	15–6, etc.		0.5t$_{CYK}$−15		ns
Cascade address delay time from CLKOUT	⑩⑥ t$_{DKCA}$	15–15, etc.		2	35	ns
$\overline{\text{INTAK}}$ high-level width	⑩⑦ t$_{IAIAH}$	15–16		2.5t$_{CYK}$−10		ns
PCLKOUT delay time from CLKOUT	⑩⑧ t$_{DKPK}$	15–1	CLKC = 00		±5	ns
$\overline{\text{IOWR}}$, $\overline{\text{MWR}}$↓ delay time from $\overline{\text{MRD}}$, $\overline{\text{IORD}}$↓	⑩⑨ t$_{DRLWL}$	15–21	Normal write	t$_{CYK}$−15		ns

Notes 1. n indicates the number of wait clock cycles inserted in the bus cycle.
2. It is assumed that the $\overline{\text{TC}}$ pin is connected with the pull-up resistor R$_{TC}$.

Remark The number in the symbol column correspond to the numbers in the timing charts.

(2) µPD70236A-12 (V$_{DD}$ = 5 V ± 10 %)

(1/4)

PARAMETER	SYMBOL		FIG.No.	TEST CONDITIONS	T$_A$ = −40 to +85 °C		UNIT
					MIN.	MAX.	
External clock input cycle	①	t$_{CYX}$	15–1		40	250	ns
External clock input high-level width	②	t$_{XKH}$	15–1		13		ns
External clock input low-level width	③	t$_{XKL}$	15–1		13		ns
External clock input rise time	④	t$_{XKR}$	15–1			7	ns
External clock input fall time	⑤	t$_{XKF}$	15–1			7	ns
CPU operating frequency	–	f$_X$	–		2	12.5	MHz
CLKOUT output frequency	⑥	t$_{CYK}$	15–1		80	500	ns
CLKOUT high-level width	⑦	t$_{KKH}$	15–1		0.5t$_{CYK}$–10		ns
CLKOUT low-level width	⑧	t$_{KKL}$	15–1		0.5t$_{CYK}$–10		ns
CLKOUT rise time	⑨	t$_{KR}$	15–1	1.0 V → 3.5 V		10	ns
CLKOUT fall time	⑩	t$_{KF}$	15–1	3.5 V → 1.0 V		10	ns
CLKOUT delay time (from external clock)	⑪	t$_{DXK}$	15–1		4	30	ns
PCLKOUT output frequency	⑫	t$_{CYPK}$	15–1		4t$_{CYX}$	1000	ns
PCLKOUT high-level width	⑬	t$_{PKH}$	15–1		2t$_{CYX}$–10		ns
PCLKOUT low-level width	⑭	t$_{PKL}$	15–1		2t$_{CYX}$–10		ns
PCLKOUT output rise time	⑮	t$_{PKR}$	15–1	1.0 V → 3.5 V		10	ns
PCKLOUT output fall time	⑯	t$_{PKF}$	15–1	3.5 V → 1.0 V		10	ns
Input rise time[Note 1]	⑰	t$_{IR}$		0.8 V → 2.2 V		15	ns
Input fall time[Note 1]	⑱	t$_{IF}$		2.2 V → 0.8 V		10	ns
Output rise time[Note 2]	⑲	t$_{OR}$		0.8 V → 2.2 V		15	ns
Output fall time[Note 2]	⑳	t$_{OF}$		2.2 V → 0.8 V		10	ns
$\overline{RESET}$ setup time (to CLKOUT↓)	㉑	t$_{SRSTK}$	15–2		30		ns
$\overline{RESET}$ hold time (from CLKOUT↓)	㉒	t$_{HKRST}$	15–2		15		ns
RESOUT output delay time (from CLKOUT↓)	㉓	t$_{DKRO}$	15–2		0	40	ns
$\overline{RESET}$ low-level width	㉔	t$_{WRSTL}$	15–2		6t$_{CYK}$		ns
$\overline{READY}$ setup time (to CLKOUT↑)	㉕	t$_{SRYK}$	15–3, etc.		7		ns
$\overline{READY}$ hold time (from CLKOUT↑)	㉖	t$_{HKRY}$	15–3, etc.		15		ns
$\overline{BCYST}$ high-level width	㉗	t$_{BCBCH}$	15–5, etc.		t$_{CYK}$(n+1)–10[Note 3]		ns
$\overline{BCYST}$ low-level width	㉘	t$_{BCBCL}$	15–5, etc.		t$_{CYK}$–10		ns
$\overline{BCYST}$ delay time from CLKOUT↓	㉙	t$_{DKBC}$	15–5, etc.		3	30	ns
$\overline{MRD}$ delay time from CLKOUT	㉚	t$_{DKMR}$	15–5, etc.		0	35	ns

Notes 1. Except external clock and $\overline{RESET}$
 2. Except CLKOUT and PCLKOUT
 3. n indicates the number of wait clock cycles inserted in the bus cycle. In a co-processor cycle, 1 (=TC cycle) must be added to n.

Remark The number in the symbol column correspond to the numbers in the timing charts.

μPD70236A-12 (V_{DD} = 5 V ± 10 %)

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PARAMETER		SYMBOL	FIG.No.	TEST CONDITIONS	T_A = −40 to +85 °C		UNIT
					MIN.	MAX.	
$\overline{MRD}{\downarrow}$, $\overline{IORD}{\downarrow}$ delay time from address/status output	㉛	t_{DARL}	15–5, etc.		0.5t_{CYK}−15		ns
Data hold time (from $\overline{MRD}{\uparrow}$, from $\overline{IORD}{\uparrow}$)	㉜	t_{HRD}	15–5, etc.		0		ns
Address delay time from CLKOUT${\downarrow}$[Note 1]	㉝	t_{DKA}	15–5, etc.		2	30	ns
Data hold time (from R/$\overline{W}{\downarrow}$)	㉞	t_{HRWD}	15–5		0		ns
Status delay time from CLKOUT${\downarrow}$	㉟	t_{DKST}	15–5, etc.		3	30	ns
$\overline{DSTB}{\downarrow}$ output delay time from CLKOUT${\uparrow}$	㊱	t_{DKDS}	15–5, etc.		5	35	ns
$\overline{DSTB}{\uparrow}$ output delay time from CLKOUT	㊲	t_{DKDSH}	15–5, etc.		3	35	ns
$\overline{DSTB}{\downarrow}$ delay time from address/status output	㊳	t_{DADSL}	15–5, etc.		0.5t_{CYK}−15		ns
$\overline{DSTB}$ high-level width	㊴	t_{DSDSH}	15–5, etc.		0.5t_{CYK}−10		ns
$\overline{DSTB}$ low-level width	㊵	t_{DSDSL}	15–6, etc.		$t_{CYK}(n+1)$−10[Note 4]		ns
Data hold time (from $\overline{DSTB}{\uparrow}$)	㊶	t_{HDSD}	15–5, etc.		0		ns
Data hold time (from address/status change point)	㊷	t_{HASD}	15–5		0		ns
Control 1[Note 2] delay time from CLKOUT	㊸	t_{DKCT1}	15–21		0	35	ns
Control 2[Note 3] delay time from CLKOUT	㊹	t_{DKCT2}	15–5, etc.		0	35	ns
Data setup time (to CLKOUT${\downarrow}$)	㊺	t_{SDK}	15–5, etc.		7		ns
Data hold time (from CLKOUT${\downarrow}$)	㊻	t_{HKD}	15–5, etc.		7		ns
Output floating time from $\overline{DSTB}{\downarrow}$	㊼	t_{DHZ}	15–5, etc.			0	ns
Address/status hold time from $\overline{MWR}{\uparrow}$	㊽	t_{HMWHA}	15–6		0.5t_{CYK}−15		ns
$\overline{MWR}$ delay time from CLKOUT	㊾	t_{DKMW}	15–6, etc.		0	35	ns
$\overline{MWR}{\downarrow}$, $\overline{IOWR}{\downarrow}$ delay time from address/status output	㊿	t_{DAWL}	15–6, etc.		0.5t_{CYK}−15		ns
$\overline{MWR}$, $\overline{IOWR}$ low-level width	�51	t_{WWL}	15–6, etc.		$t_{CYK}(n+1)$−10[Note 4]		ns
Address/status hold time from $\overline{DSTB}{\uparrow}$	�52	t_{HDSHA}	15–6, etc.		0.5t_{CYK}−15		ns
Data output delay time from $\overline{DSTB}{\uparrow}$	�53	t_{DDSHD}	15–6, etc.		0.5t_{CYK}−15		ns
Data delay time from address/status output	�54	t_{DAD}	15–6, etc.		0.5t_{CYK}−15		ns
Output setting time from $\overline{DSTB}{\uparrow}$	�55	t_{DLZ}	15–6, etc.		0.5t_{CYK}−15		ns

* **Notes 1.** These specifications apply to the following delay times from the falling edge of the CLKOUT signal.

    (1) Address delay time

    (2) $\overline{BUSLOCK}$ delay time

    (3) Delay time of signals below immediately after release of bus hold:
        A23-A0, D15-D0, M/$\overline{IO}$, BUSST1, BUSST0, $\overline{UBE}$, $\overline{BCYST}$, $\overline{DSTB}$.

  2. Control 1 applies to the $\overline{MWR}$ and $\overline{IOWR}$ signals in a DMA cycle.

  3. Control 2 applies to the $\overline{BUFEN}$, $\overline{INTAK}$ and $\overline{REFRQ}$ setups.

  4. n indicates the number of wait clock cycles inserted in the bus cycle. In a co-processor cycle, 1 (=TC cycle) must be added to n.

Remarks 1. The number in the symbol column correspond to the numbers in the timing charts.

        2. Regarding the five specifications ㉜ t_{HRD}, ㉞ t_{HRWD}, ㊶ t_{HDSD}, ㊷ t_{HASD}, and ㊻ t_{HKD}, at least one should be observed.

μPD70236A-12 (V_{DD} = 5 V ± 10 %)

PARAMETER	SYMBOL		FIG.No.	TEST CONDITIONS	T_A = −40 to +85 °C		UNIT
					MIN.	MAX.	
Data output delay time from CLKOUT↑	⑤⑥	t_{DKD}	15–6, etc.		3	35	ns
Float delay time from CLKOUT	⑤⑦	t_{FK}	15–6, etc.		0	30	ns
IORD delay time from CLKOUT	⑤⑧	t_{DKIR}	15–7		0	35	ns
IOWR delay time from CLKOUT	⑤⑨	t_{DKIW}	15–8		0	35	ns
NMI, INTPn (n = 0 to 7), CPBUSY setup time (to CLKOUT↓)	⑥⓪	t_{SIK}	15–11		10		ns
NMI, INTPn (n = 0 to 7), CPBUSY hold time (from CLKOUT↓)	⑥①	t_{HKI}	15–11		10		ns
BS8/BS16 setup time (to CLKOUT↑)	⑥②	t_{SBSK}	15–13		10		ns
BS8/BS16 hold time (from CLKOUT↑)	⑥③	t_{HKBS}	15–13		10		ns
HLDRQ setup time (to CLKOUT↑)	⑥④	t_{SHQK}	15–14		10		ns
HLDRQ hold time (from CLKOUT↑)	⑥⑤	t_{HKHQ}	15–14		15		ns
HLDAK delay time from CLKOUT↑	⑥⑥	t_{DKHA}	15–14		3	35	ns
HLDAK delay time from output float	⑥⑦	t_{DFHA}	15–14		0.5t_{CYK}−15		ns
INTPn(n = 0 to 7) low-level width	⑥⑧	t_{IPIPL}	15–17		80		ns
TCTLn (n = 0 to 2) setup time (to CLKOUT↓)	⑥⑨	t_{SGK}	15–18		40		ns
TCTLn (n = 0 to 2) hold time (from CLKOUT↓)	⑦⓪	t_{HKG}	15–18		80		ns
TCTLn (n = 0 to 2) high-level width	⑦①	t_{GGH}	15–18, etc.		40		ns
TCTLn (n = 0 to 2) low-level width	⑦②	t_{GGL}	15–18, etc.		40		ns
TOUTn (n = 0 to 2) output delay time (from TCTLn(= 0 to 2)↓)	⑦③	t_{DGTO}	15–18, etc.			90	ns
TOUTn (n = 0 to 2) output delay time (from CLKOUT↓)	⑦④	t_{DKTO}	15–18			50	ns
TCLK cycle	⑦⑤	t_{CYTK}	15–19		80	DC	ns
TCLK high-level width	⑦⑥	t_{TKTKH}	15–19		30		ns
TCLK low-level width	⑦⑦	t_{TKTKL}	15–19		35		ns
TCLK rise time	⑦⑧	t_{TKR}	15–19			15	ns
TCLK fall time	⑦⑨	t_{TKF}	15–19			15	ns
TCTLn (n = 0 to 2) hold time (from TCLK↑)	⑧⓪	t_{HTKG}	15–19		40		ns
TCTLn (n = 0 to 2) setup time (to TCLK↑)	⑧①	t_{SGTK}	15–19		40		ns
TOUTn (n = 0 to 2) output delay time (from TCLK↓)	⑧②	t_{DTKTO}	15–19			100	ns
RxD setup time (to SCU internal clock↓)	⑧③	t_{SRX}	15–20		500		ns
RxD hold time (from SCU internal clock↓)	⑧④	t_{HRX}	15–20		500		ns
TxD delay time from TOUT1↑	⑧⑤	t_{DTX}	15–20			200	ns
DMAAKn (n = 0 to 3) delay time from CLKOUT↑	⑧⑥	t_{DKHDA}	15–21		0	40	ns
MRD, IORD↓ delay time from CLKOUT↓	⑧⑦	t_{DKRL}	15–21		0	40	ns
MRD, IORD↑ delay time from CLKOUT↓	⑧⑧	t_{DKRH}	15–21		0	40	ns
DMAAKn (n = 0 to 3)↑ delay time (from IORD↑)	⑧⑨	t_{DRHDAH}	15–21		0.5t_{CYK}−15		ns
IORD↓,IOWR↓ delay time (from DMAAKn (n = 0 to 3)↓)	⑨⓪	t_{DDARW}	15–21		0.5t_{CYK}−15		ns

Remark The number in the symbol column correspond to the numbers in the timing charts.

µPD70236A-12 (V_DD = 5 V ± 10 %)

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PARAMETER	SYMBOL		FIG.No.	TEST CONDITIONS	T_A = −40 to +85 °C		UNIT
					MIN.	MAX.	
IORD↑ delay time (from MWR↑) / MRD↑ delay time (from IOWR↑)	⑨①	t_DWHRH	15–21		0		ns
IORD, MRD low-level width	⑨②	t_RR	15–21		t_CYK(n+2)−35[Note 1]		ns
IOWR, MWR low-level width (extended write)	⑨③	t_WW1	15–21	Extended write	t_CYK(n+2)−35[Note 1]		ns
IOWR, MWR low-level width (normal write)	⑨④	t_WW2	15–21	Normal write	t_CYK(n+1)−35[Note 1]		ns
TC output delay time (from CLKOUT↑)	⑨⑤	t_DKTCL	15–22		0	35	ns
TC OFF output delay time (from CLKOUT↑)	⑨⑥	t_DKTCF	15–22		0	35	ns
TC pull-up delay time (from CLKOUT↑)[Note 2]	⑨⑦	t_DKTCH	15–22	R_TC = 1.1 kΩ	0	2t_CYK−10	ns
TC low-level width	⑨⑧	t_TCTCL	15–22		t_CYK(n+1)−15[Note 1]		ns
END setup time (to CLKOUT↑)	⑨⑨	t_SEDK	15–22		10		ns
END low-level width	⑩⓪	t_EDEDL	15–22		100		ns
DMARQn (n = 0 to 3) setup time (to CLKOUT↑)	⑩①	t_SDQK	15–22, etc.		15		ns
DMAAKn (n = 0 to 3) delay time from CLKOUT↓	⑩②	t_DKLDA	15–23		0	35	ns
MRD high-level width	⑩③	t_MRMRH	15–5		0.5t_CYK−10		ns
Data set time from MRD↑	⑩④	t_DMRHLZ	15–6, etc.		0.5t_CYK−15		ns
Data output delay time from MRD↑	⑩⑤	t_DMRHD	15–6, etc.		0.5t_CYK−15		ns
Cascade address delay time from CLKOUT	⑩⑥	t_DKCA	15–15, etc.		2	30	ns
INTAK high-level width	⑩⑦	t_IAIAH	15–16		2.5t_CYK−10		ns
PCLKOUT delay time from CLKOUT	⑩⑧	t_DKPK	15–1	CLKC = 00		±5	ns
IOWR, MWR↓ delay time from MRD, IORD↓	⑩⑨	t_DRLWL	15–21	Normal write	t_CYK−15		ns

Notes 1. n indicates the number of wait clock cycles inserted in the bus cycle.
2. It is assumed that the TC pin is connected with the pull-up resistor R_TC.

Remark The number in the symbol column correspond to the numbers in the timing charts.

(3) μPD70236A-16 (V_{DD} = 5 V ± 10 %)   (1/4)

PARAMETER	SYMBOL		FIG.No.	TEST CONDITIONS	T_A = −40 to +85 °C		T_A = −10 to +70 °C		UNIT
					MIN.	MAX.	MIN.	MAX.	
External clock input cycle	①	t_{CYX}	15–1		31.25	250	31.25	250	ns
External clock input high-level width	②	t_{XKH}	15–1		8		8		ns
External clock input low-level width	③	t_{XKL}	15–1		8		8		ns
External clock input rise time	④	t_{XKR}	15–1			7		7	ns
External clock input fall time	⑤	t_{XKF}	15–1			7		7	ns
CPU operating frequency	–	f_X	–		2	16	2	16	MHz
CLKOUT output frequency	⑥	t_{CYK}	15–1		62.5	500	62.5	500	ns
CLKOUT high-level width	⑦	t_{KKH}	15–1		0.5t_{CYK}−7		0.5t_{CYK}−7		ns
CLKOUT low-level width	⑧	t_{KKL}	15–1		0.5t_{CYK}−7		0.5t_{CYK}−7		ns
CLKOUT rise time	⑨	t_{KR}	15–1	1.0 V → 3.5 V		7		7	ns
CLKOUT fall time	⑩	t_{KF}	15–1	3.5 V → 1.0 V		7		7	ns
CLKOUT delay time (from external clock)	⑪	t_{DXK}	15–1		4	30	5	30	ns
PCLKOUT output frequency	⑫	t_{CYPK}	15–1		4t_{CYX}	1000	4t_{CYX}	1000	ns
PCLKOUT high-level width	⑬	t_{PKH}	15–1		2t_{CYX}−7		2t_{CYX}−7		ns
PCLKOUT low-level width	⑭	t_{PKL}	15–1		2t_{CYX}−7		2t_{CYX}−7		ns
PCLKOUT output rise time	⑮	t_{PKR}	15–1	1.0 V → 3.5 V		7		7	ns
PCKLOUT output fall time	⑯	t_{PKF}	15–1	3.5 V → 1.0 V		7		7	ns
Input rise time[Note 1]	⑰	t_{IR}		0.8 V → 2.2 V		12		12	ns
Input fall time[Note 1]	⑱	t_{IF}		2.2 V → 0.8 V		10		10	ns
Output rise time[Note 2]	⑲	t_{OR}		0.8 V → 2.2 V		12		12	ns
Output fall time[Note 2]	⑳	t_{OF}		2.2 V → 0.8 V		10		10	ns
RESET setup time (to CLKOUT↓)	㉑	t_{SRSTK}	15–2		30		25		ns
RESET hold time (from CLKOUT↓)	㉒	t_{HKRST}	15–2		15		12		ns
RESOUT output delay time (from CLKOUT↓)	㉓	t_{DKRO}	15–2		0	40	0	40	ns
RESET low-level width	㉔	t_{WRSTL}	15–2		6t_{CYK}		6t_{CYK}		ns
READY setup time (to CLKOUT↑)	㉕	t_{SRYK}	15–3, etc.		5		5		ns
READY hold time (from CLKOUT↑)	㉖	t_{HKRY}	15–3, etc.		12		12		ns
BCYST high-level width	㉗	t_{BCBCH}	15–5, etc.		t_{CYK}(n+1)−10[Note 3]		t_{CYK}(n+1)−10[Note 3]		ns
BCYST low-level width	㉘	t_{BCBCL}	15–5, etc.		t_{CYK}−10		t_{CYK}−10		ns
BCYST delay time from CLKOUT↓	㉙	t_{DKBC}	15–5, etc.		3	30	4	25	ns
MRD delay time from CLKOUT	㉚	t_{DKMR}	15–5, etc.		0	35	0	25	ns

Notes 1. Except external clock and RESET
         2. Except CLKOUT and PCLKOUT
         3. n indicates the number of wait clock cycles inserted in the bus cycle. In a co-processor cycle, 1 (=TC cycle) must be added to n.

Remark The number in the symbol column correspond to the numbers in the timing charts.

µPD70236A-16 (V$_{DD}$ = 5 V ± 10 %)

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PARAMETER	SYMBOL	FIG.No.	TEST CONDITIONS	T$_A$ = −40 to +85 °C MIN.	T$_A$ = −40 to +85 °C MAX.	T$_A$ = −10 to +70 °C MIN.	T$_A$ = −10 to +70 °C MAX.	UNIT
MRD↓, IORD↓ delay time from address/status output	③① t$_{DARL}$	15–5, etc.		0.5tcYK−15		0.5tcYK−15		ns
Data hold time (from MRD↑, from IORD↑)	③② t$_{HRD}$	15–5, etc.		0		0		ns
Address delay time from CLKOUT↓[Note 1]	③③ t$_{DKA}$	15–5, etc.		2	30	3	20	ns
Data hold time (from R/W↓)	③④ t$_{HRWD}$	15–5		0		0		ns
Status delay time from CLKOUT↓	③⑤ t$_{DKST}$	15–5, etc.		3	30	4	20	ns
DSTB↓ output delay time from CLKOUT↑	③⑥ t$_{DKDS}$	15–5, etc.		5	35	5	30	ns
DSTB↑ output delay time from CLKOUT	③⑦ t$_{DKDSH}$	15–5, etc.		3	35	4	25	ns
DSTB↓ delay time from address/status output	③⑧ t$_{DADSL}$	15–5, etc.		0.5tcYK−15		0.5tcYK−15		ns
DSTB high-level width	③⑨ t$_{DSDSH}$	15–5, etc.		0.5tcYK−10		0.5tcYK−10		ns
DSTB low-level width	④⓪ t$_{DSDSL}$	15–6, etc.		tcYK(n+1)−10[Note 4]		tcYK(n+1)−10[Note 4]		ns
Data hold time (from DSTB↑)	④① t$_{HDSD}$	15–5, etc.		0		0		ns
Data hold time (from address/status change point)	④② t$_{HASD}$	15–5		0		0		ns
Control 1[Note 2] delay time from CLKOUT	④③ t$_{DKCT1}$	15–21		0	35	0	25	ns
Control 2[Note 3] delay time from CLKOUT	④④ t$_{DKCT2}$	15–5, etc.		0	35	0	30	ns
Data setup time (to CLKOUT↓)	④⑤ t$_{SDK}$	15–5, etc.		7		7		ns
Data hold time (from CLKOUT↓)	④⑥ t$_{HKD}$	15–5, etc.		7		7		ns
Output floating time from DSTB↓	④⑦ t$_{DHZ}$	15–5, etc.			0		0	ns
Address/status hold time from MWR↑	④⑧ t$_{HMWHA}$	15–6		0.5tcYK−15		0.5tcYK−15		ns
MWR delay time from CLKOUT	④⑨ t$_{DKMW}$	15–6, etc.		0	35	0	30	ns
MWR↓, IOWR↓ delay time from address/status output	⑤⓪ t$_{DAWL}$	15–6, etc.		0.5tcYK−15		0.5tcYK−15		ns
MWR, IOWR low-level width	⑤① t$_{WWL}$	15–6, etc.		tcYK(n+1)−10[Note 4]		tcYK(n+1)−10[Note 4]		ns
Address/status hold time from DSTB↑	⑤② t$_{HDSHA}$	15–6, etc.		0.5tcYK−15		0.5tcYK−15		ns
Data output delay time from DSTB↑	⑤③ t$_{DDSHD}$	15–6, etc.		0.5tcYK−15		0.5tcYK−15		ns
Data delay time from address/status output	⑤④ t$_{DAD}$	15–6, etc.		0.5tcYK−15		0.5tcYK−15		ns
Output setting time from DSTB↑	⑤⑤ t$_{DLZ}$	15–6, etc.		0.5tcYK−15		0.5tcYK−15		ns

★ **Notes** 1. These specifications apply to the following delay times from the falling edge of the CLKOUT signal.
     (1) Address delay time
     (2) BUSLOCK delay time
     (3) Delay time of signals below immediately after release of bus hold:
         A23-A0, D15-D0, M/IO, BUSST1, BUSST0, UBE, BCYST, DSTB.
    2. Control 1 applies to the MWR and IOWR signals in a DMA cycle.
    3. Control 2 applies to the BUFEN, INTAK and REFRQ setups.
    4. n indicates the number of wait clock cycles inserted in the bus cycle. In a co-processor cycle, 1 (=TC cycle) must be added to n.

Remarks 1. The number in the symbol column correspond to the numbers in the timing charts.
    2. Regarding the five specifications ③② t$_{HRD}$, ③④ t$_{HRWD}$, ④① t$_{HDSD}$, ④② t$_{HASD}$, and ④⑥ t$_{HKD}$, at least one should be observed.

μPD70236A-16 (V_DD = 5 V ± 10 %)

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PARAMETER	SYMBOL		FIG.No.	TEST CONDITIONS	T_A = −40 to +85 °C		T_A = −10 to +70 °C		UNIT
					MIN.	MAX.	MIN.	MAX.	
Data output delay time from CLKOUT↑	⑤⑥	t_DKD	15–6, etc.		3	35	4	30	ns
Float delay time from CLKOUT	⑤⑦	t_FK	15–6, etc.		0	30	0	25	ns
IORD delay time from CLKOUT	⑤⑧	t_DKIR	15–7		0	35	0	25	ns
IOWR delay time from CLKOUT	⑤⑨	t_DKIW	15–8		0	35	0	30	ns
NMI, INTPn (n = 0 to 7), CPBUSY setup time (to CLKOUT↓)	⑥⓪	t_SIK	15–11		7		7		ns
NMI, INTPn(n = 0 to 7), CPBUSY hold time (from CLKOUT↓)	⑥①	t_HKI	15–11		7		7		ns
BS8/BS16 setup time (to CLKOUT↑)	⑥②	t_SBSK	15–13		7		7		ns
BS8/BS16 hold time (from CLKOUT↑)	⑥③	t_HKBS	15–13		7		7		ns
HLDRQ setup time (to CLKOUT↑)	⑥④	t_SHQK	15–14		7		7		ns
HLDRQ hold time (from CLKOUT↑)	⑥⑤	t_HKHQ	15–14		10		10		ns
HLDAK delay time from CLKOUT↑	⑥⑥	t_DKHA	15–14		3	35	4	25	ns
HLDAK delay time from output float	⑥⑦	t_DFHA	15–14		0.5t_CYK−15		0.5t_CYK−15		ns
INTPn(n = 0 to 7) low-level width	⑥⑧	t_IPIPL	15–17		80		80		ns
TCTLn (n = 0 to 2) setup time (to CLKOUT↓)	⑥⑨	t_SGK	15–18		40		40		ns
TCTLn (n = 0 to 2) hold time (from CLKOUT↓)	⑦⓪	t_HKG	15–18		80		80		ns
TCTLn (n = 0 to 2) high-level width	⑦①	t_GGH	15–18, etc.		40		40		ns
TCTLn (n = 0 to 2) low-level width	⑦②	t_GGL	15–18, etc.		40		40		ns
TOUTn (n = 0 to 2) output delay time (from TCTLn (n = 0 to 2)↓)	⑦③	t_DGTO	15–18, etc.			90		90	ns
TOUTn (n = 0 to 2) output delay time (from CLKOUT↓)	⑦④	t_DKTO	15–18			50		50	ns
TCLK cycle	⑦⑤	t_CYTK	15–19		62.5	DC	62.5	DC	ns
TCLK high-level width	⑦⑥	t_TKTKH	15–19		25		25		ns
TCLK low-level width	⑦⑦	t_TKTKL	15–19		30		30		ns
TCLK rise time	⑦⑧	t_TKR	15–19			15		15	ns
TCLK fall time	⑦⑨	t_TKF	15–19			15		15	ns
TCTLn (n = 0 to 2) hold time (from TCLK↑)	⑧⓪	t_HTKG	15–19		40		40		ns
TCTLn (n = 0 to 2) setup time (to TCLK↑)	⑧①	t_SGTK	15–19		40		40		ns
TOUTn (n = 0 to 2) output delay time (from TCLK↓)	⑧②	t_DTKTO	15–19			100		100	ns
RxD setup time (to SCU internal clock↓)	⑧③	t_SRX	15–20		500		500		ns
RxD hold time (from SCU internal clock↓)	⑧④	t_HRX	15–20		500		500		ns
TxD delay time from TOUT1↑	⑧⑤	t_DTX	15–20			200		200	ns
DMAAKn (n = 0 to 3) delay time from CLKOUT↑	⑧⑥	t_DKHDA	15–21		0	40	0	35	ns
MRD, IORD↓ delay time from CLKOUT↓	⑧⑦	t_DKRL	15–21		0	40	0	35	ns
MRD, IORD↑ delay time from CLKOUT↓	⑧⑧	t_DKRH	15–21		0	40	0	35	ns
DMAAKn (n = 0 to 3)↑ delay time (from IORD↑)	⑧⑨	t_DRHDAH	15–21		0.5t_CYK−15		0.5t_CYK−15		ns
IORD↓,IOWR↓ delay time (from DMAAKn (n = 0 to 3)↓)	⑨⓪	t_DDARW	15–21		0.5t_CYK−15		0.5t_CYK−15		ns

Remark The number in the symbol column correspond to the numbers in the timing charts.

μPD70236A-16 (V_DD = 5 V ± 10 %)

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PARAMETER	SYMBOL	FIG.No.	TEST CONDITIONS	T_A = −40 to +85 °C MIN.	MAX.	T_A = −10 to +70 °C MIN.	MAX.	UNIT
IORD↑ delay time (from MWR↑) MRD↑ delay time (from IOWR↑)	⑨ tDWHRH	15–21		0		0		ns
IORD, MRD low-level width	⑫ tRR	15–21		$t_{CYK}(n+2)-35$[1]		$t_{CYK}(n+2)-25$[1]		ns
IOWR, MWR low-level width (extended write)	⑬ tWW1	15–21	Extended write	$t_{CYK}(n+2)-35$[1]		$t_{CYK}(n+2)-25$[1]		ns
IOWR, MWR low-level width (normal write)	⑭ tWW2	15–21	Normal write	$t_{CYK}(n+1)-35$[1]		$t_{CYK}(n+1)-25$[1]		ns
TC output delay time (from CLKOUT↑)	⑮ tDKTCL	15–22		0	35	0	25	ns
TC OFF output delay time (from CLKOUT↑)	⑯ tDKTCF	15–22		0	35	0	25	ns
TC pull-up delay time (from CLKOUT↑)[Note 2]	⑰ tDKTCH	15–22	RTC = 1.1 kΩ	0	$2t_{CYK}-10$	0	$2t_{CYK}-10$	ns
TC low-level width	⑱ tTCTCL	15–22		$t_{CYK}(n+1)-15$[1]		$t_{CYK}(n+1)-15$[1]		ns
END setup time (to CLKOUT↑)	⑲ tSEDK	15–22		10		10		ns
END low-level width	⑩⑩ tEDEDL	15–22		100		100		ns
DMARQn (n = 0 to 3) setup time (to CLKOUT↑)	⑩① tSDQK	15–22, etc.		12		12		ns
DMAAKn (n = 0 to 3) delay time from CLKOUT↓	⑩② tDKLDA	15–23		0	35	0	25	ns
MRD high-level width	⑩③ tMRMRH	15–5		$0.5t_{CYK}-10$		$0.5t_{CYK}-10$		ns
Data set time from MRD↑	⑩④ tDMRHLZ	15–6, etc.		$0.5t_{CYK}-15$		$0.5t_{CYK}-15$		ns
Data output delay time from MRD↑	⑩⑤ tDMRHD	15–6, etc.		$0.5t_{CYK}-15$		$0.5t_{CYK}-15$		ns
Cascade address delay time from CLKOUT	⑩⑥ tDKCA	15–15, etc.		2	30	3	20	ns
INTAK high-level width	⑩⑦ tIAIAH	15–16		$2.5t_{CYK}-10$		$2.5t_{CYK}-10$		ns
PCLKOUT delay time from CLKOUT	⑩⑧ tDKPK	15–1	CLKC = 00		±5		±5	ns
IOWR, MWR↓ delay time from MRD, IORD↓	⑩⑨ tDRLWL	15–21	Normal write	$t_{CYK}-15$		$t_{CYK}-15$		ns

Notes 1. n indicates the number of wait clock cycles inserted in the bus cycle.
2. It is assumed that the TC pin is connected with the pull-up resistor RTC.

Remark The number in the symbol column correspond to the numbers in the timing charts.

(4) μPD70236A-20 (V_DD = 5 V ± 10 %)   (1/4)

PARAMETER	SYMBOL		FIG.No.	TEST CONDITIONS	T_A = −40 to +85 °C		T_A = −10 to +70 °C		UNIT
					MIN.	MAX.	MIN.	MAX.	
External clock input cycle	①	t_CYX	15–1		25	250	25	250	ns
External clock input high-level width	②	t_XKH	15–1		8		8		ns
External clock input low-level width	③	t_XKL	15–1		8		8		ns
External clock input rise time	④	t_XKR	15–1			7		7	ns
External clock input fall time	⑤	t_XKF	15–1			7		7	ns
CPU operating frequency	–	f_X	–		2	20	2	20	MHz
CLKOUT output frequency	⑥	t_CYK	15–1		50	500	50	500	ns
CLKOUT high-level width	⑦	t_KKH	15–1		0.5t_CYK−5		0.5t_CYK−5		ns
CLKOUT low-level width	⑧	t_KKL	15–1		0.5t_CYK−5		0.5t_CYK−5		ns
CLKOUT rise time	⑨	t_KR	15–1	1.0 V → 3.5 V		5		5	ns
CLKOUT fall time	⑩	t_KF	15–1	3.5 V → 1.0 V		5		5	ns
CLKOUT delay time (from external clock)	⑪	t_DXK	15–1		4	30	5	30	ns
PCLKOUT output frequency	⑫	t_CYPK	15–1		4t_CYX	1000	4t_CYX	1000	ns
PCLKOUT high-level width	⑬	t_PKH	15–1		2t_CYX−5		2t_CYX−5		ns
PCLKOUT low-level width	⑭	t_PKL	15–1		2t_CYX−5		2t_CYX−5		ns
PCLKOUT output rise time	⑮	t_PKR	15–1	1.0 V → 3.5 V		5		5	ns
PCKLOUT output fall time	⑯	t_PKF	15–1	3.5 V → 1.0 V		5		5	ns
Input rise time[Note 1]	⑰	t_IR		0.8 V → 2.2 V		10		10	ns
Input fall time[Note 1]	⑱	t_IF		2.2 V → 0.8 V		10		10	ns
Output rise time[Note 2]	⑲	t_OR		0.8 V → 2.2 V		10		10	ns
Output fall time[Note 2]	⑳	t_OF		2.2 V → 0.8 V		10		10	ns
RESET setup time (to CLKOUT↓)	㉑	t_SRSTK	15–2		30		25		ns
RESET hold time (from CLKOUT↓)	㉒	t_HKRST	15–2		15		12		ns
RESOUT output delay time (from CLKOUT↓)	㉓	t_DKRO	15–2		0	40	0	40	ns
RESET low-level width	㉔	t_WRSTL	15–2		6t_CYK		6t_CYK		ns
READY setup time (to CLKOUT↑)	㉕	t_SRYK	15–3, etc.		5		5		ns
READY hold time (from CLKOUT↑)	㉖	t_HKRY	15–3, etc.		12		12		ns
BCYST high-level width	㉗	t_BCBCH	15–5, etc.		t_CYK(n+1)−7[Note 3]		t_CYK(n+1)−7[Note 3]		ns
BCYST low-level width	㉘	t_BCBCL	15–5, etc.		t_CYK−7		t_CYK−7		ns
BCYST delay time from CLKOUT↓	㉙	t_DKBC	15–5, etc.		3	30	4	25	ns
MRD delay time from CLKOUT	㉚	t_DKMR	15–5, etc.		0	35	0	25	ns

Notes 1. Except external clock and RESET
      2. Except CLKOUT and PCLKOUT
      3. n indicates the number of wait clock cycles inserted in the bus cycle. In a co-processor cycle, 1 (=TC cycle) must be added to n.

Remark The number in the symbol column correspond to the numbers in the timing charts.

μPD70236A-20 (V$_{DD}$ = 5 V ± 10 %)

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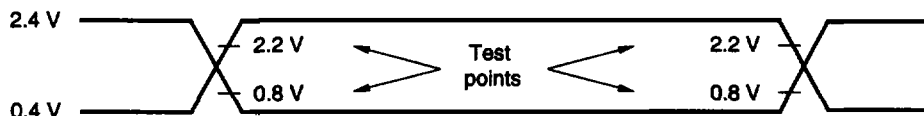| PARAMETER	SYMBOL	FIG.No.	TEST CONDITIONS	T$_A$ = −40 to +85 °C		T$_A$ = −10 to +70 °C		UNIT
				MIN.	MAX.	MIN.	MAX.	
MRD↓, IORD↓ delay time from address/status output	㉛ t$_{DARL}$	15-5, etc.		0.5tcYK−12		0.5tcYK−12		ns
Data hold time (from MRD↑, from IORD↑)	㉜ t$_{HRD}$	15-5, etc.		0		0		ns
Address delay time from CLKOUT↓ Note 1	�33 t$_{DKA}$	15-5, etc.		2	30	3	20	ns
Data hold time (from R/W↓)	�34 t$_{HRWD}$	15-5		0		0		ns
Status delay time from CLKOUT↓	�35 t$_{DKST}$	15-5, etc.		3	30	4	20	ns
DSTB↓ output delay time from CLKOUT↑	�36 t$_{DKDS}$	15-5, etc.		5	35	5	30	ns
DSTB↑ output delay time from CLKOUT	�37 t$_{DKDSH}$	15-5, etc.		3	35	4	25	ns
DSTB↓ delay time from address/status output	�38 t$_{DADSL}$	15-5, etc.		0.5tcYK−12		0.5tcYK−12		ns
DSTB high-level width	�39 t$_{DSDSH}$	15-5, etc.		0.5tcYK−7		0.5tcYK−7		ns
DSTB low-level width	㊵ t$_{DSDSL}$	15-6, etc.		tcYK(n+1)−7 Note 4		tcYK(n+1)−7 Note 4		ns
Data hold time (from DSTB↑)	㊶ t$_{HDSD}$	15-5, etc.		0		0		ns
Data hold time (from address/status change point)	㊷ t$_{HASD}$	15-5		0		0		ns
Control 1 Note 2 delay time from CLKOUT	㊸ t$_{DKCT1}$	15-21		0	35	0	25	ns
Control 2 Note 3 delay time from CLKOUT	㊹ t$_{DKCT2}$	15-5, etc.		0	35	0	30	ns
Data setup time (to CLKOUT↓)	㊺ t$_{SDK}$	15-5, etc.		7		7		ns
Data hold time (from CLKOUT↓)	㊻ t$_{HKD}$	15-5, etc.		7		7		ns
Output floating time from DSTB↓	㊼ t$_{DHZ}$	15-5, etc.			0		0	ns
Address/status hold time from MWR↑	㊽ t$_{HMWHA}$	15-6		0.5tcYK−12		0.5tcYK−12		ns
MWR delay time from CLKOUT	㊾ t$_{DKMW}$	15-6, etc.		0	35	0	30	ns
MWR↓, IOWR↓ delay time from address/status output	㊿ t$_{DAWL}$	15-6, etc.		0.5tcYK−12		0.5tcYK−12		ns
MWR, IOWR low-level width	�51 t$_{WWL}$	15-6, etc.		tcYK(n+1)−7 Note 4		tcYK(n+1)−7 Note 4		ns
Address/status hold time from DSTB↑	�52 t$_{HDSHA}$	15-6, etc.		0.5tcYK−12		0.5tcYK−12		ns
Data output delay time from DSTB↑	�53 t$_{DDSHD}$	15-6, etc.		0.5tcYK−12		0.5tcYK−12		ns
Data delay time from address/status output	�54 t$_{DAD}$	15-6, etc.		0.5tcYK−12		0.5tcYK−12		ns
Output setting time from DSTB↑	�55 t$_{DLZ}$	15-6, etc.		0.5tcYK−12		0.5tcYK−12		ns

* **Notes** 1. These specifications apply to the following delay times from the falling edge of the CLKOUT signal.
   (1) Address delay time
   (2) BUSLOCK delay time
   (3) Delay time of signals below immediately after release of bus hold:
      A23-A0, D15-D0, M/IO, BUSST1, BUSST0, UBE, BCYST, DSTB.
2. Control 1 applies to the MWR and IOWR signals in a DMA cycle.
3. Control 2 applies to the BUFEN, INTAK and REFRQ setups.
4. n indicates the number of wait clock cycles inserted in the bus cycle. In a co-processor cycle, 1 (=TC cycle) must be added to n.

Remarks 1. The number in the symbol column correspond to the numbers in the timing charts.
2. Regarding the five specifications ㉜ t$_{HRD}$, �34 t$_{HRWD}$, ㊶ t$_{HDSD}$, ㊷ t$_{HASD}$, and ㊻ t$_{HKD}$, at least one should be observed.

µPD70236A-20 (V_DD = 5 V ± 10 %)

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PARAMETER	SYMBOL	FIG.No.	TEST CONDITIONS	T_A = −40 to +85 °C		T_A = −10 to +70 °C		UNIT
				MIN.	MAX.	MIN.	MAX.	
Data output delay time from CLKOUT↑	㉟	t_DKD	15–6, etc.		3	35	4	30	ns
Float delay time from CLKOUT	㉝	t_FK	15–6, etc.		0	30	0	25	ns
IORD delay time from CLKOUT	㉟	t_DKIR	15–7		0	35	0	25	ns
IOWR delay time from CLKOUT	㉟	t_DKIW	15–8		0	35	0	30	ns
NMI, INTPn (n = 0 to 7), CPBUSY setup time (to CLKOUT↓)	㉠	t_SIK	15–11		7		7		ns
NMI, INTPn(n = 0 to 7), CPBUSY hold time (from CLKOUT↓)	㉑	t_HKI	15–11		7		7		ns
BS8/BS16 setup time (to CLKOUT↑)	㉒	t_SBSK	15–13		7		7		ns
BS8/BS16 hold time (from CLKOUT↑)	㉓	t_HKBS	15–13		7		7		ns
HLDRQ setup time (to CLKOUT↑)	㉔	t_SHQK	15–14		7		7		ns
HLDRQ hold time (from CLKOUT↑)	㉕	t_HKHQ	15–14		10		10		ns
HLDAK delay time from CLKOUT↑	㉖	t_DKHA	15–14		3	35	4	25	ns
HLDAK delay time from output float	㉗	t_DFHA	15–14		0.5t_CYK−15		0.5t_CYK−15		ns
INTPn (n = 0 to 7) low-level width	㉘	t_IPIPL	15–17		80		80		ns
TCTLn (n = 0 to 2) setup time (to CLKOUT↓)	㉙	t_SGK	15–18		40		40		ns
TCTLn (n = 0 to 2) hold time (from CLKOUT↓)	㉚	t_HKG	15–18		80		80		ns
TCTLn (n = 0 to 2) high-level width	㉛	t_GGH	15–18, etc.		40		40		ns
TCTLn (n = 0 to 2) low-level width	㉜	t_GGL	15–18, etc.		40		40		ns
TOUTn (n = 0 to 2) output delay time (from TCTLn (n = 0 to 2)↓)	㉝	t_DGTO	15–18, etc.			90		90	ns
TOUTn (n = 0 to 2) output delay time (from CLKOUT↓)	㉞	t_DKTO	15–18			50		50	ns
TCLK cycle	㉟	t_CYTK	15–19		50	DC	50	DC	ns
TCLK high-level width	㊱	t_TKTKH	15–19		20		20		ns
TCLK low-level width	㊲	t_TKTKL	15–19		25		25		ns
TCLK rise time	㊳	t_TKR	15–19			15		15	ns
TCLK fall time	㊴	t_TKF	15–19			15		15	ns
TCTLn (n = 0 to 2) hold time (from TCLK↑)	㊵	t_HTKG	15–19		40		40		ns
TCTLn (n = 0 to 2) setup time (to TCLK↑)	㊶	t_SGTK	15–19		40		40		ns
TOUTn (n = 0 to 2) output delay time (from TCLK↓)	㊷	t_DTKTO	15–19			100		100	ns
RxD setup time (to SCU internal clock↓)	㊸	t_SRX	15–20		500		500		ns
RxD hold time (from SCU internal clock↓)	㊹	t_HRX	15–20		500		500		ns
TxD delay time from TOUT1↑	㊺	t_DTX	15–20			200		200	ns
DMAAKn (n = 0 to 3) delay time from CLKOUT↑	㊻	t_DKHDA	15–21		0	40	0	35	ns
MRD, IORD↓ delay time from CLKOUT↓	㊼	t_DKRL	15–21		0	40	0	35	ns
MRD, IORD↑ delay time from CLKOUT↓	㊽	t_DKRH	15–21		0	40	0	35	ns
DMAAKn (n = 0 to 3)↑ delay time (from IORD↑)	㊾	t_DRHDAH	15–21		0.5t_CYK−12		0.5t_CYK−12		ns
IORD↓,IOWR↓ delay time (from DMAAKn (n = 0 to 3)↓)	㊿	t_DDARW	15–21		0.5t_CYK−12		0.5t_CYK−12		ns

Remark The number in the symbol column correspond to the numbers in the timing charts.

μPD70236A-20 (V_DD = 5 V ± 10 %)   (4/4)

PARAMETER	SYMBOL	FIG.No.	TEST CONDITIONS	T_A = −40 to +85 °C		T_A = −10 to +70 °C		UNIT
				MIN.	MAX.	MIN.	MAX.	
$\overline{\text{IORD}}$↑ delay time (from $\overline{\text{MWR}}$↑) $\overline{\text{MRD}}$↑ delay time (from $\overline{\text{IOWR}}$↑)	⑨① t_DWHRH	15–21		0		0		ns
$\overline{\text{IORD}}$, $\overline{\text{MRD}}$ low-level width	⑨② t_RR	15–21		t_CYK(n+2)–35[Note1]		t_CYK(n+2)–25[Note1]		ns
$\overline{\text{IOWR}}$, $\overline{\text{MWR}}$ low-level width (extended write)	⑨③ t_WW1	15–21	Extended write	t_CYK(n+2)–35[Note1]		t_CYK(n+2)–25[Note1]		ns
$\overline{\text{IOWR}}$, $\overline{\text{MWR}}$ low-level width (normal write)	⑨④ t_WW2	15–21	Normal write	t_CYK(n+1)–35[Note1]		t_CYK(n+1)–25[Note1]		ns
$\overline{\text{TC}}$ output delay time (from CLKOUT↑)	⑨⑤ t_DKTCL	15–22		0	35	0	25	ns
$\overline{\text{TC}}$ OFF output delay time (from CLKOUT↑)	⑨⑥ t_DKTCF	15–22		0	35	0	25	ns
$\overline{\text{TC}}$ pull-up delay time (from CLKOUT↑)[Note 2]	⑨⑦ t_DKTCH	15–22	R_TC = 1.1 kΩ	0	2t_CYK–10	0	2t_CYK–10	ns
$\overline{\text{TC}}$ low-level width	⑨⑧ t_TCTCL	15–22		t_CYK(n+1)–12[Note1]		t_CYK(n+1)–12[Note1]		ns
$\overline{\text{END}}$ setup time (to CLKOUT↑)	⑨⑨ t_SEDK	15–22		10		10		ns
$\overline{\text{END}}$ low-level width	⑩⓪ t_EDEDL	15–22		100		100		ns
DMARQn (n = 0 to 3) setup time (to CLKOUT↑)	⑩① t_SDQK	15–22, etc.		12		12		ns
$\overline{\text{DMAAKn}}$ (n = 0 to 3) delay time from CLKOUT↓	⑩② t_DKLDA	15–23		0	35	0	25	ns
$\overline{\text{MRD}}$ high-level width	⑩③ t_MRMRH	15–5		0.5t_CYK–7		0.5t_CYK–7		ns
Data set time from $\overline{\text{MRD}}$↑	⑩④ t_DMRHLZ	15–6, etc.		0.5t_CYK–12		0.5t_CYK–12		ns
Data output delay time from $\overline{\text{MRD}}$↑	⑩⑤ t_DMRHD	15–6, etc.		0.5t_CYK–12		0.5t_CYK–12		ns
Cascade address delay time from CLKOUT	⑩⑥ t_DKCA	15–15, etc.		2	30	3	20	ns
$\overline{\text{INTAK}}$ high-level width	⑩⑦ t_IAIAH	15–16		2.5t_CYK–7		2.5t_CYK–7		ns
PCLKOUT delay time from CLKOUT	⑩⑧ t_DKPK	15–1	CLKC = 00		±5		±5	ns
$\overline{\text{IOWR}}$, $\overline{\text{MWR}}$↓ delay time from $\overline{\text{MRD}}$, $\overline{\text{IORD}}$↓	⑩⑨ t_DRLWL	15–21	Normal write	t_CYK–12		t_CYK–12		ns

Notes   1. n indicates the number of wait clock cycles inserted in the bus cycle.
           2. It is assumed that the $\overline{\text{TC}}$ pin is connected with the pull-up resistor R_TC.

Remark   The number in the symbol column correspond to the numbers in the timing charts.

AC Test Input Waveform (Except X1)

```
2.4 V  ──────╲        ╱─────────────────────────────────╲        ╱──────
              ╲ ╱ 2.2 V      →  Test  ←      2.2 V ╲ ╱
               ╳            ╲     points    ╱        ╳
              ╱ ╲ 0.8 V      →        ←      0.8 V ╱ ╲
0.4 V  ──────╱        ╲─────────────────────────────────╱        ╲──────
```

AC Test Input Waveform (X1)

```
VDD  ──────╲        ╱─────────────────────────────────╲        ╱──────
            ╲ ╱ VDD–0.5 V    →  Test  ←    VDD–0.5 V ╲ ╱
             ╳            ╲     points    ╱            ╳
            ╱ ╲ 0.4 V       →        ←      0.4 V ╱ ╲
0 V  ──────╱        ╲─────────────────────────────────╱        ╲──────
```

AC Test Output Test Points

```
──────╲        ╱─────────────────────────────────╲        ╱──────
       ╲ ╱ 2.2 V      →  Test  ←      2.2 V ╲ ╱
        ╳            ╲     points    ╱        ╳
       ╱ ╲ 0.8 V      →        ←      0.8 V ╱ ╲
──────╱        ╲─────────────────────────────────╱        ╲──────
```

Load Conditions


```
┌──────────────┐
│              │
│     DUT      │────────┐        $C_L = 100pF$
│              │        │
│              │       ═╪═
└──────────────┘        │
                       ╧ (GND)
```
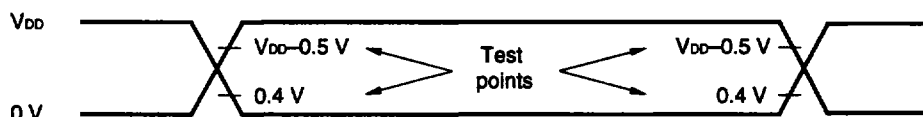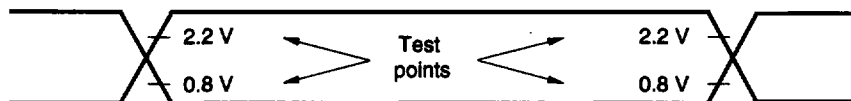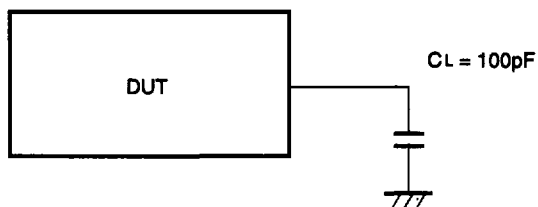
Caution   If the load capacitance exceeds 100 pF due to the construction of the circuit, the load capacitance of this device should be reduced to 100 pF or less by insertion of a buffer, etc.

15.2 SPECIFICATIONS WHEN V_{DD} = 3.6 TO 4.5 V

Absolute Maximum Ratings (T_A = 25 °C)

PARAMETER	SYMBOL	TEST CONDITIONS	RATING	UNIT
Supply voltage	V_{DD}		−0.5 to +7.0	V
Input voltage	V_I	Except X1, V_{DD} = 3.6 to 4.5 V	−0.5 to V_{DD}+0.3	V
Clock input voltage	V_K	X1, V_{DD} = 3.6 to 4.5 V	−0.5 to V_{DD}+1.0	V
Output short current	Ios		50	mA
Output voltage	V_O	V_{DD} = 3.6 to 4.5 V	−0.5 to V_{DD}+0.3	V
Operating ambient temperature	T_A		−40 to +85	°C
Storage temperature	T_{stg}		−65 to +150	°C

Cautions 1. Do not connect output pin (or I/O pin) of IC product directly to other output pins, V_{DD}, V_{CC} or GND. Open drain output pins or open collector output pins, however, can be connected each other. Output pins having high impedance capability can be also connected each other in an external circuit designed the timing to prevent output conflict.

2. Exposure to Absolute Maximum Ratings for extended periods may affect device reliability; exceeding the ratings could cause permanent damage. The parameters apply independently.
The device should be operated within the limits specified under DC and AC Characteristics.

DC Characteristics (T$_A$ = – 40 to +85 °C, V$_{DD}$ = 3.6 to 4.5 V)

PARAMETER	SYMBOL	TEST CONDITIONS	MIN.	TYP.	MAX.	UNIT
Input voltage, high	V$_{IH}$	Except $\overline{RESET}$	2.2		V$_{DD}$+0.3	V
		$\overline{RESET}$	0.8 V$_{DD}$		V$_{DD}$+0.3	V
Input voltage, low	V$_{IL}$	Except $\overline{RESET}$	–0.5		0.2 V$_{DD}$	V
		$\overline{RESET}$	–0.5		0.2 V$_{DD}$	V
Clock input voltage, high	V$_{KH}$	X2, X1	0.8 V$_{DD}$		V$_{DD}$+0.5	V
Clock input voltage, low	V$_{KL}$	X2, X1	–0.5		+0.6	V
Output voltage, high	V$_{OH}$	I$_{OH}$ = –2.5 mA	0.7 V$_{DD}$			V
		I$_{OH}$ = –100 μA	V$_{DD}$–0.4			V
Output voltage, low	V$_{OL}$	Except $\overline{TC}$, I$_{OL}$ = 2.5 mA			0.4	V
		$\overline{TC}$, I$_{OL}$ = 5.0 mA			0.4	V
Input leak current, high	I$_{LIH}$	V$_I$ = V$_{DD}$			10	μA
Input leak current, low	I$_{LIL}$	V$_I$ = 0 V			–10	μA
Output leak current, high	I$_{LOH}$	V$_O$ = V$_{DD}$			10	μA
Output leak current, low	I$_{LOL}$	V$_O$ = 0 V			–10	μA
High-level latch leakage current	I$_{LLH}$	V$_I$ = 3.0 V	0		–200	μA
Low-level latch leakage current	I$_{LLL}$	V$_I$ = 0.8 V	0		200	μA
Latch inversion current (L → H)	I$_{ILH}$				200	μA
Latch inversion current (H → L)	I$_{ILL}$				–200	μA
Supply current^{Note}	I$_{DD}$	In operation (fx = 2 to 16 MHz)		2.9fx + 2	5fx + 5	mA
		HALT (fx = 2 to 16 MHz)		0.03125fx + 0.3	0.35fx + 2.0	mA
		STOP		4.0	150	μA

*

Note   Setting condition : The CPU clock is used for the TCLK0 to TCLK2 with refreshing enabled.
       The units of the constants 2.9, 5, 0.03125, 0.35 are mA/MHz.

Remark   The TYP. values are the reference values when T$_A$ = 25 °C and V$_{DD}$ = 4.0 V.

Capacitance (T$_A$ = 25 °C, V$_{DD}$ = 0 V)

PARAMETER	SYMBOL	TEST CONDITIONS	MIN.	TYP.	MAX.	UNIT
Input capacitance	C$_I$	fc = 1 MHz Unmeasured pins returned to 0 V.			15	pF
Input output capacitance	C$_{IO}$				15	pF
Output capacitance	C$_O$				15	pF

Recommended Oscillator Circuit

(a) Crystal resonator connection (T$_A$ = −40 to +85 °C, V$_{DD}$ = 3.6 to 4.5 V)

   (I) Recommended conditions of oscillation with basic wave

MANUFACTURER	OSCILLATOR FREQUENCY f$_{xx}$ [MHz]	PRODUCT NAME	RECOMMENDED CONSTANT	
			C1 [pF]	C2 [pF]
Kinseki, Ltd.	20	HC-49/U	10	10

Cautions 1. The oscillation circuit should be located as close as possible to the X1 and X2 pins.
   2. No other signal lines should cross the shaded area.
   3. Sufficient evaluation is required for matching between the μPD70236A and the resonator.

   (II) Recommended conditions with third overtone

MANUFACTURER	OSCILLATOR FREQUENCY f$_{xx}$ [MHz]	PRODUCT NAME	RECOMMENDED CONSTANT			
			C1 [pF]	C2 [pF]	C3 [pF]	L [μH]
Kinseki, Ltd.	32	HC-49/U	5	1000	5	5.6
	25		5	1000	10	4.7

Cautions 1. The oscillation circuit should be located as close as possible to the X1 and X2 pins.
   2. No other signal lines should cross the shaded area.
   3. Sufficient evaluation is required for matching between the μPD70236A and the resonator.

(b) External clock input
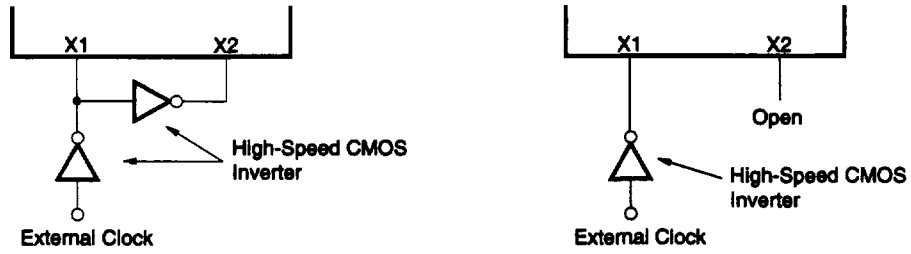
Cautions 1. The high-speed CMOS inverter should be located as close as possible to the X1 and X2 pins.
         2. Ensure that matching between the μPD70236A and the high-speed CMOS inverter is fully evaluated.

AC Characteristics (V_DD = 3.6 to 4.5 V, Output pin load capacitance : C_L = 100 pF)

(1) μPD70236A-16 (V_DD = 3.6 to 4.5 V)

(1/4)

PARAMETER	SYMBOL		FIG.No.	TEST CONDITIONS	T_A = −40 to +85 °C		UNIT
					MIN.	MAX.	
External clock input cycle	①	t_CYX	15–1		40	250	ns
External clock input high-level width	②	t_XKH	15–1		10		ns
External clock input low-level width	③	t_XKL	15–1		10		ns
External clock input rise time	④	t_XKR	15–1			7	ns
External clock input fall time	⑤	t_XKF	15–1			7	ns
CPU operating frequency	–	f_X	–		2	12.5	MHz
CLKOUT output frequency	⑥	t_CYK	15–1		80	500	ns
CLKOUT high-level width	⑦	t_KKH	15–1		0.5t_CYK−10		ns
CLKOUT low-level width	⑧	t_KKL	15–1		0.5t_CYK−10		ns
CLKOUT rise time	⑨	t_KR	15–1	0.2V_DD → 0.7V_DD		10	ns
CLKOUT fall time	⑩	t_KF	15–1	0.7V_DD → 0.2V_DD		10	ns
CLKOUT delay time (from external clock)	⑪	t_DXK	15–1		4	30	ns
PCLKOUT output frequency	⑫	t_CYPK	15–1		4t_CYX	1000	ns
PCLKOUT high-level width	⑬	t_PKH	15–1		2t_CYX−10		ns
PCLKOUT low-level width	⑭	t_PKL	15–1		2t_CYX−10		ns
PCLKOUT output rise time	⑮	t_PKR	15–1	0.2V_DD → 0.7V_DD		10	ns
PCKLOUT output fall time	⑯	t_PKF	15–1	0.7V_DD → 0.2V_DD		10	ns
Input rise time[Note 1]	⑰	t_IR		0.7V_DD → 0.2V_DD		12	ns
Input fall time[Note 1]	⑱	t_IF		0.2V_DD → 0.7V_DD		10	ns
Output rise time[Note 2]	⑲	t_OR		0.7V_DD → 0.2V_DD		12	ns
Output fall time[Note 2]	⑳	t_OF		0.2V_DD → 0.7V_DD		10	ns
RESET setup time (to CLKOUT↓)	㉑	t_SRSTK	15–2		30		ns
RESET hold time (from CLKOUT↓)	㉒	t_HKRST	15–2		15		ns
RESOUT output delay time (from CLKOUT↓)	㉓	t_DKRO	15–2		0	40	ns
RESET low-level width	㉔	t_WRSTL	15–2		6t_CYK		ns
READY setup time (to CLKOUT↑)	㉕	t_SRYK	15–3, etc.		7		ns
READY hold time (from CLKOUT↑)	㉖	t_HKRY	15–3, etc.		15		ns
BCYST high-level width	㉗	t_BCBCH	15–5, etc.		t_CYK(n+1)−10[Note 3]		ns
BCYST low-level width	㉘	t_BCBCL	15–5, etc.		t_CYK−10		ns
BCYST delay time from CLKOUT↓	㉙	t_DKBC	15–5, etc.		4	35	ns
MRD delay time from CLKOUT	㉚	t_DKMR	15–5, etc.		0	40	ns

Notes 1. Except external clock and RESET
2. Except CLKOUT and PCLKOUT
3. n indicates the number of wait clock cycles inserted in the bus cycle. In a co-processor cycle, 1 (=TC cycle) must be added to n.

Remark The number in the symbol column correspond to the numbers in the timing charts.

μPD70236A-16 (V$_{DD}$ = 3.6 to 4.5 V)

(2/4)

PARAMETER	SYMBOL		FIG.No.	TEST CONDITIONS	T$_A$ = −40 to +85 °C		UNIT
					MIN.	MAX.	
$\overline{MRD}\downarrow$, $\overline{IORD}\downarrow$ delay time from address/status output	㉛	t$_{DARL}$	15–5, etc.		0.5tcyк–15		ns
Data hold time (from $\overline{MRD}\uparrow$, from $\overline{IORD}\uparrow$)	㉜	t$_{HRD}$	15–5, etc.		0		ns
Address delay time from CLKOUT↓[Note 1]	㉝	t$_{DKA}$	15–5, etc.		3	35	ns
Data hold time (from R/$\overline{W}\downarrow$)	㉞	t$_{HRWD}$	15–5		0		ns
Status delay time from CLKOUT↓	㉟	t$_{DKST}$	15–5, etc.		4	35	ns
$\overline{DSTB}\downarrow$ output delay time from CLKOUT↑	㊱	t$_{DKDS}$	15–5, etc.		5	45	ns
$\overline{DSTB}\uparrow$ output delay time from CLKOUT	㊲	t$_{DKDSH}$	15–5, etc.		4	40	ns
$\overline{DSTB}\downarrow$ delay time from address/status output	㊳	t$_{DADSL}$	15–5, etc.		0.5tcyк–15		ns
$\overline{DSTB}$ high-level width	㊴	t$_{DSDSH}$	15–5, etc.		0.5tcyк–10		ns
$\overline{DSTB}$ low-level width	㊵	t$_{DSDSL}$	15–6, etc.		tcyк(n+1)–10[Note 4]		ns
Data hold time (from $\overline{DSTB}\uparrow$)	㊶	t$_{HDSD}$	15–5, etc.		0		ns
Data hold time (from address/status change point)	㊷	t$_{HASD}$	15–5		0		ns
Control 1[Note 2] delay time from CLKOUT	㊸	t$_{DKCT1}$	15–21		0	40	ns
Control 2[Note 3] delay time from CLKOUT	㊹	t$_{DKCT2}$	15–5, etc.		0	40	ns
Data setup time (to CLKOUT↓)	㊺	t$_{SDK}$	15–5, etc.		10		ns
Data hold time (from CLKOUT↓)	㊻	t$_{HKD}$	15–5, etc.		10		ns
Output floating time from $\overline{DSTB}\downarrow$	㊼	t$_{DHZ}$	15–5, etc.			0	ns
Address/status hold time from $\overline{MWR}\uparrow$	㊽	t$_{HMWHA}$	15–6		0.5tcyк–15		ns
$\overline{MWR}$ delay time from CLKOUT	㊾	t$_{DKMW}$	15–6, etc.		0	40	ns
$\overline{MWR}\downarrow$, $\overline{IOWR}\downarrow$ delay time from address/status output	㊿	t$_{DAWL}$	15–6, etc.		0.5tcyк–15		ns
$\overline{MWR}$, $\overline{IOWR}$ low-level width	�51	t$_{WWL}$	15–6, etc.		tcyк(n+1)–10[Note 4]		ns
Address/status hold time from $\overline{DSTB}\uparrow$	�52	t$_{HDSHA}$	15–6, etc.		0.5tcyк–15		ns
Data output delay time from $\overline{DSTB}\uparrow$	�53	t$_{DDSHD}$	15–6, etc.		0.5tcyк–15		ns
Data delay time from address/status output	�54	t$_{DAD}$	15–6, etc.		0.5tcyк–15		ns
Output setting time from $\overline{DSTB}\uparrow$	�55	t$_{DLZ}$	15–6, etc.		0.5tcyк–15		ns

Notes 1. These specifications apply to the following delay times from the falling edge of the CLKOUT signal.   ✶

    (1) Address delay time

    (2) $\overline{BUSLOCK}$ delay time

    (3) Delay time of signals below immediately after release of bus hold:

        A23-A0, D15-D0, M/$\overline{IO}$, BUSST1, BUSST0, $\overline{UBE}$, $\overline{BCYST}$, $\overline{DSTB}$.

  2. Control 1 applies to the $\overline{MWR}$ and $\overline{IOWR}$ signals in a DMA cycle.

  3. Control 2 applies to the $\overline{BUFEN}$, $\overline{INTAK}$ and $\overline{REFRQ}$ setups.

  4. n indicates the number of wait clock cycles inserted in the bus cycle. In a co-processor cycle, 1 (=TC cycle) must be added to n.

Remarks 1. The number in the symbol column correspond to the numbers in the timing charts.

       2. Regarding the five specifications ㉜ t$_{HRD}$, ㉞ t$_{HRWD}$, ㊶ t$_{HDSD}$, ㊷ t$_{HASD}$, and ㊻ t$_{HKD}$, at least one should be observed.

μPD70236A-16 (V_DD = 3.6 to 4.5 V)

(3/4)

PARAMETER	SYMBOL	FIG.No.	TEST CONDITIONS	T_A = –40 to +85 °C MIN.	T_A = –40 to +85 °C MAX.	UNIT
Data output delay time from CLKOUT↑	56 t_DKO	15–6, etc.		4	40	ns
Float delay time from CLKOUT	57 t_FK	15–6, etc.		0	40	ns
IORD delay time from CLKOUT	58 t_DKIR	15–7		0	40	ns
IOWR delay time from CLKOUT	59 t_DKIW	15–8		0	40	ns
NMI, INTPn (n = 0 to 7), CPBUSY setup time (to CLKOUT↓)	60 t_SIK	15–11		10		ns
NMI, INTPn(n = 0 to 7), CPBUSY hold time (from CLKOUT↓)	61 t_HKI	15–11		10		ns
BS8/BS16 setup time (to CLKOUT↑)	62 t_SBSK	15–13		10		ns
BS8/BS16 hold time (from CLKOUT↑)	63 t_HKBS	15–13		10		ns
HLDRQ setup time (to CLKOUT↑)	64 t_SHQK	15–14		10		ns
HLDRQ hold time (from CLKOUT↑)	65 t_HKHQ	15–14		15		ns
HLDAK delay time from CLKOUT↑	66 t_DKHA	15–14		4	40	ns
HLDAK delay time from output float	67 t_DFHA	15–14		0.5t_CYK–15		ns
INTPn(n = 0 to 7) low-level width	68 t_IPIPL	15–17		90		ns
TCTLn (n = 0 to 2) setup time (to CLKOUT↓)	69 t_SGK	15–18		55		ns
TCTLn (n = 0 to 2) hold time (from CLKOUT↓)	70 t_HKG	15–18		90		ns
TCTLn (n = 0 to 2) high-level width	71 t_GGH	15–18, etc.		45		ns
TCTLn (n = 0 to 2) low-level width	72 t_GGL	15–18, etc.		45		ns
TOUTn (n = 0 to 2) output delay time (from TCTLn (n = 0 to 2)↓)	73 t_DGTO	15–18, etc.			100	ns
TOUTn (n = 0 to 2) output delay time (from CLKOUT↓)	74 t_DKTO	15–18			70	ns
TCLK cycle	75 t_CYTK	15–19		80	DC	ns
TCLK high-level width	76 t_TKTKH	15–19		30		ns
TCLK low-level width	77 t_TKTKL	15–19		35		ns
TCLK rise time	78 t_TKR	15–19			15	ns
TCLK fall time	79 t_TKF	15–19			15	ns
TCTLn (n = 0 to 2) hold time (from TCLK↑)	80 t_HTKG	15–19		60		ns
TCTLn (n = 0 to 2) setup time (to TCLK↑)	81 t_SGTK	15–19		45		ns
TOUTn (n = 0 to 2) output delay time (from TCLK↓)	82 t_DTKTO	15–19			120	ns
RxD setup time (to SCU internal clock↓)	83 t_SRX	15–20		700		ns
RxD hold time (from SCU internal clock↓)	84 t_HRX	15–20		700		ns
TxD delay time from TOUT1↑	85 t_DTX	15–20			300	ns
DMAAKn (n = 0 to 3) delay time from CLKOUT↑	86 t_DKHDA	15–21		0	40	ns
MRD, IORD↓ delay time from CLKOUT↓	87 t_DKRL	15–21		0	40	ns
MRD, IORD↑ delay time from CLKOUT↓	88 t_DKRH	15–21		0	40	ns
DMAAKn (n = 0 to 3)↑ delay time (from IORD↑)	89 t_DRHDAH	15–21		0.5t_CYK–15		ns
IORD↓,IOWR↓ delay time (from DMAAKn (n = 0 to 3)↓)	90 t_DDARW	15–21		0.5t_CYK–15		ns

Remark The number in the symbol column correspond to the numbers in the timing charts.

μPD70236A-16 (V$_{DD}$ = 3.6 to 4.5 V)

(4/4)

PARAMETER	SYMBOL		FIG.No.	TEST CONDITIONS	T$_A$ = −40 to +85 °C		UNIT
					MIN.	MAX.	
$\overline{IORD}$↑ delay time (from $\overline{MWR}$↑) $\overline{MRD}$↑ delay time (from $\overline{IOWR}$↑)	⑨①	t$_{DWHRH}$	15–21		0		ns
$\overline{IORD}$, $\overline{MRD}$ low-level width	⑨②	t$_{RR}$	15–21		t$_{CYK}$(n+2)−40[Note 1]		ns
$\overline{IOWR}$, $\overline{MWR}$ low-level width (extended write)	⑨③	t$_{WW1}$	15–21	Extended write	t$_{CYK}$(n+2)−40[Note 1]		ns
$\overline{IOWR}$, $\overline{MWR}$ low-level width (normal write)	⑨④	t$_{WW2}$	15–21	Normal write	t$_{CYK}$(n+1)−40[Note 1]		ns
$\overline{TC}$ output delay time (from CLKOUT↑)	⑨⑤	t$_{DKTCL}$	15–22		0	40	ns
$\overline{TC}$ OFF output delay time (from CLKOUT↑)	⑨⑥	t$_{DKTCF}$	15–22		0	40	ns
$\overline{TC}$ pull-up delay time (from CLKOUT↑)[Note 2]	⑨⑦	t$_{DKTCH}$	15–22	R$_{TC}$ = 1.1 kΩ	0	2t$_{CYK}$−15	ns
$\overline{TC}$ low-level width	⑨⑧	t$_{TCTCL}$	15–22		t$_{CYK}$(n+1)−15[Note 1]		ns
$\overline{END}$ setup time (to CLKOUT↑)	⑨⑨	t$_{SEDK}$	15–22		15		ns
$\overline{END}$ low-level width	⑩⓪	t$_{EDEDL}$	15–22		100		ns
DMARQn (n = 0 to 3) setup time (to CLKOUT↑)	⑩①	t$_{SDQK}$	15–22, etc.		15		ns
$\overline{DMAAKn}$ (n = 0 to 3) delay time from CLKOUT↓	⑩②	t$_{DKLDA}$	15–23		0	40	ns
$\overline{MRD}$ high-level width	⑩③	t$_{MRMRH}$	15–5		0.5t$_{CYK}$−10		ns
Data set time from $\overline{MRD}$↑	⑩④	t$_{DMRHLZ}$	15–6, etc.		0.5t$_{CYK}$−15		ns
Data output delay time from $\overline{MRD}$↑	⑩⑤	t$_{DMRHD}$	15–6, etc.		0.5t$_{CYK}$−15		ns
Cascade address delay time from CLKOUT	⑩⑥	t$_{DKCA}$	15–15, etc.		3	35	ns
$\overline{INTAK}$ high-level width	⑩⑦	t$_{IAIAH}$	15–16		2.5t$_{CYK}$−10		ns
PCLKOUT delay time from CLKOUT	⑩⑧	t$_{DKPK}$	15–1	CLKC = 00		±5	ns
$\overline{IOWR}$, $\overline{MWR}$↓ delay time from $\overline{MRD}$, $\overline{IORD}$↓	⑩⑨	t$_{DRLWL}$	15–21	Normal write	t$_{CYK}$−15		ns

*

Notes　1. n indicates the number of wait clock cycles inserted in the bus cycle.

　　　　　2. It is assumed that the $\overline{TC}$ pin is connected with the pull-up resistor R$_{TC}$.

Remark　The number in the symbol column correspond to the numbers in the timing charts.

(2) μPD70236A-20 (V_DD = 3.6 to 4.5 V)

(1/4)

PARAMETER	SYMBOL		FIG.No.	TEST CONDITIONS	T_A = −40 to +85 °C		UNIT
					MIN.	MAX.	
External clock input cycle	①	tcYx	15−1		31.25	250	ns
External clock input high-level width	②	txKH	15−1		8		ns
External clock input low-level width	③	txKL	15−1		8		ns
External clock input rise time	④	txKR	15−1			7	ns
External clock input fall time	⑤	txKF	15−1			7	ns
CPU operating frequency	−	fx	−		2	16	MHz
CLKOUT output frequency	⑥	tcYK	15−1		62.5	500	ns
CLKOUT high-level width	⑦	tKKH	15−1		0.5tcYK−10		ns
CLKOUT low-level width	⑧	tKKL	15−1		0.5tcYK−10		ns
CLKOUT rise time	⑨	tKR	15−1	0.2VDD → 0.7VDD		10	ns
CLKOUT fall time	⑩	tKF	15−1	0.7VDD → 0.2VDD		10	ns
CLKOUT delay time (from external clock)	⑪	tDxK	15−1		4	30	ns
PCLKOUT output frequency	⑫	tcYPK	15−1		4tcYx	1000	ns
PCLKOUT high-level width	⑬	tPKH	15−1		2tcYx−10		ns
PCLKOUT low-level width	⑭	tPKL	15−1		2tcYx−10		ns
PCLKOUT output rise time	⑮	tPKR	15−1	0.2VDD → 0.7VDD		10	ns
PCKLOUT output fall time	⑯	tPKF	15−1	0.7VDD → 0.2VDD		10	ns
Input rise time[Note 1]	⑰	tIR		0.7VDD → 0.2VDD		12	ns
Input fall time[Note 1]	⑱	tIF		0.2VDD → 0.7VDD		10	ns
Output rise time[Note 2]	⑲	tOR		0.7VDD → 0.2VDD		12	ns
Output fall time[Note 2]	⑳	tOF		0.2VDD → 0.7VDD		10	ns
RESET setup time (to CLKOUT↓)	㉑	tsRSTK	15−2		30		ns
RESET hold time (from CLKOUT↓)	㉒	tHKRST	15−2		15		ns
RESOUT output delay time (from CLKOUT↓)	㉓	tDKRO	15−2		0	40	ns
RESET low-level width	㉔	tWRSTL	15−2		6tcYK		ns
READY setup time (to CLKOUT↑)	㉕	tsRYK	15−3, etc.		7		ns
READY hold time (from CLKOUT↑)	㉖	tHKRY	15−3, etc.		15		ns
BCYST high-level width	㉗	tBCBCH	15−5, etc.		tcYK(n+1)−10[Note 3]		ns
BCYST low-level width	㉘	tBCBCL	15−5, etc.		tcYK−10		ns
BCYST delay time from CLKOUT↓	㉙	tDKBC	15−5, etc.		4	35	ns
MRD delay time from CLKOUT	㉚	tDKMR	15−5, etc.		0	40	ns

Notes 1. Except external clock and RESET

2. Except CLKOUT and PCLKOUT

3. n indicates the number of wait clock cycles inserted in the bus cycle. In a co-processor cycle, 1 (=TC cycle) must be added to n.

Remark The number in the symbol column correspond to the numbers in the timing charts.

μPD70236A-20 (V_DD = 3.6 to 4.5 V)

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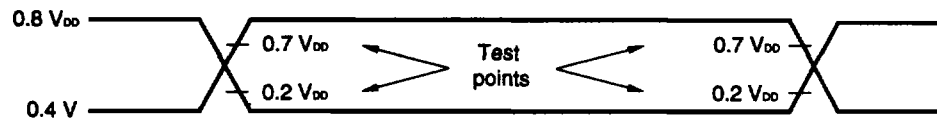| PARAMETER	SYMBOL	FIG.No.	TEST CONDITIONS	T_A = −40 to +85 °C		UNIT
				MIN.	MAX.	
MRD↓, IORD↓ delay time from address/status output	㉛ t_{DARL}	15–5, etc.		0.5t_{CYK}−15		ns
Data hold time (from MRD↑, from IORD↑)	㉜ t_{HRD}	15–5, etc.		0		ns
Address delay time from CLKOUT↓ Note 1	㉝ t_{DKA}	15–5, etc.		3	35	ns
Data hold time (from R/W↓)	㉞ t_{HRWD}	15–5		0		ns
Status delay time from CLKOUT↓	㉟ t_{DKST}	15–5, etc.		4	35	ns
DSTB↓ output delay time from CLKOUT↑	㊱ t_{DKDS}	15–5, etc.		5	45	ns
DSTB↑ output delay time from CLKOUT	㊲ t_{DKDSH}	15–5, etc.		4	40	ns
DSTB↓ delay time from address/status output	㊳ t_{DADSL}	15–5, etc.		0.5t_{CYK}−15		ns
DSTB high-level width	㊴ t_{DSDSH}	15–5, etc.		0.5t_{CYK}−10		ns
DSTB low-level width	㊵ t_{DSDSL}	15–6, etc.		$t_{CYK}(n+1)$−10 Note 4		ns
Data hold time (from DSTB↑)	㊶ t_{HDSD}	15–5, etc.		0		ns
Data hold time (from address/status change point)	㊷ t_{HASD}	15–5		0		ns
Control 1 Note 2 delay time from CLKOUT	㊸ t_{DKCT1}	15–21		0	40	ns
Control 2 Note 3 delay time from CLKOUT	㊹ t_{DKCT2}	15–5, etc.		0	40	ns
Data setup time (to CLKOUT↓)	㊺ t_{SDK}	15–5, etc.		10		ns
Data hold time (from CLKOUT↓)	㊻ t_{HKD}	15–5, etc.		10		ns
Output floating time from DSTB↓	㊼ t_{DHZ}	15–5, etc.			0	ns
Address/status hold time from MWR↑	㊽ t_{HMWHA}	15–6		0.5t_{CYK}−15		ns
MWR delay time from CLKOUT	㊾ t_{DKMW}	15–6, etc.		0	40	ns
MWR↓, IOWR↓ delay time from address/status output	㊿ t_{DAWL}	15–6, etc.		0.5t_{CYK}−15		ns
MWR, IOWR low-level width	�51 t_{WWL}	15–6, etc.		$t_{CYK}(n+1)$−10 Note 4		ns
Address/status hold time from DSTB↑	�52 t_{HDSHA}	15–6, etc.		0.5t_{CYK}−15		ns
Data output delay time from DSTB↑	�53 t_{DDSHD}	15–6, etc.		0.5t_{CYK}−15		ns
Data delay time from address/status output	�54 t_{DAD}	15–6, etc.		0.5t_{CYK}−15		ns
Output setting time from DSTB↑	�55 t_{DLZ}	15–6, etc.		0.5t_{CYK}−15		ns

Notes 1. These specifications apply to the following delay times from the falling edge of the CLKOUT signal. ∗
  (1) Address delay time
  (2) BUSLOCK delay time
  (3) Delay time of signals below immediately after release of bus hold:
    A23-A0, D15-D0, M/IO, BUSST1, BUSST0, UBE, BCYST, DSTB.
2. Control 1 applies to the MWR and IOWR signals in a DMA cycle.
3. Control 2 applies to the BUFEN, INTAK and REFRQ setups.
4. n indicates the number of wait clock cycles inserted in the bus cycle. In a co-processor cycle, 1 (=TC cycle) must be added to n.

Remarks 1. The number in the symbol column correspond to the numbers in the timing charts.
2. Regarding the five specifications ㉜t_{HRD}, ㉞t_{HRWD}, ㊶t_{HDSD}, ㊷t_{HASD}, and ㊻t_{HKD}, at least one should be observed.

μPD70236A-20 (V$_{DD}$ = 3.6 to 4.5 V)

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PARAMETER	SYMBOL	FIG.No.	TEST CONDITIONS	T$_A$ = –40 to +85 °C		UNIT
				MIN.	MAX.	
Data output delay time from CLKOUT↑	⑤⑥ t$_{DKD}$	15–6, etc.		4	40	ns
Float delay time from CLKOUT	⑤⑦ t$_{FK}$	15–6, etc.		0	40	ns
$\overline{IORD}$ delay time from CLKOUT	⑤⑧ t$_{DKIR}$	15–7		0	40	ns
$\overline{IOWR}$ delay time from CLKOUT	⑤⑨ t$_{DKIW}$	15–8		0	40	ns
$\overline{NMI}$, INTPn (n = 0 to 7), $\overline{CPBUSY}$ setup time (to CLKOUT↓)	⑥⓪ t$_{SIK}$	15–11		10		ns
$\overline{NMI}$, INTPn(n = 0 to 7), $\overline{CPBUSY}$ hold time (from CLKOUT↓)	⑥① t$_{HKI}$	15–11		10		ns
$\overline{BS8}$/BS16 setup time (to CLKOUT↑)	⑥② t$_{SBSK}$	15–13		10		ns
$\overline{BS8}$/BS16 hold time (from CLKOUT↑)	⑥③ t$_{HKBS}$	15–13		10		ns
HLDRQ setup time (to CLKOUT↑)	⑥④ t$_{SHQK}$	15–14		10		ns
HLDRQ hold time (from CLKOUT↑)	⑥⑤ t$_{HKHQ}$	15–14		15		ns
HLDAK delay time from CLKOUT↑	⑥⑥ t$_{DKHA}$	15–14		4	40	ns
HLDAK delay time from output float	⑥⑦ t$_{DFHA}$	15–14		0.5t$_{CYK}$–15		ns
INTPn(n = 0 to 7) low-level width	⑥⑧ t$_{IPIPL}$	15–17		90		ns
TCTLn (n = 0 to 2) setup time (to CLKOUT↓)	⑥⑨ t$_{SGK}$	15–18		55		ns
TCTLn (n = 0 to 2) hold time (from CLKOUT↓)	⑦⓪ t$_{HKG}$	15–18		90		ns
TCTLn (n = 0 to 2) high-level width	⑦① t$_{GGH}$	15–18, etc.		45		ns
TCTLn (n = 0 to 2) low-level width	⑦② t$_{GGL}$	15–18, etc.		45		ns
TOUTn (n = 0 to 2) output delay time (from TCTLn (n = 0 to 2)↓)	⑦③ t$_{DGTO}$	15–18, etc.			100	ns
TOUTn (n = 0 to 2) output delay time (from CLKOUT↓)	⑦④ t$_{DKTO}$	15–18			70	ns
TCLK cycle	⑦⑤ t$_{CYTK}$	15–19		62.5	DC	ns
TCLK high-level width	⑦⑥ t$_{TKTKH}$	15–19		25		ns
TCLK low-level width	⑦⑦ t$_{TKTKL}$	15–19		30		ns
TCLK rise time	⑦⑧ t$_{TKR}$	15–19			15	ns
TCLK fall time	⑦⑨ t$_{TKF}$	15–19			15	ns
TCTLn (n = 0 to 2) hold time (from TCLK↑)	⑧⓪ t$_{HTKG}$	15–19		60		ns
TCTLn (n = 0 to 2) setup time (to TCLK↑)	⑧① t$_{SGTK}$	15–19		45		ns
TOUTn (n = 0 to 2) output delay time (from TCLK↓)	⑧② t$_{DTKTO}$	15–19			120	ns
RxD setup time (to SCU internal clock↓)	⑧③ t$_{SRX}$	15–20		700		ns
RxD hold time (from SCU internal clock↓)	⑧④ t$_{HRX}$	15–20		700		ns
TxD delay time from TOUT1↑	⑧⑤ t$_{DTX}$	15–20			300	ns
$\overline{DMAAKn}$ (n = 0 to 3) delay time from CLKOUT↑	⑧⑥ t$_{DKHDA}$	15–21		0	40	ns
$\overline{MRD}$, $\overline{IORD}$↓ delay time from CLKOUT↓	⑧⑦ t$_{DKRL}$	15–21		0	40	ns
$\overline{MRD}$, $\overline{IORD}$↑ delay time from CLKOUT↓	⑧⑧ t$_{DKRH}$	15–21		0	40	ns
$\overline{DMAAKn}$ (n = 0 to 3)↑ delay time (from $\overline{IORD}$↑)	⑧⑨ t$_{DRHDAH}$	15–21		0.5t$_{CYK}$–15		ns
$\overline{IORD}$↓,$\overline{IOWR}$↓ delay time (from $\overline{DMAAKn}$ (n = 0 to 3)↓)	⑨⓪ t$_{DDARW}$	15–21		0.5t$_{CYK}$–15		ns

Remark   The number in the symbol column correspond to the numbers in the timing charts.

μPD70236A-20 (V_DD = 3.6 to 4.5 V)

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PARAMETER	SYMBOL		FIG.No.	TEST CONDITIONS	T_A = −40 to +85 °C		UNIT
					MIN.	MAX.	
IORD↑ delay time (from MWR↑) MRD↑ delay time (from IOWR↑)	91	t_DWHRH	15–21		0		ns
IORD, MRD low-level width	92	t_RR	15–21		t_CYK(n+2)−40[Note 1]		ns
IOWR, MWR low-level width (extended write)	93	t_WW1	15–21	Extended write	t_CYK(n+2)−40[Note 1]		ns
IOWR, MWR low-level width (normal write)	94	t_WW2	15–21	Normal write	t_CYK(n+1)−40[Note 1]		ns
TC output delay time (from CLKOUT↑)	95	t_DKTCL	15–22		0	40	ns
TC OFF output delay time (from CLKOUT↑)	96	t_DKTCF	15–22		0	40	ns
TC pull-up delay time (from CLKOUT↑)[Note 2]	97	t_DKTCH	15–22	R_TC = 1.1 kΩ	0	2t_CYK−15	ns
TC low-level width	98	t_RCTCL	15–22		t_CYK(n+1)−15[Note 1]		ns
END setup time (to CLKOUT↑)	99	t_SEDK	15–22		15		ns
END low-level width	100	t_EDEDL	15–22		100		ns
DMARQn (n = 0 to 3) setup time (to CLKOUT↑)	101	t_SDQK	15–22, etc.		15		ns
DMAAKn (n = 0 to 3) delay time from CLKOUT↓	102	t_DKLDA	15–23		0	40	ns
MRD high-level width	103	t_MRMRH	15–5		0.5t_CYK−10		ns
Data set time from MRD↑	104	t_DMRHLZ	15–6, etc.		0.5t_CYK−15		ns
Data output delay time from MRD↑	105	t_DMRHD	15–6, etc.		0.5t_CYK−15		ns
Cascade address delay time from CLKOUT	106	t_DKCA	15–15, etc.		3	35	ns
INTAK high-level width	107	t_IAIAH	15–16		2.5t_CYK−10		ns
PCLKOUT delay time from CLKOUT	108	t_DKPK	15–1	CLKC = 00		±5	ns
IOWR, MWR↓ delay time from MRD, IORD↓	109	t_DRLWL	15–21	Normal write	t_CYK−15		ns

*

Notes 1. n indicates the number of wait clock cycles inserted in the bus cycle.

2. It is assumed that the TC pin is connected with the pull-up resistor R_TC.

Remark The number in the symbol column correspond to the numbers in the timing charts.

AC Test Input Waveform (Except X1)

```
0.8 Vᴅᴅ ───────╲    ╱─── 0.7 Vᴅᴅ ──→      ←── 0.7 Vᴅᴅ ───╲    ╱───
                ╳                        Test                    ╳
0.4 V  ─────────╱    ╲─── 0.2 Vᴅᴅ ──→    points  ←── 0.2 Vᴅᴅ ───╱    ╲───
```

AC Test Input Waveform (X1)

```
Vᴅᴅ ───────╲    ╱─── 0.8 Vᴅᴅ ──→      ←── 0.8 Vᴅᴅ ───╲    ╱───
            ╳                        Test                    ╳
0 V  ───────╱    ╲─── 0.2 Vᴅᴅ ──→    points  ←── 0.2 Vᴅᴅ ───╱    ╲───
```

AC Test Output Test Points

```
───────╲    ╱─── 0.7 Vᴅᴅ ──→      ←── 0.7 Vᴅᴅ ───╲    ╱───
        ╳                        Test                    ╳
───────╱    ╲─── 0.2 Vᴅᴅ ──→    points  ←── 0.2 Vᴅᴅ ───╱    ╲───
```

Load Conditions

```
┌──────────────┐
│              │
│     DUT      │────────┬──── CL = 100pF
│              │        │
└──────────────┘      ──┴──
                      ──┬──
                        │
                       ╱╱╱
```

Caution   If the load capacitance exceeds 100 pF due to the construction of the circuit, the load capacitance of this device should be reduced to 100 pF or less by insertion of a buffer, etc.

15.3 SPECIFICATIONS WHEN V_{DD} = 2.7 TO 3.6 V

Absolute Maximum Ratings (T_A = 25 °C)

PARAMETER	SYMBOL	TEST CONDITIONS	RATING	UNIT
Supply voltage	V_{DD}		−0.5 to +7.0	V
Input voltage	V_I	Except X1, V_{DD} = 2.7 to 3.6 V	−0.5 to V_{DD} +0.3	V
Clock input voltage	V_K	X1, V_{DD} = 2.7 to 3.6 V	−0.5 to V_{DD} +1.0	V
Output short current	I_{OS}		50	mA
Output voltage	V_O	V_{DD} = 2.7 to 3.6 V	−0.5 to V_{DD} +0.3	V
Operating ambient temperature	T_A		−40 to +85	°C
Storage temperature	T_{stg}		−65 to +150	°C

Cautions 1. Do not connect output pin (or I/O pin) of IC product directly to other output pins, V_{DD}, V_{CC} or GND. Open drain output pins or open collector output pins, however, can be connected each other. Output pins having high impedance capability can be also connected each other in an external circuit designed the timing to prevent output conflict.

2. Exposure to Absolute Maximum Ratings for extended periods may affect device reliability; exceeding the ratings could cause permanent damage. The parameters apply independently.
The device should be operated within the limits specified under DC and AC Characteristics.

DC Characteristics (T$_A$ = − 40 to +85 °C, V$_{DD}$ = 2.7 to 3.6 V)

PARAMETER	SYMBOL	TEST CONDITIONS	MIN.	TYP.	MAX.	UNIT
Input voltage, high	V$_{IH}$	Except RESET	0.7 V$_{DD}$		V$_{DD}$+0.3	V
		RESET	0.8 V$_{DD}$		V$_{DD}$+0.3	V
Input voltage, low	V$_{IL}$	Except RESET	−0.5		0.2 V$_{DD}$	V
		RESET	−0.5		0.2 V$_{DD}$	V
Clock input voltage, high	V$_{KH}$	X2, X1	0.8 V$_{DD}$		V$_{DD}$+0.5	V
Clock input voltage, low	V$_{KL}$	X2, X1	−0.5		0.14 V$_{DD}$	V
Output voltage, high	V$_{OH}$	I$_{OH}$ = −2.5 mA	0.7 V$_{DD}$			V
		I$_{OH}$ = −100 μA	V$_{DD}$−0.4			V
Output voltage, low	V$_{OL}$	I$_{OL}$ = 2.5 mA			0.4	V
Input leak current, high	I$_{LIH}$	V$_I$ = V$_{DD}$			10	μA
Input leak current, low	I$_{LIL}$	V$_I$ = 0 V			−10	μA
Output leak current, high	I$_{LOH}$	V$_O$ = V$_{DD}$			10	μA
Output leak current, low	I$_{LOL}$	V$_O$ = 0 V			−10	μA
High-level latch leakage current	I$_{LLH}$	V$_I$ = 2.5 V	0		−200	μA
Low-level latch leakage current	I$_{LLL}$	V$_I$ = 0.8 V	0		200	μA
Latch inversion current (L → H)	I$_{ILH}$				200	μA
Latch inversion current (H → L)	I$_{ILL}$				−200	μA
Supply current[Note]	I$_{DD}$	In operation (f$_x$ = 2 to 10 MHz)		2.2f$_x$ + 2	4f$_x$ + 5	mA
		HALT (f$_x$ = 2 to 10 MHz)		0.035f$_x$+ 0.2	0.35f$_x$+1.5	mA
		STOP		3.0	100	μA

Note Setting condition : The CPU clock is used for the TCLK0 to TCLK2 with refreshing enabled.
The units of the constants 2.2, 4, 0.035 and 0.35 are mA/MHz.

Remark The TYP. values are the reference values when T$_A$ = 25 °C and V$_{DD}$ = 3.0 V.

Capacitance (T$_A$ = 25 °C, V$_{DD}$ = 0 V)

PARAMETER	SYMBOL	TEST CONDITIONS	MIN.	TYP.	MAX.	UNIT
Input capacitance	C$_I$	fc = 1 MHz Unmeasured pins returned to 0 V.			15	pF
Input output capacitance	C$_{IO}$				15	pF
Output capacitance	C$_O$				15	pF

Recommended Oscillator Circuit

(a) Ceramic resonator connection (TA = −40 to +85 °C, VDD = 2.8 to 3.6 V)
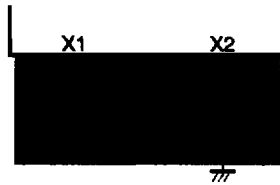
MANUFACTURER	OSCILLATOR FREQUENCY fxx [MHz]	PRODUCT NAME	RECOMMENDED CONSTANT		
			C1 [pF]	C2 [pF]	Rd [Ω]
Murata Mfg. Co., Ltd.	20	CSA20.00MXZ040	—	5	33

Cautions 1. The oscillation circuit should be located as close as possible to the X1 and X2 pins.
2. No other signal lines should cross the shaded area.
3. Sufficient evaluation is required for matching between the μPD70236A and the resonator.

(b) Crystal resonator connection (TA = −40 to +85 °C, VDD = 2.7 to 3.6 V) : Recommended conditions of oscillation with basic wave
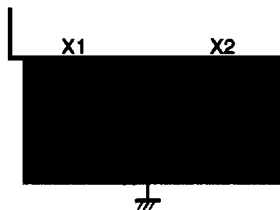
MANUFACTURER	OSCILLATOR FREQUENCY fxx [MHz]	PRODUCT NAME	RECOMMENDED CONSTANT	
			C1 [pF]	C2 [pF]
Kinseki, Ltd.	20	HC-49/U	10	10
	16		20	20

Cautions 1. The oscillation circuit should be located as close as possible to the X1 and X2 pins.
2. No other signal lines should cross the shaded area.
3. Sufficient evaluation is required for matching between the μPD70236A and the resonator.

(c) External clock input
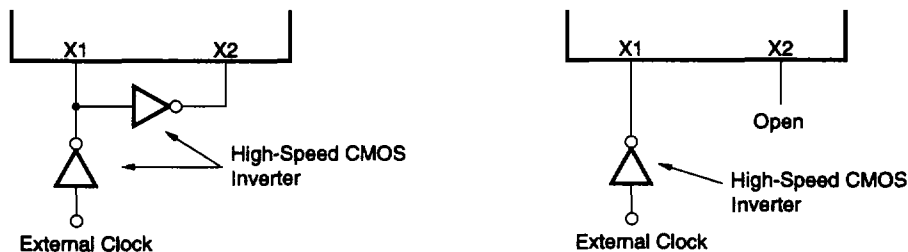
Cautions 1. The high-speed CMOS inverter should be located as close as possible to the X1 and X2 pins.
2. Ensure that matching between the μPD70236A and the high-speed CMOS inverter is fully evaluated.

AC Characteristics (V$_{DD}$ = 2.7 to 3.6 V, Output pin load capacitance : C$_L$ = 100 pF)

(1) μPD70236A-16 (V$_{DD}$ = 2.7 to 3.6 V)

(1/4)

PARAMETER		SYMBOL	FIG.No.	TEST CONDITIONS	T$_A$ = –40 to +85 °C		UNIT
					MIN.	MAX.	
External clock input cycle	①	t$_{CYX}$	15–1		62.5	250	ns
External clock input high-level width	②	t$_{XKH}$	15–1		20		ns
External clock input low-level width	③	t$_{XKL}$	15–1		20		ns
External clock input rise time	④	t$_{XKR}$	15–1			10	ns
External clock input fall time	⑤	t$_{XKF}$	15–1			10	ns
CPU operating frequency	–	f$_X$	–		2	8	MHz
CLKOUT output frequency	⑥	t$_{CYK}$	15–1		125	500	ns
CLKOUT high-level width	⑦	t$_{XKH}$	15–1		0.5t$_{CYK}$–20		ns
CLKOUT low-level width	⑧	t$_{XKL}$	15–1		0.5t$_{CYK}$–20		ns
CLKOUT rise time	⑨	t$_{KR}$	15–1	0.2V$_{DD}$ → 0.7V$_{DD}$		20	ns
CLKOUT fall time	⑩	t$_{KF}$	15–1	0.7V$_{DD}$ → 0.2V$_{DD}$		20	ns
CLKOUT delay time (from external clock)	⑪	t$_{DXK}$	15–1		5	50	ns
PCLKOUT output frequency	⑫	t$_{CYPK}$	15–1		4t$_{CYX}$	1000	ns
PCLKOUT high-level width	⑬	t$_{PKH}$	15–1		2t$_{CYX}$–20		ns
PCLKOUT low-level width	⑭	t$_{PKL}$	15–1		2t$_{CYX}$–20		ns
PCLKOUT output rise time	⑮	t$_{PKR}$	15–1	0.2V$_{DD}$ → 0.7V$_{DD}$		20	ns
PCKLOUT output fall time	⑯	t$_{PKF}$	15–1	0.7V$_{DD}$ → 0.2V$_{DD}$		20	ns
Input rise time[Note 1]	⑰	t$_{IR}$		0.7V$_{DD}$ → 0.2V$_{DD}$		15	ns
Input fall time[Note 1]	⑱	t$_{IF}$		0.2V$_{DD}$ → 0.7V$_{DD}$		10	ns
Output rise time[Note 2]	⑲	t$_{OR}$		0.7V$_{DD}$ → 0.2V$_{DD}$		15	ns
Output fall time[Note 2]	⑳	t$_{OF}$		0.2V$_{DD}$ → 0.7V$_{DD}$		10	ns
$\overline{RESET}$ setup time (to CLKOUT↓)	㉑	t$_{SRSTK}$	15–2		30		ns
$\overline{RESET}$ hold time (from CLKOUT↓)	㉒	t$_{HKRST}$	15–2		15		ns
RESOUT output delay time (from CLKOUT↓)	㉓	t$_{DKRO}$	15–2		0	60	ns
$\overline{RESET}$ low-level width	㉔	t$_{WRSTL}$	15–2		6t$_{CYK}$		ns
$\overline{READY}$ setup time (to CLKOUT↑)	㉕	t$_{SRYK}$	15–3, etc.		10		ns
$\overline{READY}$ hold time (from CLKOUT↑)	㉖	t$_{HKRY}$	15–3, etc.		20		ns
$\overline{BCYST}$ high-level width	㉗	t$_{BCBCH}$	15–5, etc.		t$_{CYK}$(n+1)–15[Note 3]		ns
$\overline{BCYST}$ low-level width	㉘	t$_{BCBCL}$	15–5, etc.		t$_{CYK}$–15		ns
$\overline{BCYST}$ delay time from CLKOUT↓	㉙	t$_{DKBC}$	15–5, etc.		5	40	ns
$\overline{MRD}$ delay time from CLKOUT	㉚	t$_{DKMR}$	15–5, etc.		0	60	ns

Notes 1. Except external clock and $\overline{RESET}$
2. Except CLKOUT and PCLKOUT
3. n indicates the number of wait clock cycles inserted in the bus cycle. In a co-processor cycle, 1 (=TC cycle) must be added to n.

Remark The number in the symbol column correspond to the numbers in the timing charts.

μPD70236A-16 (V$_{DD}$ = 2.7 to 3.6 V)

(2/4)

PARAMETER	SYMBOL		FIG.No.	TEST CONDITIONS	T$_A$ = −40 to +85 °C		UNIT
					MIN.	MAX.	
$\overline{MRD}{\downarrow}$, $\overline{IORD}{\downarrow}$ delay time from address/status output	③	t$_{DARL}$	15–5, etc.		0.5t$_{CYK}$−20		ns
Data hold time (from $\overline{MRD}{\uparrow}$, from $\overline{IORD}{\uparrow}$)	㉜	t$_{HRD}$	15–5, etc.		0		ns
Address delay time from CLKOUT↓[Note 1]	㉝	t$_{DKA}$	15–5, etc.		4	45	ns
Data hold time (from R/$\overline{W}{\downarrow}$)	㉞	t$_{HRWD}$	15–5		0		ns
Status delay time from CLKOUT↓	㉟	t$_{DKST}$	15–5, etc.		5	45	ns
$\overline{DSTB}{\downarrow}$ output delay time from CLKOUT↑	㊱	t$_{DKDS}$	15–5, etc.		5	60	ns
$\overline{DSTB}{\uparrow}$ output delay time from CLKOUT	㊲	t$_{DKDSH}$	15–5, etc.		5	50	ns
$\overline{DSTB}{\downarrow}$ delay time from address/status output	㊳	t$_{DADSL}$	15–5, etc.		0.5t$_{CYK}$−20		ns
$\overline{DSTB}$ high-level width	㊴	t$_{DSDSH}$	15–5, etc.		0.5t$_{CYK}$−15		ns
$\overline{DSTB}$ low-level width	㊵	t$_{DSDSL}$	15–6, etc.		t$_{CYK}$(n+1)−15[Note 4]		ns
Data hold time (from $\overline{DSTB}{\uparrow}$)	㊶	t$_{HDSD}$	15–5, etc.		0		ns
Data hold time (from address/status change point)	㊷	t$_{HASD}$	15–5		0		ns
Control 1[Note 2] delay time from CLKOUT	㊸	t$_{DKCT1}$	15–21		0	60	ns
Control 2[Note 3] delay time from CLKOUT	㊹	t$_{DKCT2}$	15–5, etc.		0	60	ns
Data setup time (to CLKOUT↓)	㊺	t$_{SDK}$	15–5, etc.		10		ns
Data hold time (from CLKOUT↓)	㊻	t$_{HKD}$	15–5, etc.		10		ns
Output floating time from $\overline{DSTB}{\downarrow}$	㊼	t$_{DHZ}$	15–5, etc.			0	ns
Address/status hold time from $\overline{MWR}{\uparrow}$	㊽	t$_{HMWHA}$	15–6		0.5t$_{CYK}$−20		ns
$\overline{MWR}$ delay time from CLKOUT	㊾	t$_{DKMW}$	15–6, etc.		0	60	ns
$\overline{MWR}{\downarrow}$, $\overline{IOWR}{\downarrow}$ delay time from address/status output	㊿	t$_{DAWL}$	15–6, etc.		0.5t$_{CYK}$−20		ns
$\overline{MWR}$, $\overline{IOWR}$ low-level width	�51	t$_{WWL}$	15–6, etc.		t$_{CYK}$(n+1)−15[Note 4]		ns
Address/status hold time from $\overline{DSTB}{\uparrow}$	�52	t$_{HDSHA}$	15–6, etc.		0.5t$_{CYK}$−20		ns
Data output delay time from $\overline{DSTB}{\uparrow}$	�53	t$_{DDSHD}$	15–6, etc.		0.5t$_{CYK}$−20		ns
Data delay time from address/status output	�54	t$_{DAD}$	15–6, etc.		0.5t$_{CYK}$−20		ns
Output setting time from $\overline{DSTB}{\uparrow}$	�55	t$_{DLZ}$	15–6, etc.		0.5t$_{CYK}$−20		ns

Notes **1.** These specifications apply to the following delay times from the falling edge of the CLKOUT signal.   *

    (1) Address delay time

    (2) $\overline{BUSLOCK}$ delay time

    (3) Delay time of signals below immediately after release of bus hold:

        A23-A0, D15-D0, M/$\overline{IO}$, BUSST1, BUSST0, $\overline{UBE}$, $\overline{BCYST}$, $\overline{DSTB}$.

  2. Control 1 applies to the $\overline{MWR}$ and $\overline{IOWR}$ signals in a DMA cycle.

  3. Control 2 applies to the $\overline{BUFEN}$, $\overline{INTAK}$ and $\overline{REFRQ}$ setups.

  4. n indicates the number of wait clock cycles inserted in the bus cycle. In a co-processor cycle, 1 (=TC cycle) must be added to n.

Remarks **1.** The number in the symbol column correspond to the numbers in the timing charts.

     2. Regarding the five specifications ㉜ t$_{HRD}$, ㉞ t$_{HRWD}$, ㊶ t$_{HDSD}$, ㊷ t$_{HASD}$, and ㊻ t$_{HKD}$, at least one should be observed.

μPD70236A-16 (V_{DD} = 2.7 to 3.6 V)

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PARAMETER		SYMBOL	FIG.No.	TEST CONDITIONS	T_A = −40 to +85 °C		UNIT
					MIN.	MAX.	
Data output delay time from CLKOUT↑	⑤⑥	t_{DKD}	15–6, etc.		5	60	ns
Float delay time from CLKOUT	⑤⑦	t_{FK}	15–6, etc.		0	60	ns
IORD delay time from CLKOUT	⑤⑧	t_{DKIR}	15–7		0	60	ns
IOWR delay time from CLKOUT	⑤⑨	t_{DKIW}	15–8		0	60	ns
NMI, INTPn (n = 0 to 7), CPBUSY setup time (to CLKOUT↓)	⑥⓪	t_{SIK}	15–11		10		ns
NMI, INTPn (n = 0 to 7), CPBUSY hold time (from CLKOUT↓)	⑥①	t_{HKI}	15–11		5		ns
BS8/BS16 setup time (to CLKOUT↑)	⑥②	t_{SBSK}	15–13		5		ns
BS8/BS16 hold time (from CLKOUT↑)	⑥③	t_{HKBS}	15–13		5		ns
HLDRQ setup time (to CLKOUT↑)	⑥④	t_{SHQK}	15–14		5		ns
HLDRQ hold time (from CLKOUT↑)	⑥⑤	t_{HKHQ}	15–14		20		ns
HLDAK delay time from CLKOUT↑	⑥⑥	t_{DKHA}	15–14		5	45	ns
HLDAK delay time from output float	⑥⑦	t_{DFHA}	15–14		0.5t_{CYK}−20		ns
INTPn(n = 0 to 7) low-level width	⑥⑧	t_{IPIPL}	15–17		100		ns
TCTLn (n = 0 to 2) setup time (to CLKOUT↓)	⑥⑨	t_{SGK}	15–18		100		ns
TCTLn (n = 0 to 2) hold time (from CLKOUT↓)	⑦⓪	t_{HKG}	15–18		100		ns
TCTLn (n = 0 to 2) high-level width	⑦①	t_{GGH}	15–18, etc.		50		ns
TCTLn (n = 0 to 2) low-level width	⑦②	t_{GGL}	15–18, etc.		50		ns
TOUTn (n = 0 to 2) output delay time (from TCTLn (n = 0 to 2)↓)	⑦③	t_{DGTO}	15–18, etc.			120	ns
TOUTn (n = 0 to 2) output delay time (from CLKOUT↓)	⑦④	t_{DKTO}	15–18			100	ns
TCLK cycle	⑦⑤	t_{CYTK}	15–19		125	DC	ns
TCLK high-level width	⑦⑥	t_{TKTKH}	15–19		30		ns
TCLK low-level width	⑦⑦	t_{TKTKL}	15–19		45		ns
TCLK rise time	⑦⑧	t_{TKR}	15–19			15	ns
TCLK fall time	⑦⑨	t_{TKF}	15–19			15	ns
TCTLn (n = 0 to 2) hold time (from TCLK↑)	⑧⓪	t_{HTKG}	15–19		100		ns
TCTLn (n = 0 to 2) setup time (to TCLK↑)	⑧①	t_{SGTK}	15–19		50		ns
TOUTn (n = 0 to 2) output delay time (from TCLK↓)	⑧②	t_{DTKTO}	15–19			150	ns
RxD setup time (to SCU internal clock↓)	⑧③	t_{SRX}	15–20		100		ns
RxD hold time (from SCU internal clock↓)	⑧④	t_{HRX}	15–20		100		ns
TxD delay time from TOUT1↑	⑧⑤	t_{DTX}	15–20			500	ns
DMAAKn (n = 0 to 3) delay time from CLKOUT↑	⑧⑥	t_{DKHDA}	15–21		0	60	ns
MRD, IORD↓ delay time from CLKOUT↓	⑧⑦	t_{DKRL}	15–21		0	60	ns
MRD, IORD↑ delay time from CLKOUT↓	⑧⑧	t_{DKRH}	15–21		0	60	ns
DMAAKn (n = 0 to 3)↑ delay time (from IORD↑)	⑧⑨	t_{DRHDAH}	15–21		0.5t_{CYK}−20		ns
IORD↓, IOWR↓ delay time (from DMAAKn (n = 0 to 3)↓)	⑨⓪	t_{DDARW}	15–21		0.5t_{CYK}−20		ns

Remark The number in the symbol column correspond to the numbers in the timing charts.

μPD70236A-16 (VDD = 2.7 to 3.6 V)

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PARAMETER	SYMBOL		FIG.No.	TEST CONDITIONS	TA = −40 to +85 °C		UNIT
					MIN.	MAX.	
IORD↑ delay time (from MWR↑) MRD↑ delay time (from IOWR↑)	⑨①	tDWHRH	15–21		0		ns
IORD, MRD low-level width	⑨②	tRR	15–21		tCYK(n+2)−60 Note 1		ns
IOWR, MWR low-level width (extended write)	⑨③	tWW1	15–21	Extended write	tCYK(n+2)−60 Note 1		ns
IOWR, MWR low-level width (normal write)	⑨④	tWW2	15–21	Normal write	tCYK(n+1)−60 Note 1		ns
TC output delay time (from CLKOUT↑)	⑨⑤	tDKTCL	15–22		0	60	ns
TC OFF output delay time (from CLKOUT↑)	⑨⑥	tDKTCF	15–22		0	60	ns
TC pull-up delay time (from CLKOUT↑) Note 2	⑨⑦	tDKTCH	15–22	RTC = 2.2 kΩ	0	2tCYK−20	ns
TC low-level width	⑨⑧	tTCTCL	15–22		tCYK(n+1)−25 Note 1		ns
END setup time (to CLKOUT↑)	⑨⑨	tSEDK	15–22		20		ns
END low-level width	⑩⓪	tEDEDL	15–22		100		ns
DMARQn (n = 0 to 3) setup time (to CLKOUT↑)	⑩①	tSDQK	15–22, etc.		20		ns
DMAAKn (n = 0 to 3) delay time from CLKOUT↓	⑩②	tDKLDA	15–23		0	60	ns
MRD high-level width	⑩③	tMRMRH	15–5		0.5tCYK−15		ns
Data set time from MRD↑	⑩④	tDMRHLZ	15–6, etc.		0.5tCYK−20		ns
Data output delay time from MRD↑	⑩⑤	tDMRHD	15–6, etc.		0.5tCYK−20		ns
Cascade address delay time from CLKOUT	⑩⑥	tDKCA	15–15, etc.		4	45	ns
INTAK high-level width	⑩⑦	tIAIAH	15–16		2.5tCYK−15		ns
PCLKOUT delay time from CLKOUT	⑩⑧	tDKPK	15–1	CLKC = 00		±5	ns
IOWR, MWR↓ delay time from MRD, IORD↓	⑩⑨	tDRLWL	15–21	Normal write	tCYK−20		ns

*

Notes 1. n indicates the number of wait clock cycles inserted in the bus cycle.

2. It is assumed that the TC pin is connected with the pull-up resistor RTC.

Remark The number in the symbol column correspond to the numbers in the timing charts.

(2) µPD70236A-20 (V$_{DD}$ = 2.7 to 3.6 V)

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PARAMETER	SYMBOL		FIG.No.	TEST CONDITIONS	T$_A$ = −40 to +85 °C		UNIT
					MIN.	MAX.	
External clock input cycle	①	tcYX	15–1		50	250	ns
External clock input high-level width	②	tXKH	15–1		15		ns
External clock input low-level width	③	tXKL	15–1		15		ns
External clock input rise time	④	tXKR	15–1			10	ns
External clock input fall time	⑤	tXKF	15–1			10	ns
CPU operating frequency	–	fx	–		2	10	MHz
CLKOUT output frequency	⑥	tcYK	15–1		100	500	ns
CLKOUT high-level width	⑦	tKKH	15–1		0.5tcYK−20		ns
CLKOUT low-level width	⑧	tKKL	15–1		0.5tcYK−20		ns
CLKOUT rise time	⑨	tKR	15–1	0.2V$_{DD}$ → 0.7V$_{DD}$		20	ns
CLKOUT fall time	⑩	tKF	15–1	0.7V$_{DD}$ → 0.2V$_{DD}$		20	ns
CLKOUT delay time (from external clock)	⑪	tDXK	15–1		5	50	ns
PCLKOUT output frequency	⑫	tcYPK	15–1		4tcYX	1000	ns
PCLKOUT high-level width	⑬	tPKH	15–1		2tcYX−20		ns
PCLKOUT low-level width	⑭	tPKL	15–1		2tcYX−20		ns
PCLKOUT output rise time	⑮	tPKR	15–1	0.2V$_{DD}$ → 0.7V$_{DD}$		20	ns
PCKLOUT output fall time	⑯	tPKF	15–1	0.7V$_{DD}$ → 0.2V$_{DD}$		20	ns
Input rise time[Note 1]	⑰	tIR		0.7V$_{DD}$ → 0.2V$_{DD}$		15	ns
Input fall time[Note 1]	⑱	tIF		0.2V$_{DD}$ → 0.7V$_{DD}$		10	ns
Output rise time[Note 2]	⑲	tOR		0.7V$_{DD}$ → 0.2V$_{DD}$		15	ns
Output fall time[Note 2]	⑳	tOF		0.2V$_{DD}$ → 0.7V$_{DD}$		10	ns
RESET setup time (to CLKOUT↓)	㉑	tsRSTK	15–2		30		ns
RESET hold time (from CLKOUT↓)	㉒	tHKRST	15–2		15		ns
RESOUT output delay time (from CLKOUT↓)	㉓	tDKRO	15–2		0	60	ns
RESET low-level width	㉔	twRSTL	15–2		6tcYK		ns
READY setup time (to CLKOUT↑)	㉕	tsRYK	15–3, etc.		10		ns
READY hold time (from CLKOUT↑)	㉖	tHKRY	15–3, etc.		20		ns
BCYST high-level width	㉗	tBCBCH	15–5, etc.		tcYK(n+1)−15[Note 3]		ns
BCYST low-level width	㉘	tBCBCL	15–5, etc.		tcYK−15		ns
BCYST delay time from CLKOUT↓	㉙	tDKBC	15–5, etc.		5	40	ns
MRD delay time from CLKOUT	㉚	tDKMR	15–5, etc.		0	60	ns

Notes 1. Except external clock and RESET

2. Except CLKOUT and PCLKOUT

3. n indicates the number of wait clock cycles inserted in the bus cycle. In a co-processor cycle, 1 (=TC cycle) must be added to n.

Remark The number in the symbol column correspond to the numbers in the timing charts.

µPD70236A-20 (V$_{DD}$ = 2.7 to 3.6 V)

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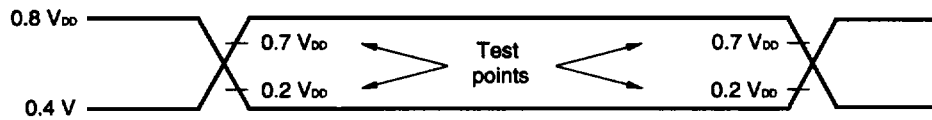
PARAMETER	SYMBOL	FIG.No.	TEST CONDITIONS	T$_A$ = −40 to +85 °C		UNIT
				MIN.	MAX.	
MRD↓, IORD↓ delay time from address/status output	③① t$_{DARL}$	15–5, etc.		0.5t$_{CYK}$−20		ns
Data hold time (from MRD↑, from IORD↑)	③② t$_{HRD}$	15–5, etc.		0		ns
Address delay time from CLKOUT↓$^{Note 1}$	③③ t$_{DKA}$	15–5, etc.		4	45	ns
Data hold time (from R/W↓)	③④ t$_{HRWD}$	15–5		0		ns
Status delay time from CLKOUT↓	③⑤ t$_{DKST}$	15–5, etc.		5	45	ns
DSTB↓ output delay time from CLKOUT↑	③⑥ t$_{DKDS}$	15–5, etc.		5	60	ns
DSTB↑ output delay time from CLKOUT	③⑦ t$_{DKDSH}$	15–5, etc.		5	50	ns
DSTB↓ delay time from address/status output	③⑧ t$_{DADSL}$	15–5, etc.		0.5t$_{CYK}$−20		ns
DSTB high-level width	③⑨ t$_{DSDSH}$	15–5, etc.		0.5t$_{CYK}$−15		ns
DSTB low-level width	④⓪ t$_{DSDSL}$	15–6, etc.		t$_{CYK}$(n+1)−15$^{Note 4}$		ns
Data hold time (from DSTB↑)	④① t$_{HDSD}$	15–5, etc.		0		ns
Data hold time (from address/status change point)	④② t$_{HASD}$	15–5		0		ns
Control 1$^{Note 2}$ delay time from CLKOUT	④③ t$_{DKCT1}$	15–21		0	60	ns
Control 2$^{Note 3}$ delay time from CLKOUT	④④ t$_{DKCT2}$	15–5, etc.		0	60	ns
Data setup time (to CLKOUT↓)	④⑤ t$_{SDK}$	15–5, etc.		10		ns
Data hold time (from CLKOUT↓)	④⑥ t$_{HKD}$	15–5, etc.		10		ns
Output floating time from DSTB↓	④⑦ t$_{DHZ}$	15–5, etc.			0	ns
Address/status hold time from MWR↑	④⑧ t$_{HMWHA}$	15–6		0.5t$_{CYK}$−20		ns
MWR delay time from CLKOUT	④⑨ t$_{DKMW}$	15–6, etc.		0	60	ns
MWR↓, IOWR↓ delay time from address/status output	⑤⓪ t$_{DAWL}$	15–6, etc.		0.5t$_{CYK}$−20		ns
MWR, IOWR low-level width	⑤① t$_{WWL}$	15–6, etc.		t$_{CYK}$(n+1)−15$^{Note 4}$		ns
Address/status hold time from DSTB↑	⑤② t$_{HDSHA}$	15–6, etc.		0.5t$_{CYK}$−20		ns
Data output delay time from DSTB↑	⑤③ t$_{DDSHD}$	15–6, etc.		0.5t$_{CYK}$−20		ns
Data delay time from address/status output	⑤④ t$_{DAD}$	15–6, etc.		0.5t$_{CYK}$−20		ns
Output setting time from DSTB↑	⑤⑤ t$_{DLZ}$	15–6, etc.		0.5t$_{CYK}$−20		ns

★ **Notes** 1. These specifications apply to the following delay times from the falling edge of the CLKOUT signal.

   (1) Address delay time
   (2) BUSLOCK delay time
   (3) Delay time of signals below immediately after release of bus hold:
       A23-A0, D15-D0, M/IO, BUSST1, BUSST0, UBE, BCYST, DSTB.

2. Control 1 applies to the MWR and IOWR signals in a DMA cycle.

3. Control 2 applies to the BUFEN, INTAK and REFRQ setups.

4. n indicates the number of wait clock cycles inserted in the bus cycle. In a co-processor cycle, 1 (=TC cycle) must be added to n.

Remarks 1. The number in the symbol column correspond to the numbers in the timing charts.

2. Regarding the five specifications ③② t$_{HRD}$, ③④ t$_{HRWD}$, ④① t$_{HDSD}$, ④② t$_{HASD}$ and ④⑥ t$_{HKD}$, at least one should be observed.

µPD70236A-20 (V_DD = 2.7 to 3.6 V)

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PARAMETER		SYMBOL	FIG.No.	TEST CONDITIONS	T_A = −40 to +85 °C		UNIT
					MIN.	MAX.	
Data output delay time from CLKOUT↑	⑤⑥	t_DKD	15–6, etc.		5	60	ns
Float delay time from CLKOUT	⑤⑦	t_FK	15–6, etc.		0	60	ns
IORD delay time from CLKOUT	⑤⑧	t_DKIR	15–7		0	60	ns
IOWR delay time from CLKOUT	⑤⑨	t_DKIW	15–8		0	60	ns
NMI, INTPn (n = 0 to 7), CPBUSY setup time (to CLKOUT↓)	⑥⓪	t_SIK	15–11		10		ns
NMI, INTPn(n = 0 to 7), CPBUSY hold time (from CLKOUT↓)	⑥①	t_HKI	15–11		15		ns
BS8/BS16 setup time (to CLKOUT↑)	⑥②	t_SBSK	15–13		15		ns
BS8/BS16 hold time (from CLKOUT↑)	⑥③	t_HKBS	15–13		15		ns
HLDRQ setup time (to CLKOUT↑)	⑥④	t_SHQK	15–14		15		ns
HLDRQ hold time (from CLKOUT↑)	⑥⑤	t_HKHQ	15–14		20		ns
HLDAK delay time from CLKOUT↑	⑥⑥	t_DKHA	15–14		5	45	ns
HLDAK delay time from output float	⑥⑦	t_DFHA	15–14		0.5t_CYK−20		ns
INTPn(n = 0 to 7) low-level width	⑥⑧	t_IPIPL	15–17		100		ns
TCTLn (n = 0 to 2) setup time (to CLKOUT↓)	⑥⑨	t_SGK	15–18		100		ns
TCTLn (n = 0 to 2) hold time (from CLKOUT↓)	⑦⓪	t_HKG	15–18		100		ns
TCTLn (n = 0 to 2) high-level width	⑦①	t_GGH	15–18, etc.		50		ns
TCTLn (n = 0 to 2) low-level width	⑦②	t_GGL	15–18, etc.		50		ns
TOUTn (n = 0 to 2) output delay time (from TCTLn (n = 0 to 2)↓)	⑦③	t_DGTO	15–18, etc.			120	ns
TOUTn (n = 0 to 2) output delay time (from CLKOUT↓)	⑦④	t_DKTO	15–18			100	ns
TCLK cycle	⑦⑤	t_CYTK	15–19		100	DC	ns
TCLK high-level width	⑦⑥	t_TKTKH	15–19		30		ns
TCLK low-level width	⑦⑦	t_TKTKL	15–19		45		ns
TCLK rise time	⑦⑧	t_TKR	15–19			15	ns
TCLK fall time	⑦⑨	t_TKF	15–19			15	ns
TCTLn (n = 0 to 2) hold time (from TCLK↑)	⑧⓪	t_HTKG	15–19		100		ns
TCTLn (n = 0 to 2) setup time (to TCLK↑)	⑧①	t_SGTK	15–19		50		ns
TOUTn (n = 0 to 2) output delay time (from TCLK↓)	⑧②	t_DTKTO	15–19			150	ns
RxD setup time (to SCU internal clock↓)	⑧③	t_SRX	15–20		1000		ns
RxD hold time (from SCU internal clock↓)	⑧④	t_HRX	15–20		1000		ns
TxD delay time from TOUT1↑	⑧⑤	t_DTX	15–20			500	ns
DMAAKn (n = 0 to 3) delay time from CLKOUT↑	⑧⑥	t_DKHDA	15–21		0	60	ns
MRD, IORD↓ delay time from CLKOUT↓	⑧⑦	t_DKRL	15–21		0	60	ns
MRD, IORD↑ delay time from CLKOUT↓	⑧⑧	t_DKRH	15–21		0	60	ns
DMAAKn (n = 0 to 3)↑ delay time (from IORD↑)	⑧⑨	t_DRHDAH	15–21		0.5t_CYK−20		ns
IORD↓,IOWR↓ delay time (from DMAAKn (n = 0 to 3)↓)	⑨⓪	t_DDARW	15–21		0.5t_CYK−20		ns

Remark   The number in the symbol column correspond to the numbers in the timing charts.

μPD70236A-20 (V_DD = 2.7 to 3.6 V)

(4/4)

PARAMETER	SYMBOL	FIG.No.	TEST CONDITIONS	T_A = −40 to +85 °C MIN.	MAX.	UNIT
IORD↑ delay time (from MWR↑) / MRD↑ delay time (from IOWR↑)	�91 t_DWHRH	15–21		0		ns
IORD, MRD low-level width	�92 t_RR	15–21		$t_{CYK}(n+2)-60$[Note 1]		ns
IOWR, MWR low-level width (extended write)	�93 t_WW1	15–21	Extended write	$t_{CYK}(n+2)-60$[Note 1]		ns
IOWR, MWR low-level width (normal write)	�94 t_WW2	15–21	Normal write	$t_{CYK}(n+1)-60$[Note 1]		ns
TC output delay time (from CLKOUT↑)	�95 t_DKTCL	15–22		0	60	ns
TC OFF output delay time (from CLKOUT↑)	�96 t_DKTCF	15–22		0	60	ns
TC pull-up delay time (from CLKOUT↑)[Note 2]	�97 t_DKTCH	15–22	R_TC = 2.2 kΩ	0	$2t_{CYK}-20$	ns
TC low-level width	�98 t_TCTCL	15–22		$t_{CYK}(n+1)-25$[Note 1]		ns
END setup time (to CLKOUT↑)	�99 t_SEDK	15–22		20		ns
END low-level width	⑩⓪ t_EDEDL	15–22		100		ns
DMARQn (n = 0 to 3) setup time (to CLKOUT↑)	⑩① t_SDQK	15–22, etc.		20		ns
DMAAKn (n = 0 to 3) delay time from CLKOUT↓	⑩② t_DKLDA	15–23		0	60	ns
MRD high-level width	⑩③ t_MRMRH	15–5		$0.5t_{CYK}-15$		ns
Data set time from MRD↑	⑩④ t_DMRHLZ	15–6, etc.		$0.5t_{CYK}-20$		ns
Data output delay time from MRD↑	⑩⑤ t_DMRHD	15–6, etc.		$0.5t_{CYK}-20$		ns
Cascade address delay time from CLKOUT	⑩⑥ t_DKCA	15–15, etc.		4	45	ns
INTAK high-level width	⑩⑦ t_IAIAH	15–16		$2.5t_{CYK}-15$		ns
PCLKOUT delay time from CLKOUT	⑩⑧ t_DKPK	15–1	CLKC = 00		±5	ns
IOWR, MWR↓ delay time from MRD, IORD↓	⑩⑨ t_DRLWL	15–21	Normal write	$t_{CYK}-20$		ns

Notes 1. n indicates the number of wait clock cycles inserted in the bus cycle.

     2. It is assumed that the TC pin is connected with the pull-up resistor R_TC.

Remark The number in the symbol column correspond to the numbers in the timing charts.

AC Test Input Waveform (Except X1)

$0.8 V_{DD}$
$0.4 V$
$0.7 V_{DD}$
$0.2 V_{DD}$
Test points
$0.7 V_{DD}$
$0.2 V_{DD}$

AC Test Input Waveform (X1)

V_{DD}
$0 V$
$0.8 V_{DD}$
$0.2 V_{DD}$
Test points
$0.8 V_{DD}$
$0.2 V_{DD}$

AC Test Output Test Points

$0.7 V_{DD}$
$0.2 V_{DD}$
Test points
$0.7 V_{DD}$
$0.2 V_{DD}$

Load Conditions

DUT
$C_L = 100pF$

Caution If the load capacitance exceeds 100 pF due to the construction of the circuit, the load capacitance of this device should be reduced to 100 pF or less by insertion of a buffer, etc.

15.4 RELATIVE SPECIFICATIONS

*

When two signals change with a phase difference of 0.5n (n = 1, 2, 3, . . .) in relation to CLKOUT as signal A and signal B in the figure below, the minimum value of the relative specifications (delay time from signal A ↑ to signal B ↑) of the two signals is as shown below.
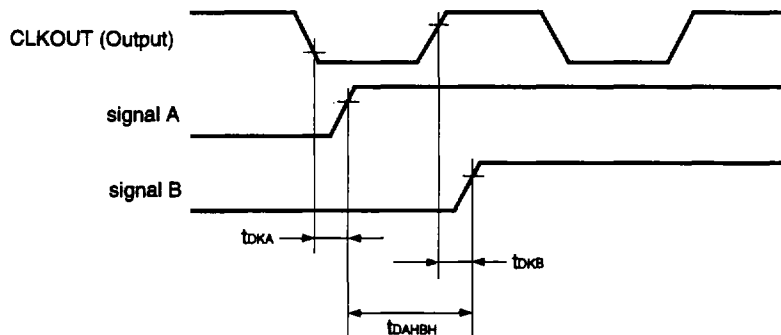
Remark t_DKA   : Delay time from CLKOUT ↓ to signal A ↑
            t_DKB   : Delay time from CLKOUT ↑ to signal B ↑
            t_DAHBH   : Delay time from signal A ↑ to signal B ↑

Table 15-1 V53A Relative Specifications

Symbol	Power supply voltage (V_{DD})	μPD70236A-10	μPD70236A-12	μPD70236A-16	μPD70236A-20	Unit
t_DAHBH (MIN.)	5 V ± 10 %	0.5n x t_CYK − 15	0.5n x t_CYK − 15	0.5n x t_CYK − 15	0.5n x t_CYK − 12	ns
	3.6 to 4.5 V	—	—	0.5n x t_CYK − 15	0.5n x t_CYK − 15	ns
	2.7 to 3.6 V	—	—	0.5n x t_CYK − 20	0.5n x t_CYK − 20	ns

15.5 TIMING CHART

The timing chart of the μPD70236A is described below.

On this timing chart, it is assumed that the WCU programmable wait is 0.

Fig. 15-1 Clock Timing

External Clock (Input) (X1)

CLKOUT (Output)

PCLKOUT (Output)

Fig. 15-2 Reset Timing

CLKOUT (Output)

RESET (Input)

RESOUT (Output)
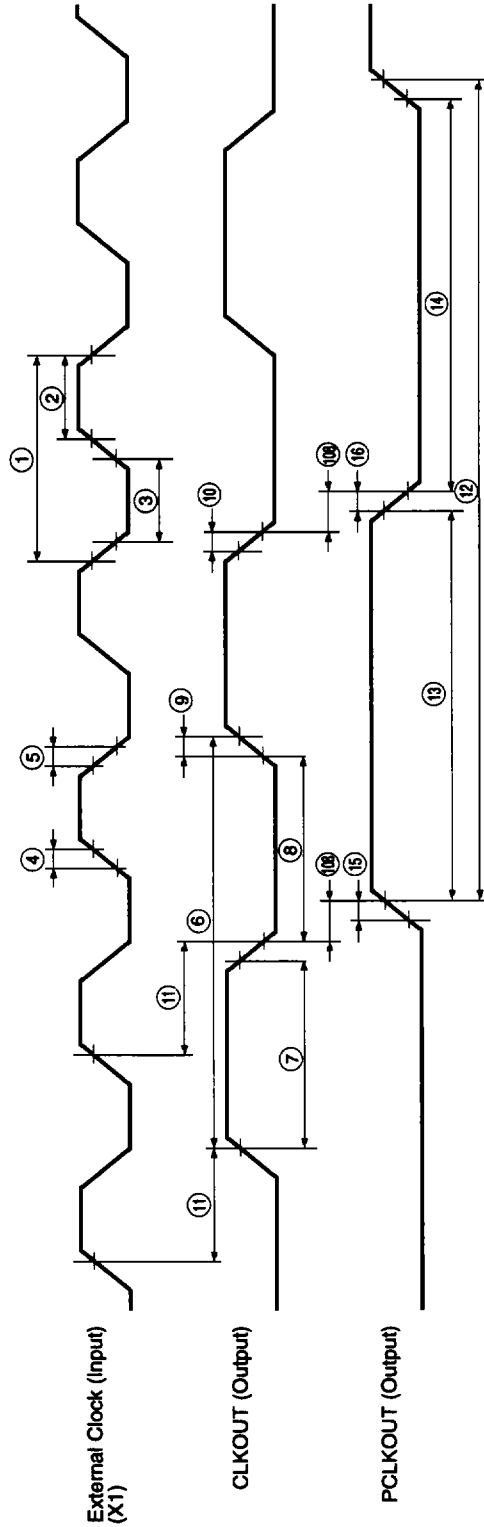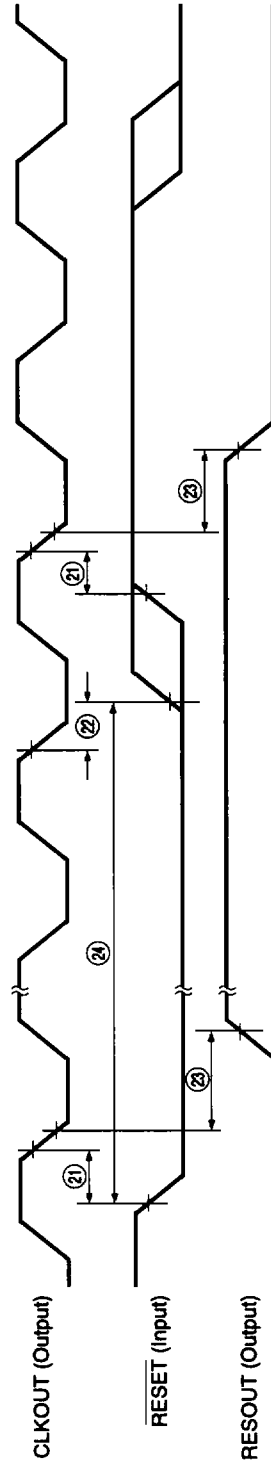
Remark RESET can be input asynchronously with respect to CLKOUT.

Fig. 15-3 CPU Ready Timing (No Wait)
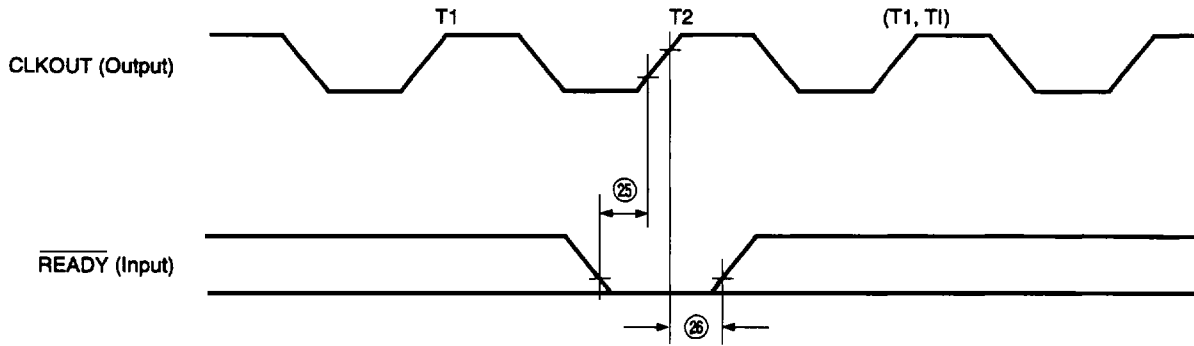
Fig. 15-4 CPU Ready Timing (1 Wait)
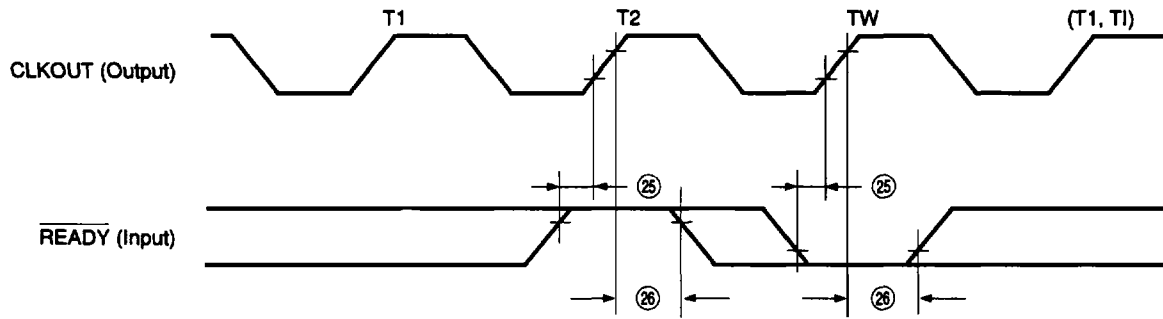
Fig. 15-5 Basic Read Cycle (No Wait)
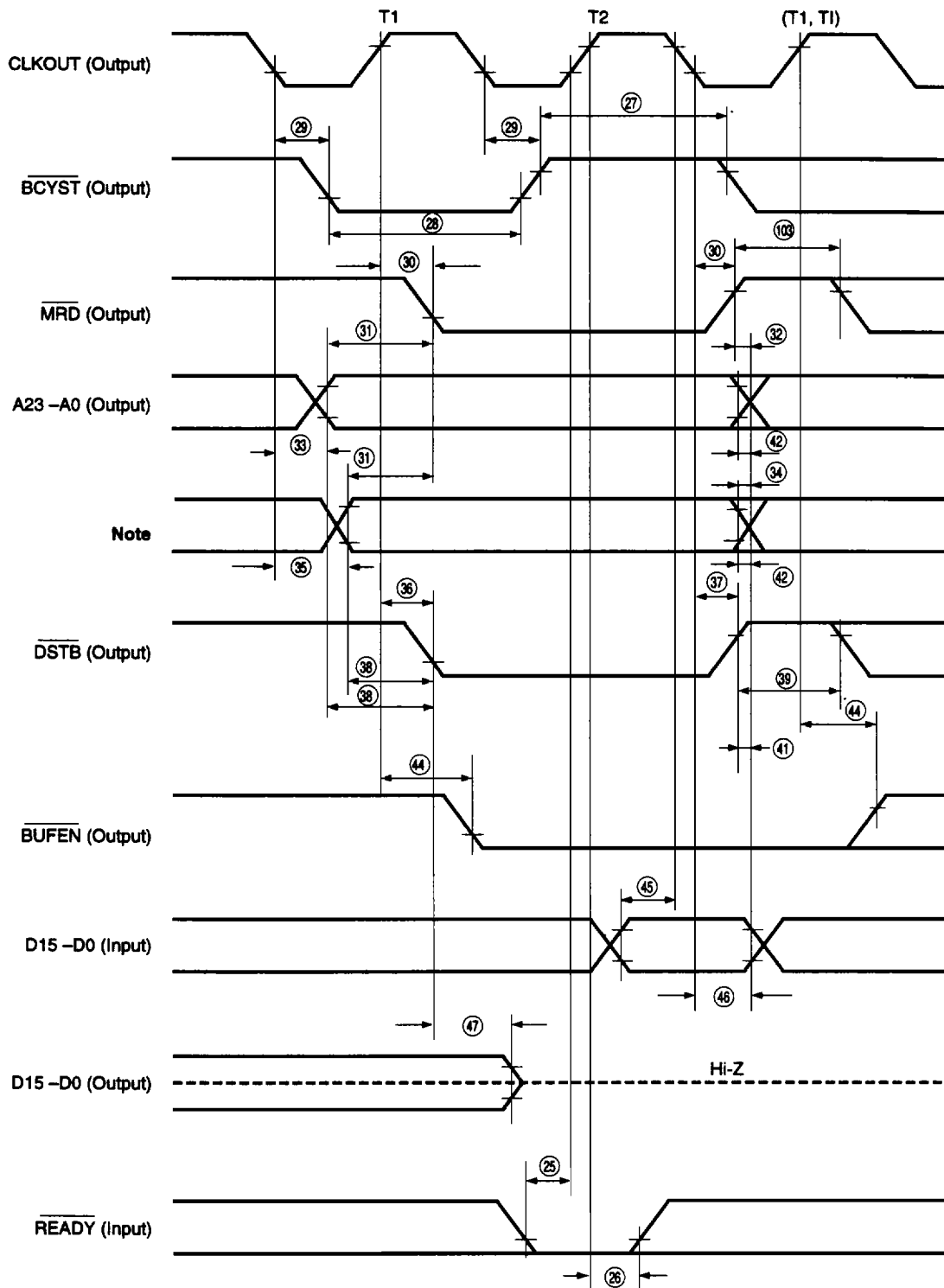
Note   R/W, M/IO, BUSST2, BUSST1, BUSST0, UBE, AEX (all output)

Fig. 15-6 Basic Write Cycle (No Wait)
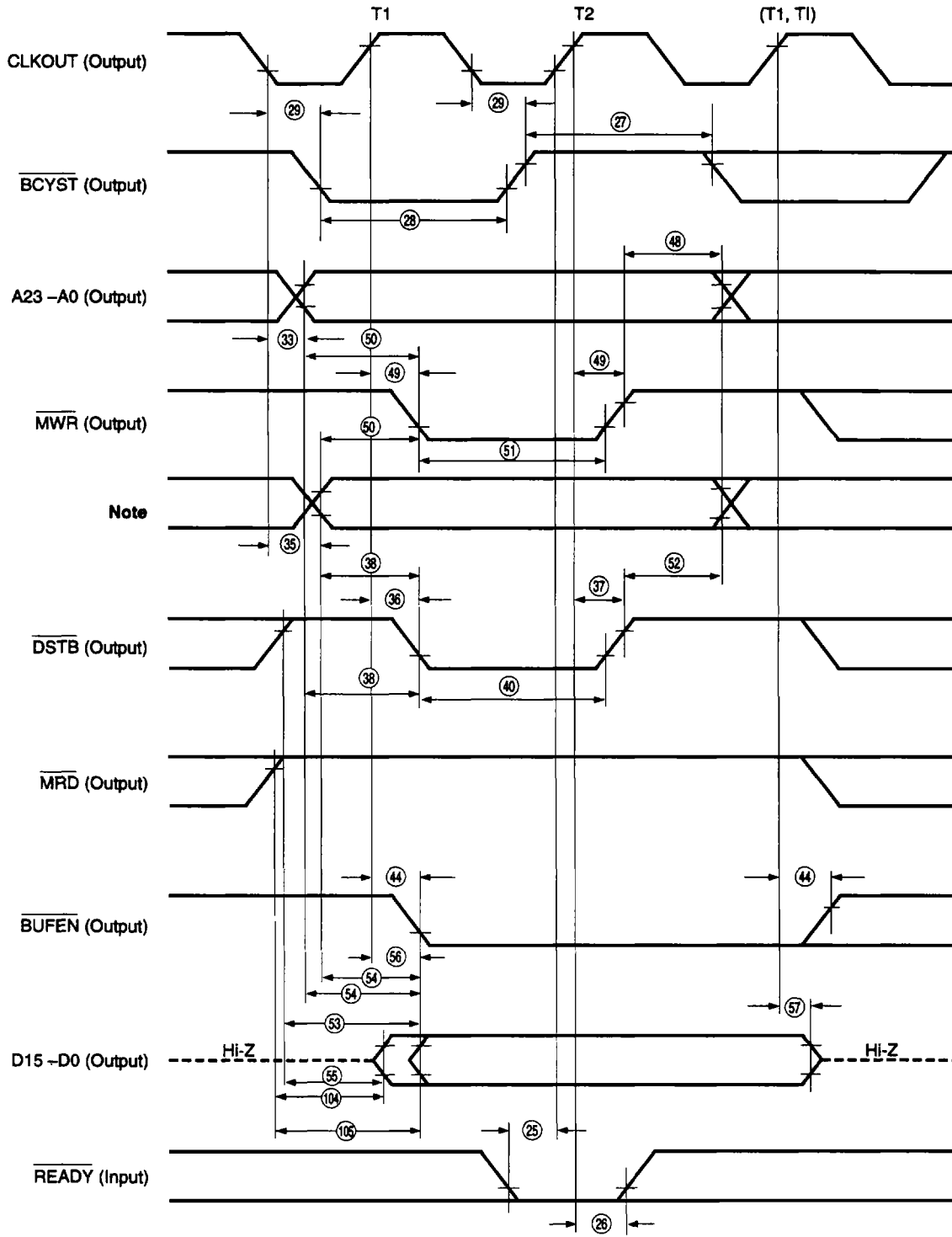
Note R/W̄, M/ĪŌ, BUSST2, BUSST1, BUSST0, ŪBĒ, AEX (all output)

Fig. 15-7 External I/O Read Cycle (No Wait)
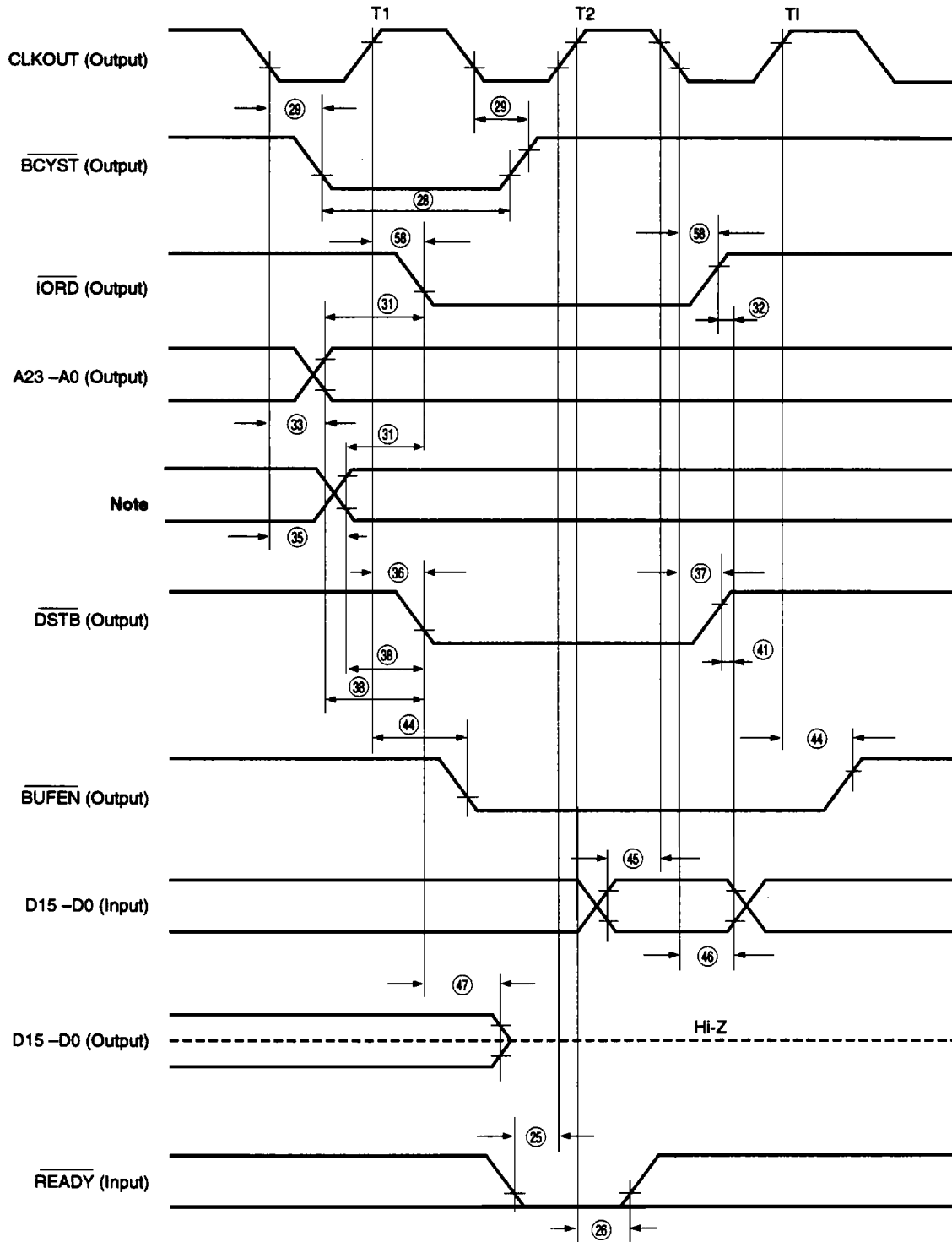
Note   R/W̄, M/IŌ, BUSST2, BUSST1, BUSST0, ŪBE, AEX (all output)

Fig. 15-8 External I/O Write Cycle (No Wait)
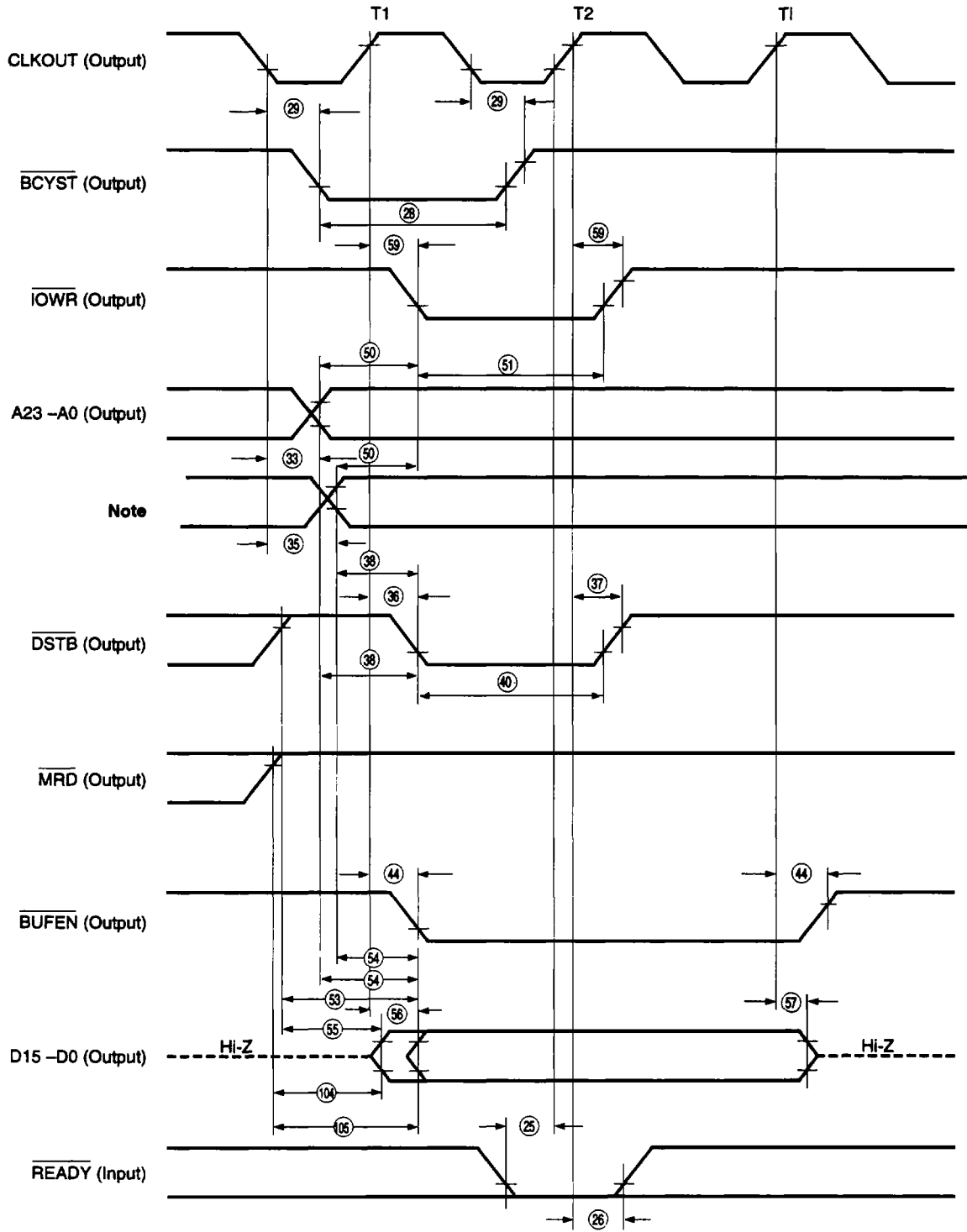
Note R/W̄, M/ĪŌ, BUSST2, BUSST1, BUSST0, ŪBE, AEX (all output)

Fig. 15-9 Internal I/O Read Cycle

Note R/W̄, M/IŌ, BUSST2, BUSST1, BUSST0, ŪBE, AEX (all output)

CLKOUT (Output)

A23–A0 (Output)

B̄C̄ȲS̄T̄ (Output)
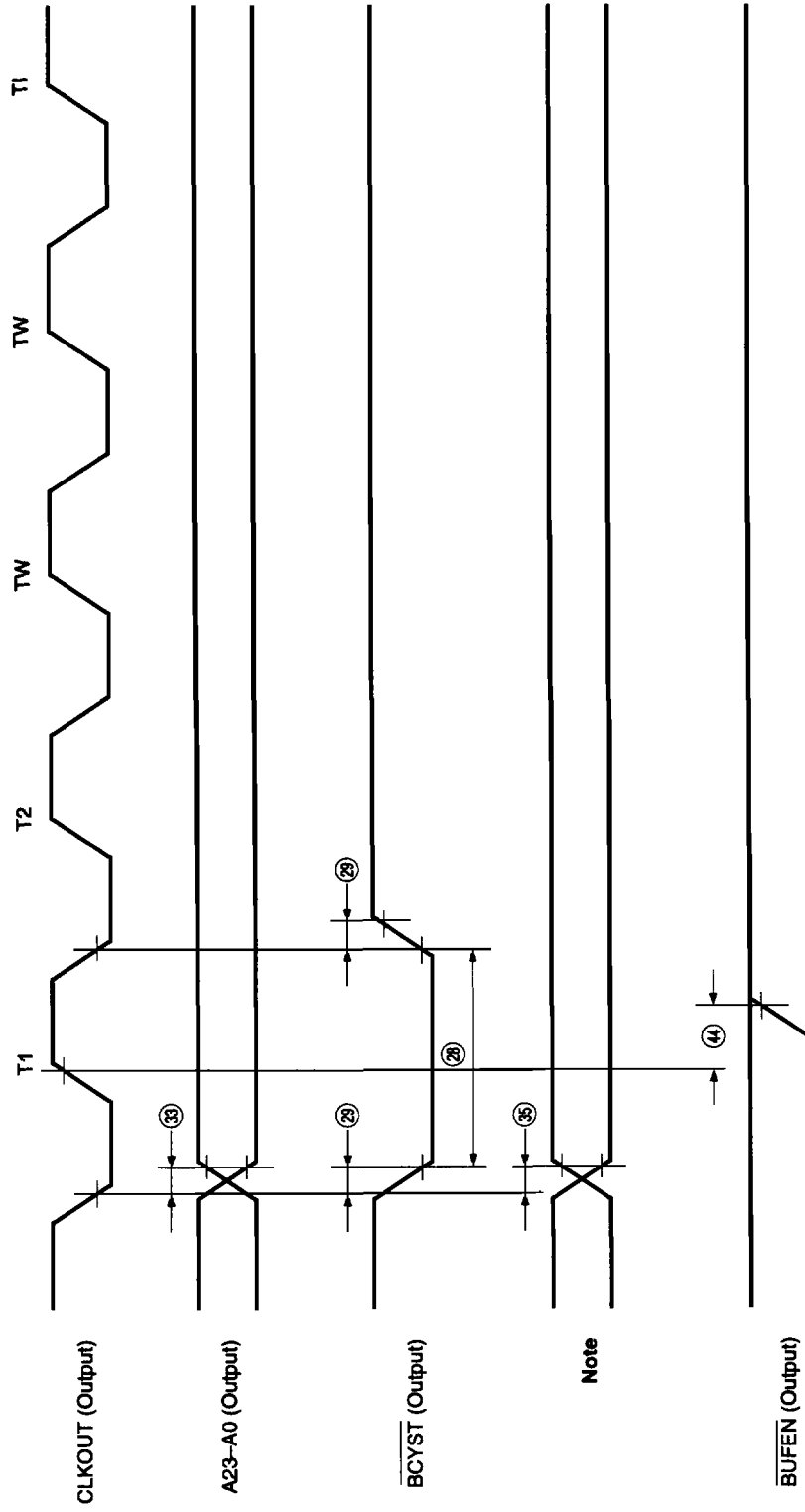
Note

B̄Ū̄F̄Ē̄N̄ (Output)

Fig. 15-10 Internal I/O Write Cycle
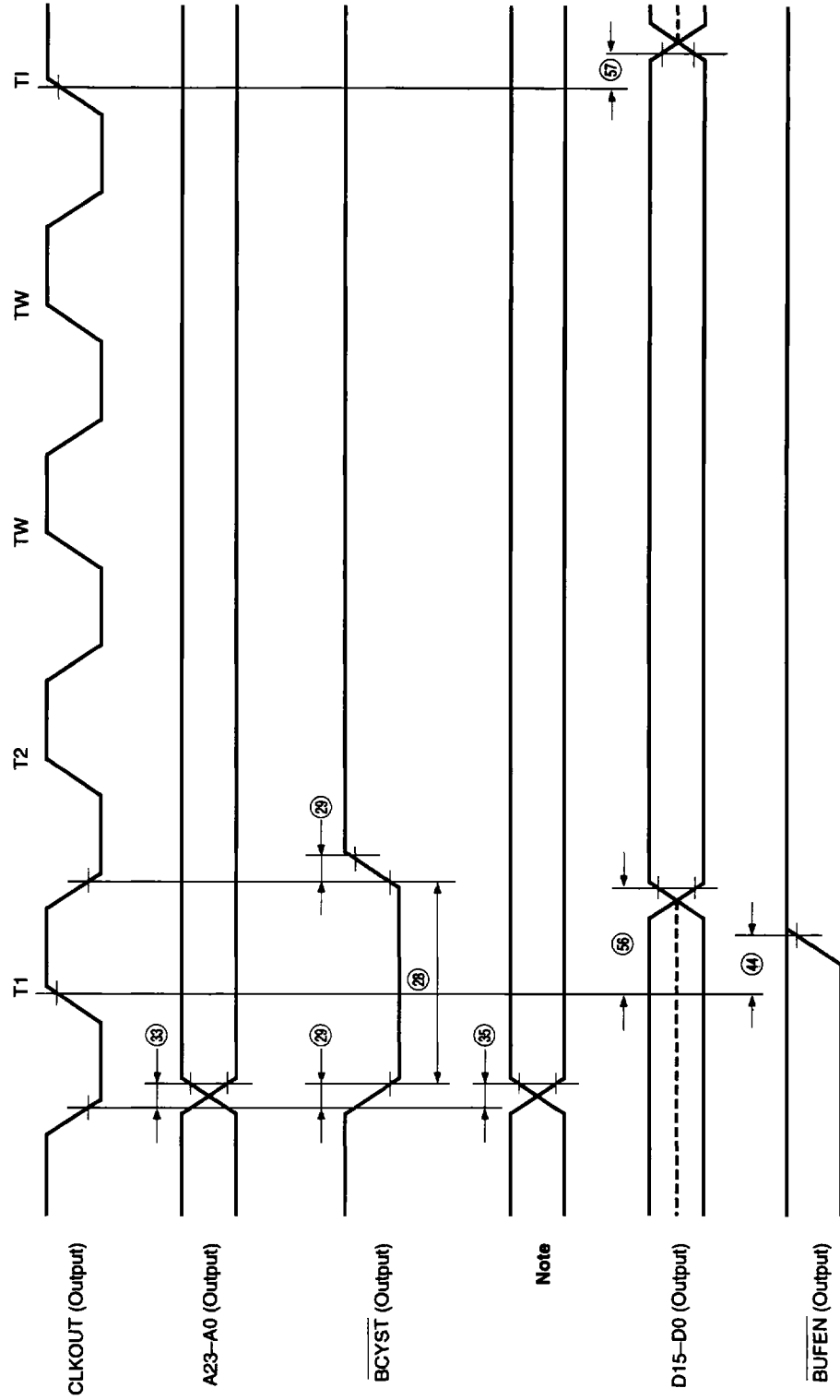
Note R/W̄, M/ĪŌ, BUSST2, BUSST1, BUSST0, ŪBE, AEX (all output)

Remark A dashed line indicates high impedance.

Fig. 15-11 Input Setup & Input Hold Times
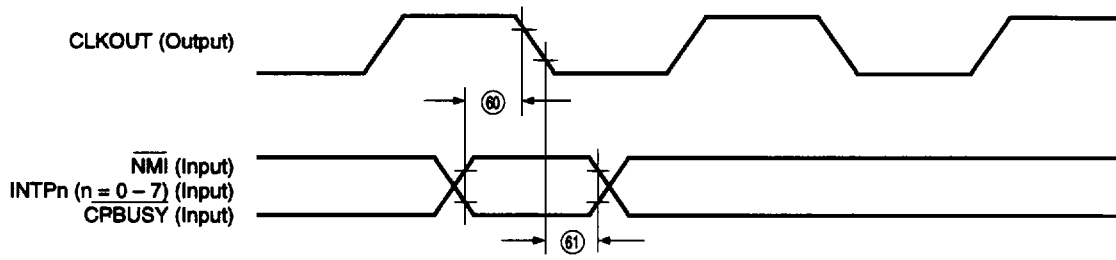
Remark $\overline{\text{NMI}}$, INTP0 to INTP7, and $\overline{\text{CPBUSY}}$ can be input asynchronously with respect to CLKOUT.

Fig. 15-12 Bus Lock
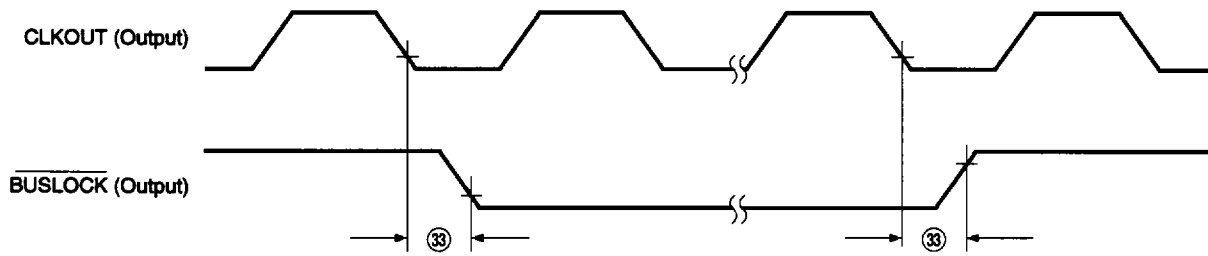
Fig. 15-13 Bus Sizing Cycle (No Wait)
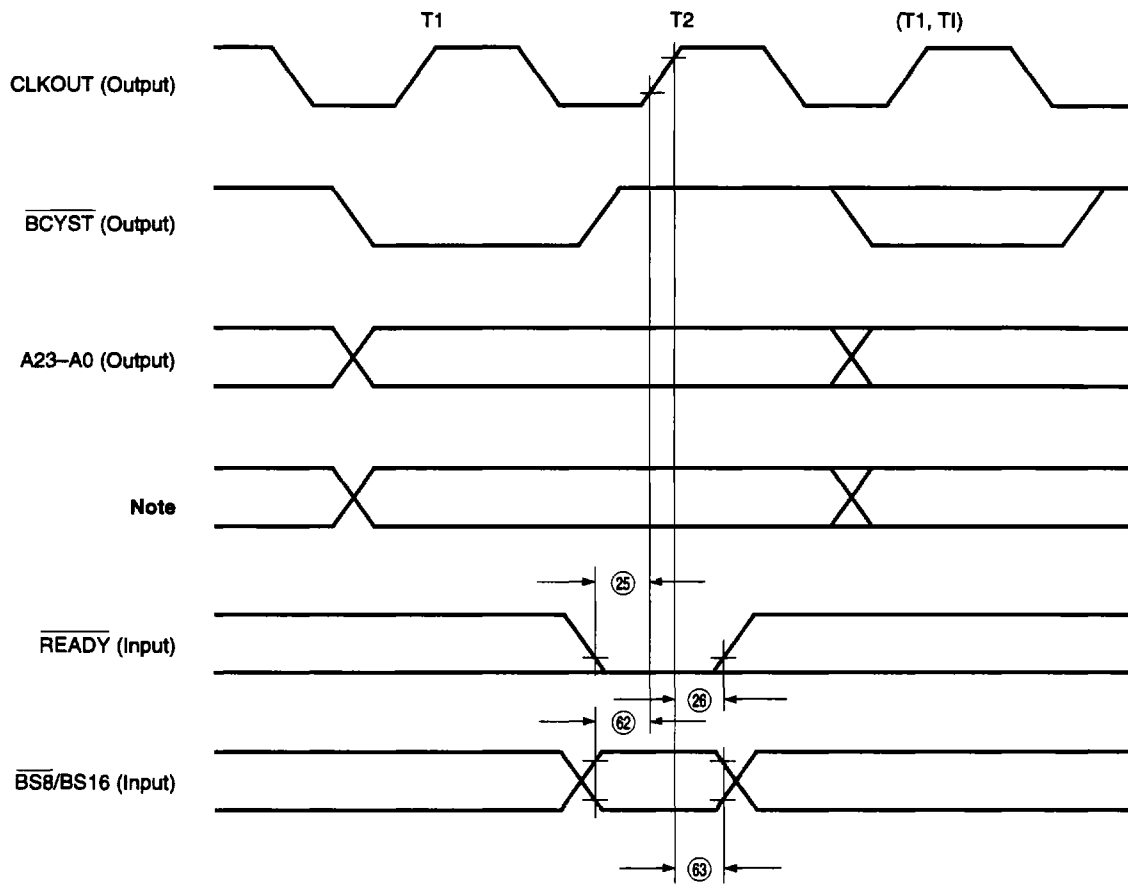
Note   R/W̄, M/ĪŌ, BUSST2, BUSST1, BUSST0, ŪBĒ, AEX (all output)

Fig. 15-14 Bus Hold
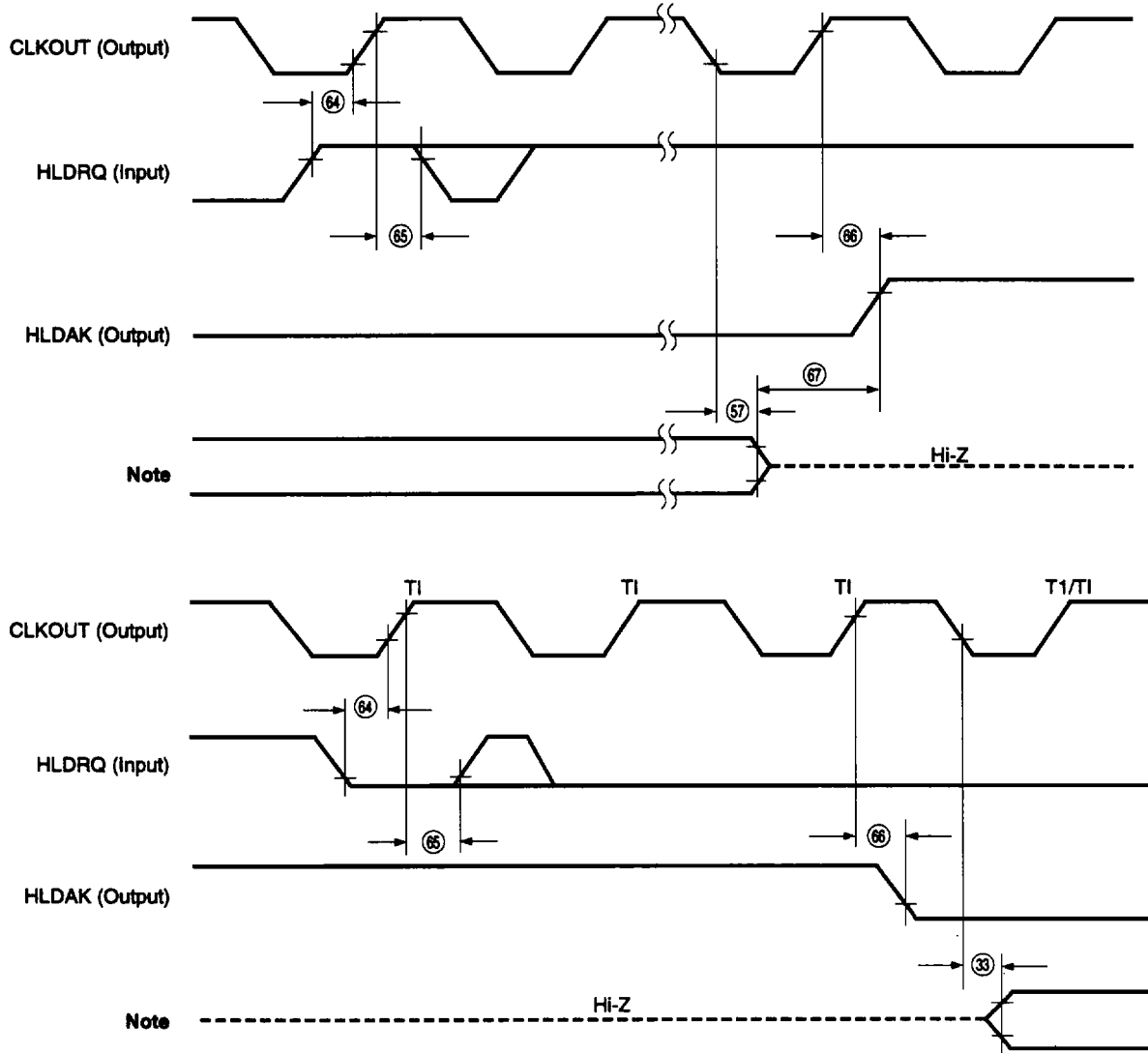
Note   R/W̄, M/ĪŌ, BUSST2, BUSST1, BUSST0, ŪBĒ (all output)

Fig. 15-15 Interrupt Acknowledge (Single Mode)
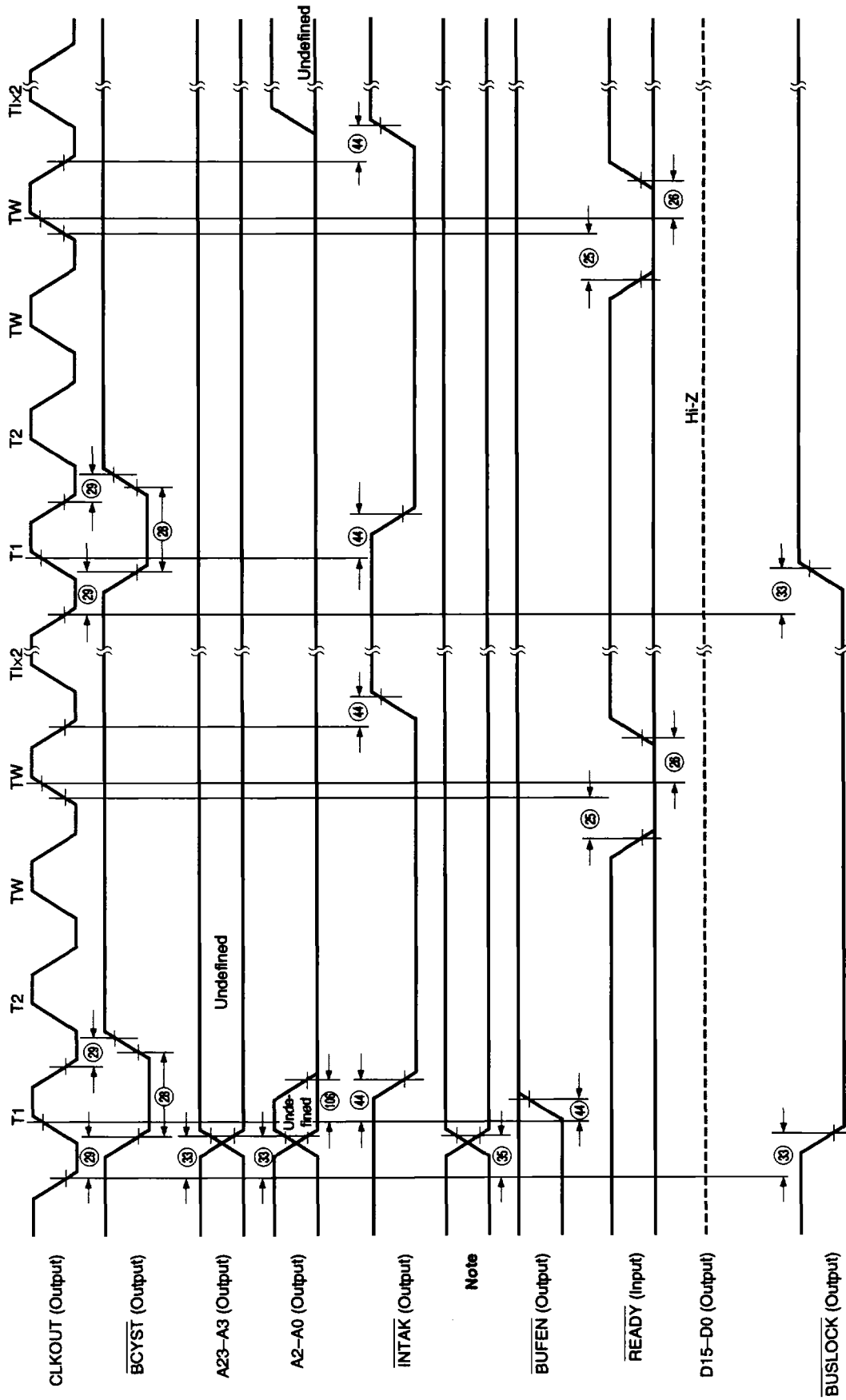
Note   R/W̄, M/ĪŌ, BUSST2, BUSST1, BUSST0, ŪBĒ, AEX (all output)

Remark   D̄S̄T̄B̄ is inactive.

Fig. 15-16 Interrupt Acknowledge (Cascade Mode)
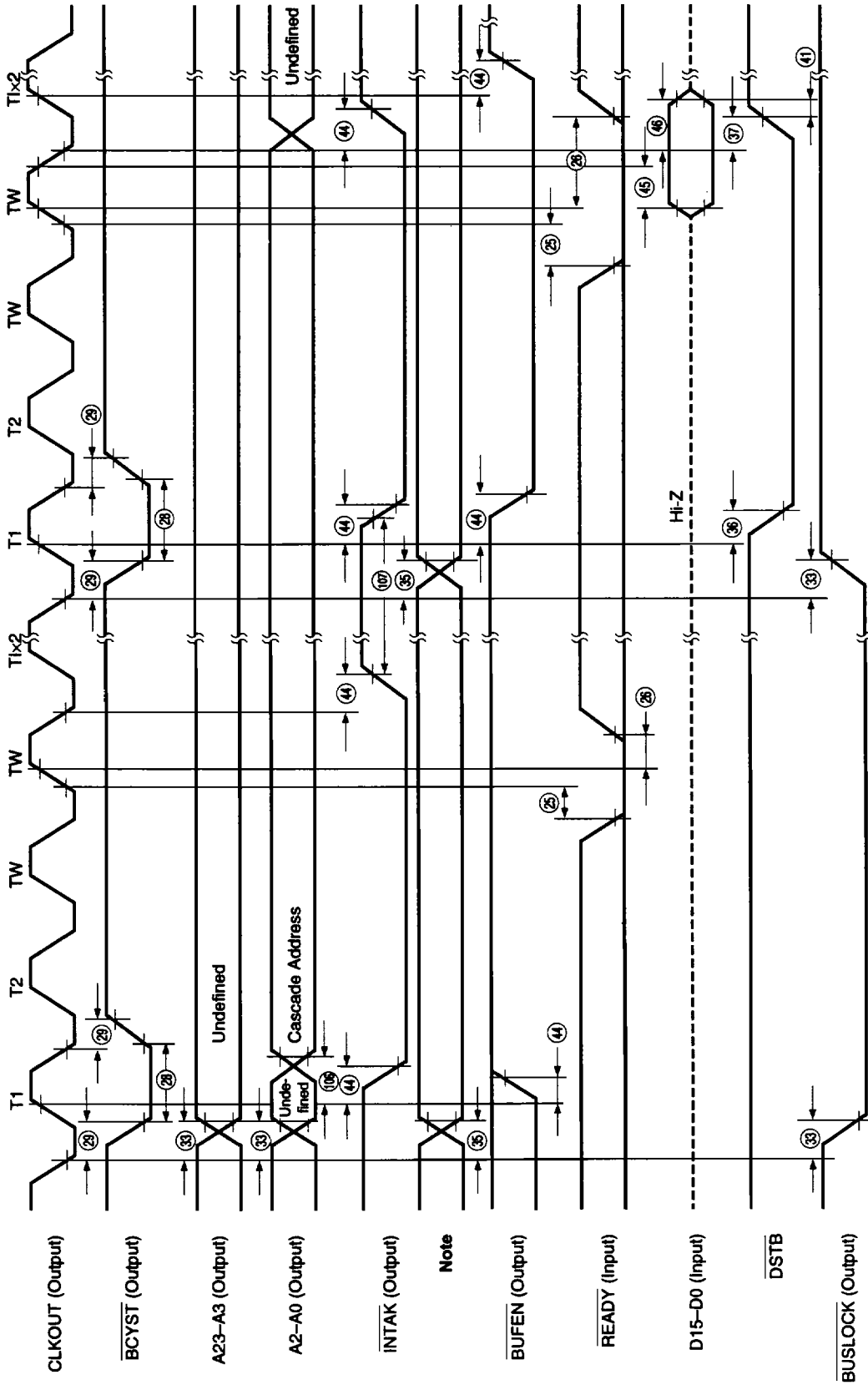
Note R/W̄, M/ĪO, BUSST2, BUSST1, BUSST0, ŪBĒ, AEX (all output)

Fig. 15-17 ICU Timing

INTPn (Input)
(n = 0~7)

⑥⑧

Fig. 15-18 TCU Timing (1)

CLKOUT (Output)

TCTLn (Input)
(n = 0~2)

TOUTn (Output)
(n = 0~2)

⑥⑨ ⑦⑩ ⑦⑪ ⑦② ⑦③ ⑦④ ⑦⓪ ⑥⑨

Fig. 15-19 TCU Timing (2)

TCLK (Input)

TCTLn (Input)
(n = 0–2)

TOUTn (Output)
(n = 0–2)

Fig. 15-20 SCU Timing

RxD (Input)

TOUT1 (Output)

TxD (Output)

16 or 64 TOUT1 pulses

16 or 64 TOUT1 pulses
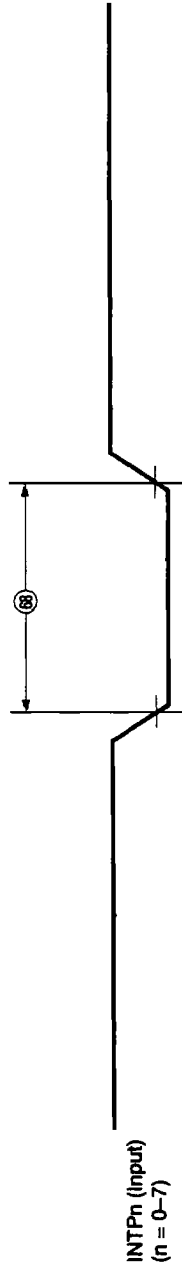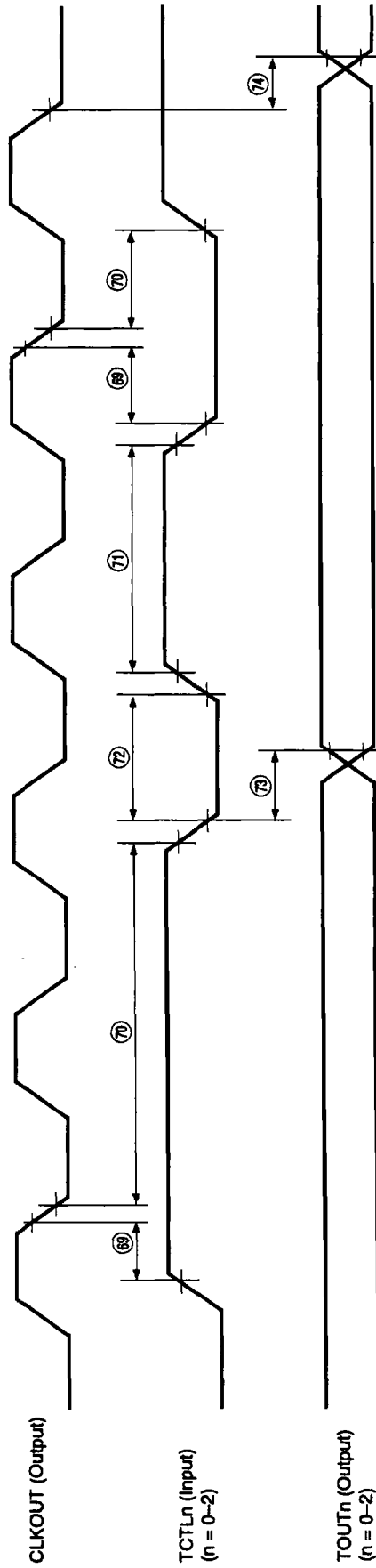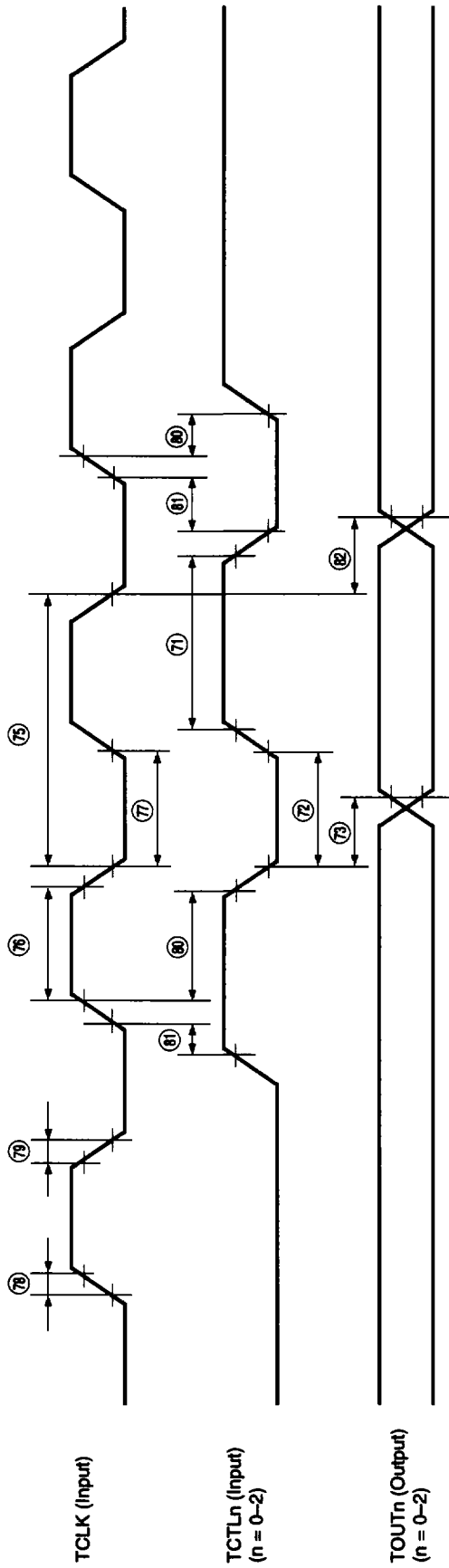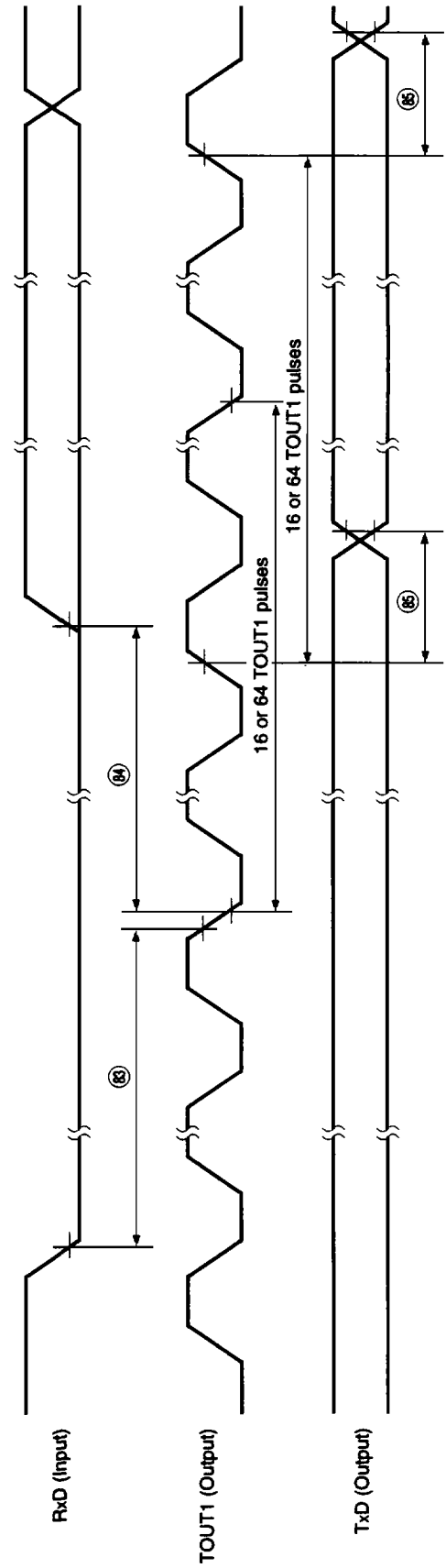
Fig. 15-21 DMAU Timing (1)
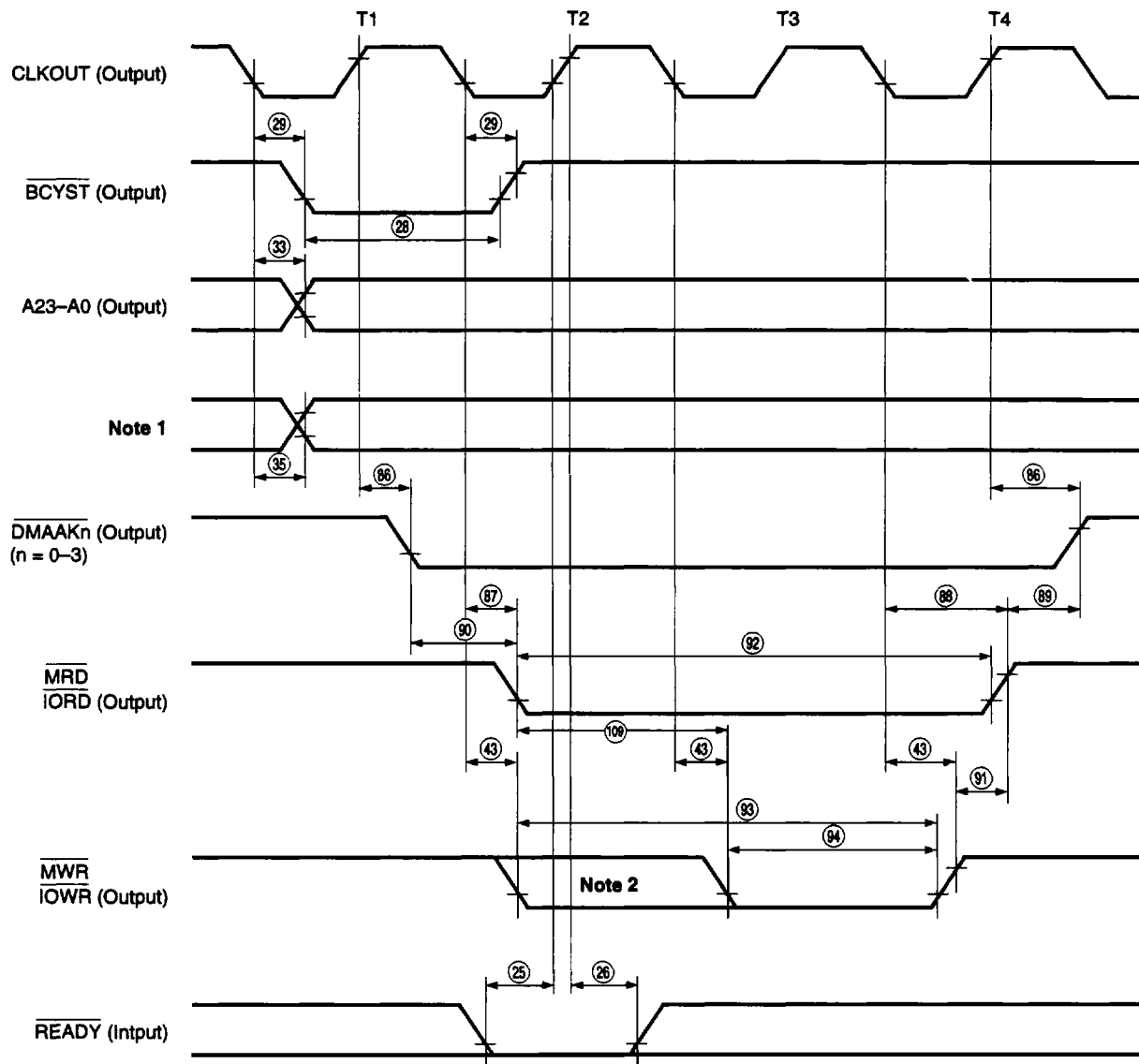
Notes 1. R/W̄, M/ĪŌ, BUSST2 to BUSST0, ŪBĒ (all output)
    2. In extended write mode, a low-level signal is output.
Remark D̄S̄T̄B̄ and B̄ŪF̄ĒN̄ are inactive.

Fig. 15-22 DMAU Timing (2)

CLKOUT (Output)

TC̄ (Output)Note

ĒND (Input)
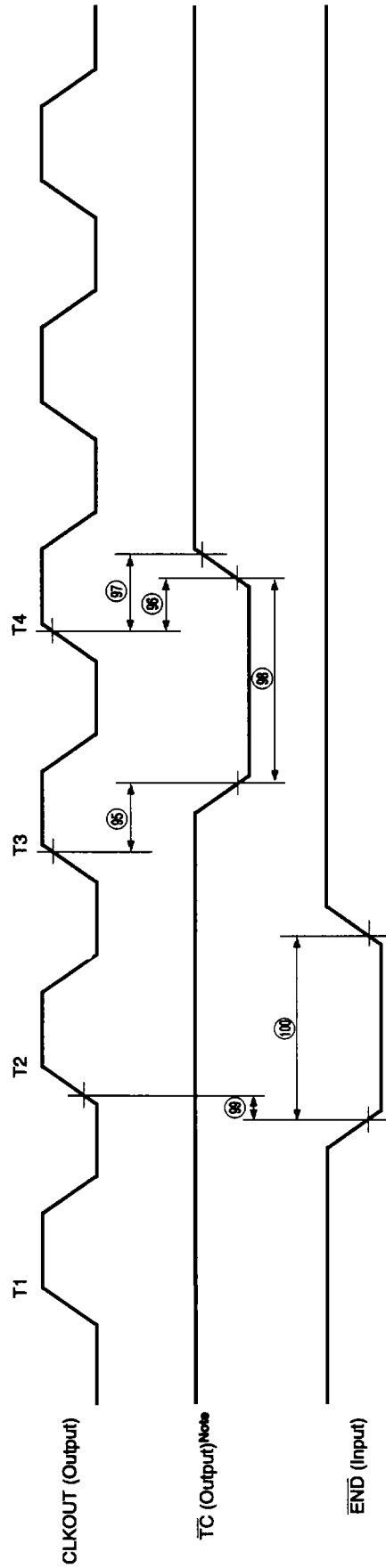
Note Presupposes that the TC̄ pin is pulled up by resistor RTC.

CLKOUT (Output)
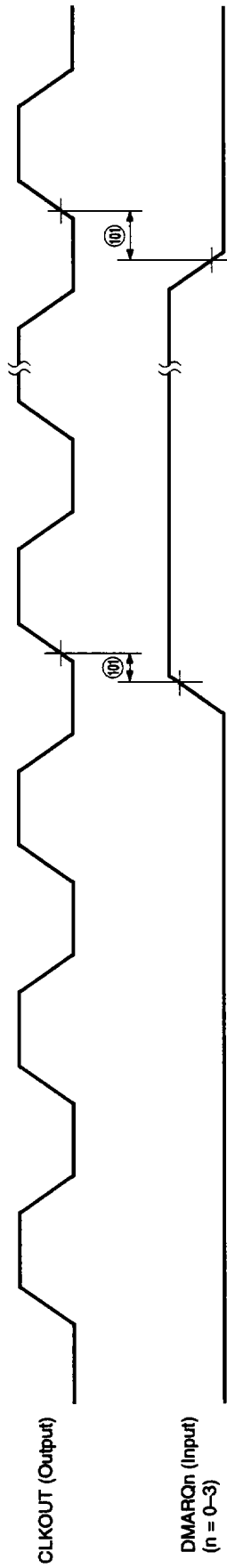
DMARQn (Input)
(n = 0–3)

Remark DMARQn (n = 0 to 3) can be input asynchronously with respect to CLKOUT.

Fig. 15-23 DMAU Timing (3) (Cascade Mode)

(a) Normal Operation
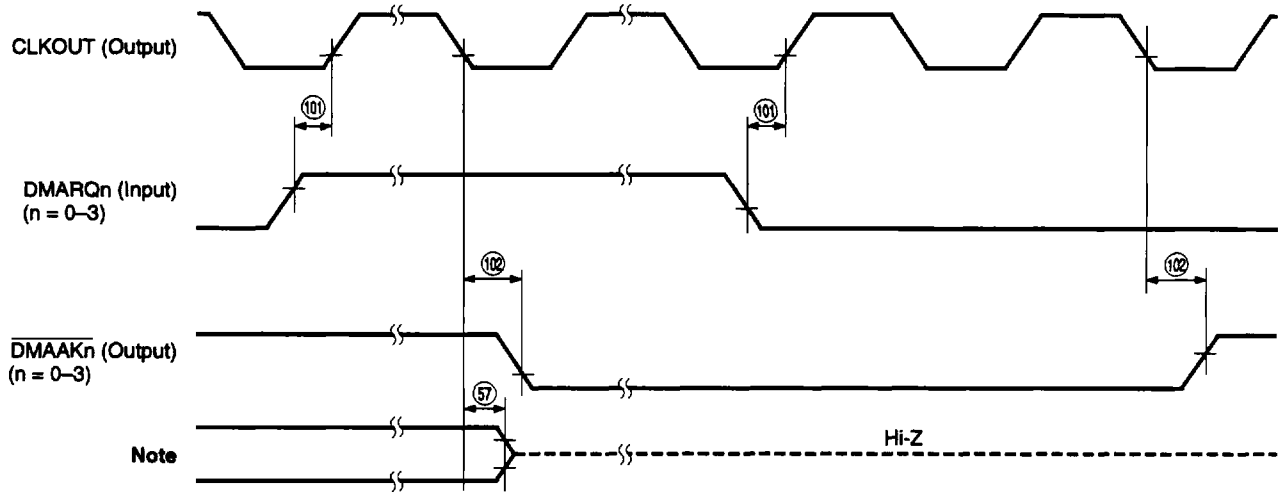
Note   A23 to A0, $\overline{\text{UBE}}$, $\overline{\text{MRD}}$, $\overline{\text{MWR}}$, $\overline{\text{IORD}}$, $\overline{\text{IOWR}}$, $\overline{\text{BUFEN}}$, $\overline{\text{BCYST}}$, $\overline{\text{DSTB}}$
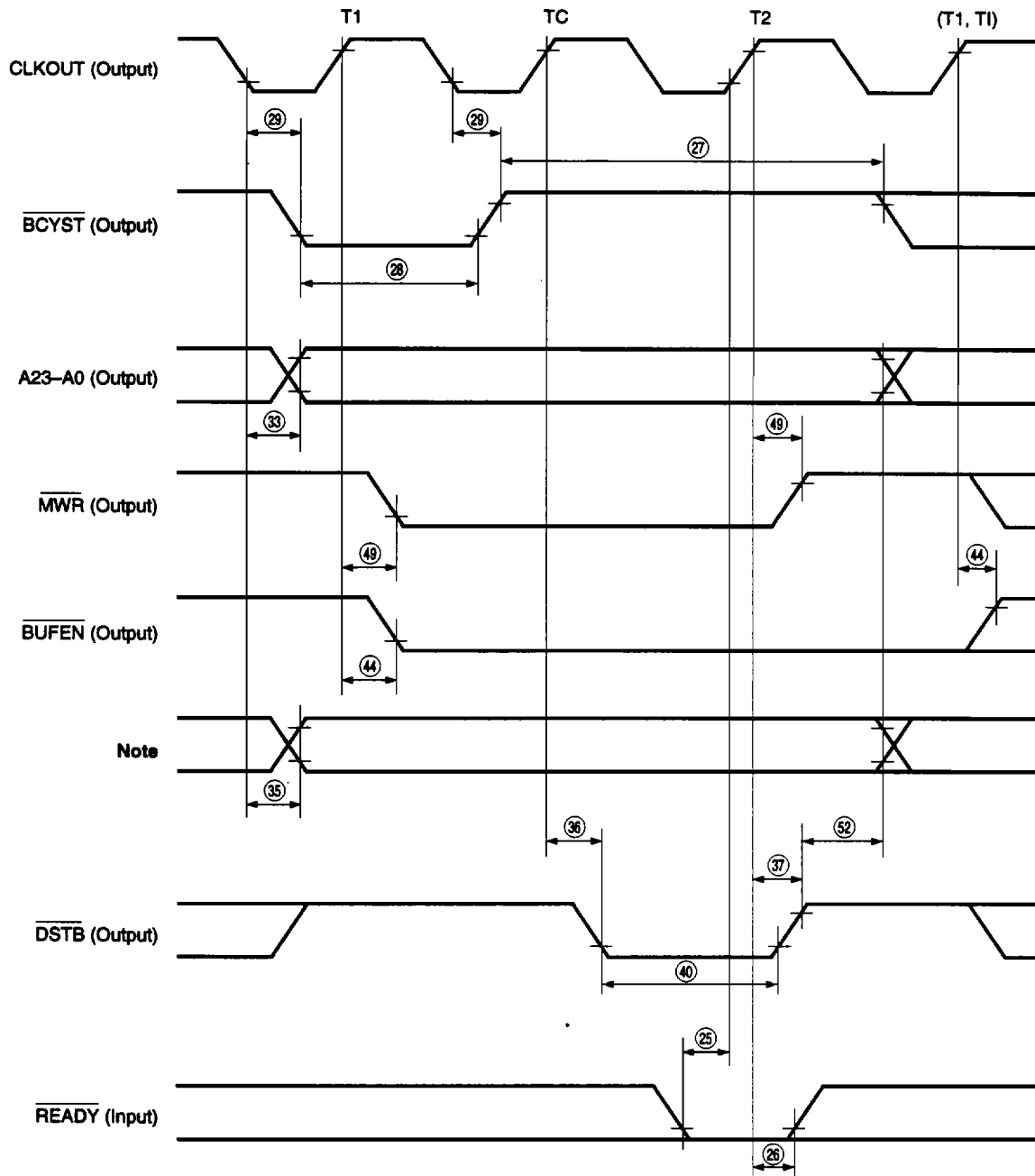
(b) With Refresh Cycle Inserted
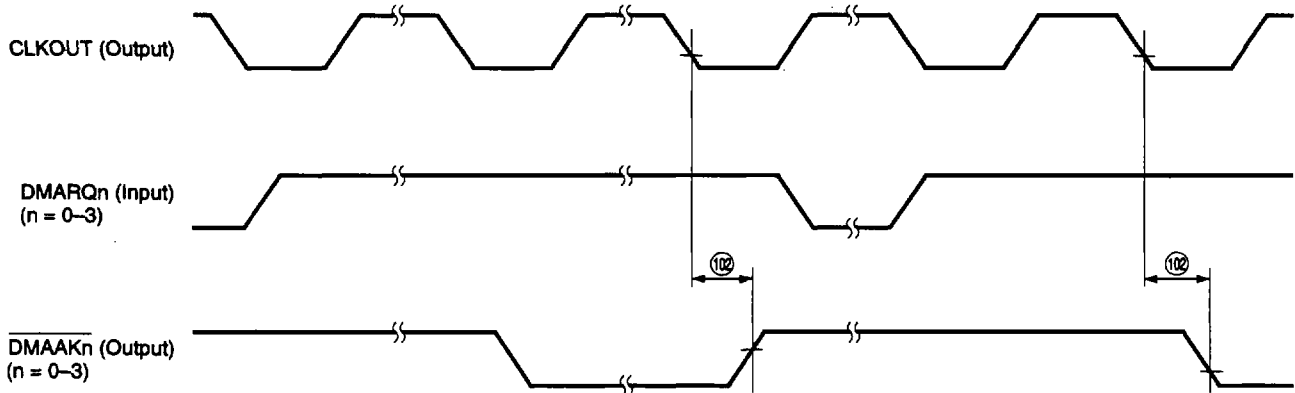
Fig. 15-24 Refresh Timing
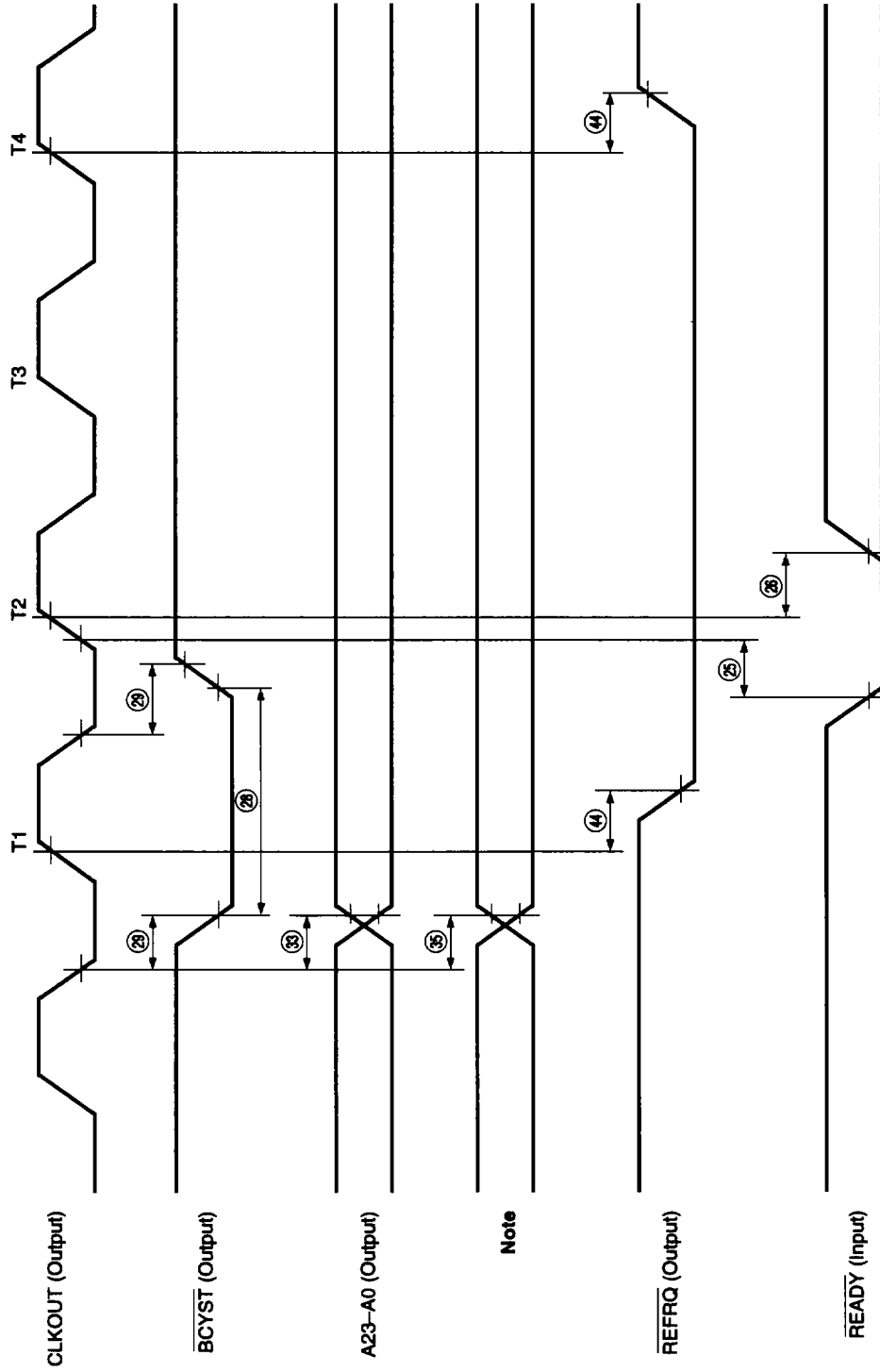
CLKOUT (Output)

BCYST (Output)

A23–A0 (Output)

Note

REFRQ (Output)

READY (Input)

Note R/W̄, M/IŌ, BUSST2, BUSST1, BUSST0, ŪBĒ, AEX (all output)

Remark D̄STB and BŪFĒN are inactive.

Fig. 15-25 Coprocessor Memory Read Cycle (No Walt)
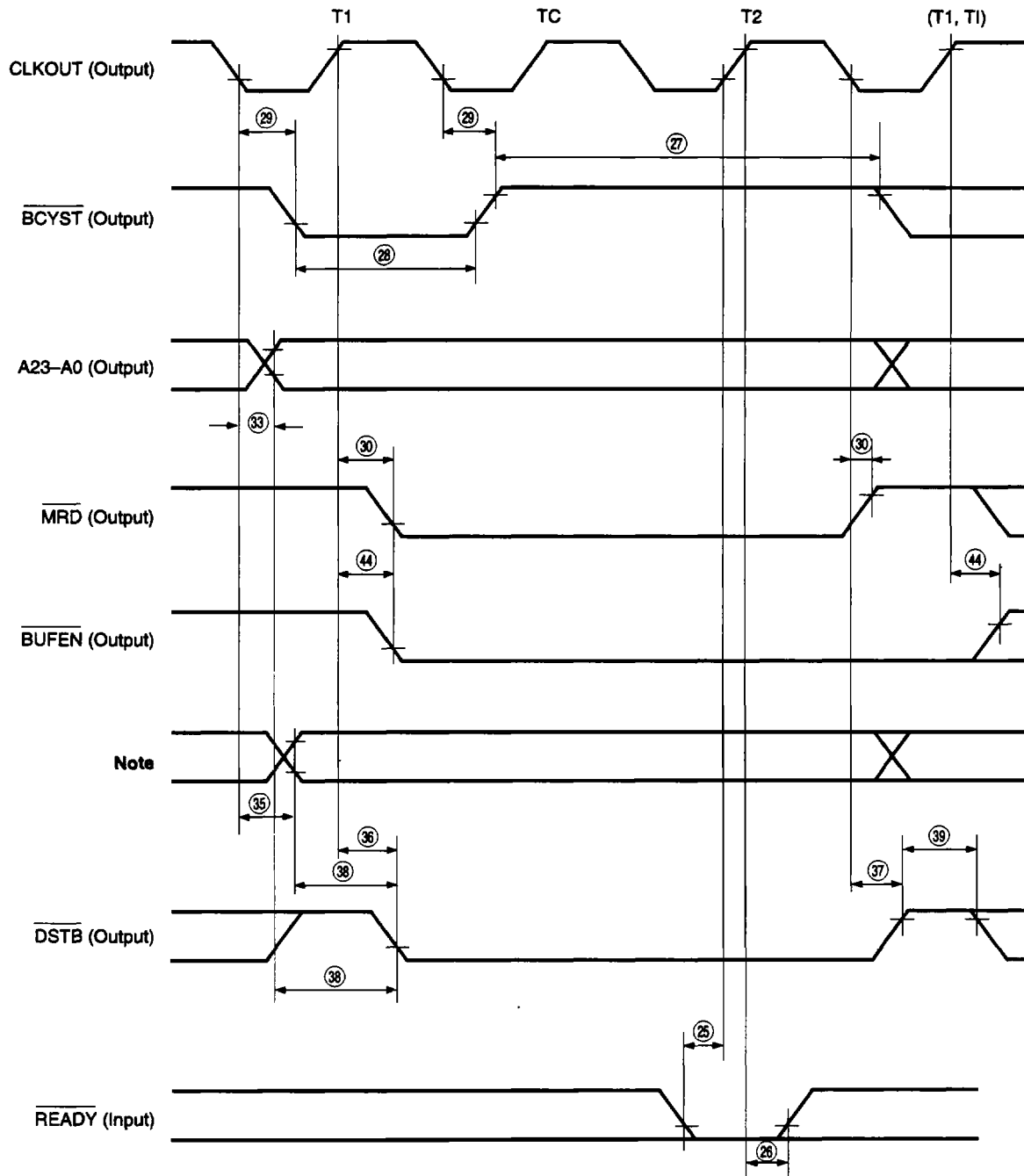
Note   R/W̄, M/ĪŌ, BUSST2, BUSST1, BUSST0, ŪBĒ, AEX (all output)

Fig. 15-26 Coprocessor Memory Write Cycle (No Wait)

Note   R/W̄, M/IŌ, BUSST2, BUSST1, BUSST0, ŪBE, AEX (all output)