

MOS INTEGRATED CIRCUIT

μ PD44645084, 44645094, 44645184, 44645364

72M-BIT QDR™ II SRAM

4-WORD BURST OPERATION

Description

The μ PD44645084 is a 8,388,608-word by 8-bit, the μ PD44645094 is a 8,388,608-word by 9-bit, the μ PD44645184 is a 4,194,304-word by 18-bit and the μ PD44645364 is a 2,097,152-word by 36-bit synchronous quad data rate static RAM fabricated with advanced CMOS technology using full CMOS six-transistor memory cell.

The μ PD44645084, μ PD44645094, μ PD44645184 and μ PD44645364 integrate unique synchronous peripheral circuitry and a burst counter. All input registers controlled by an input clock pair (K and K#) are latched on the positive edge of K and K#.

These products are suitable for application which require synchronous operation, high speed, low voltage, high density and wide bit configuration.

These products are packaged in 165-pin PLASTIC BGA.

Features

- 1.8 ± 0.1 V power supply
- 165-pin PLASTIC BGA (15 x 17)
- HSTL interface
- PLL circuitry for wide output data valid window and future frequency scaling
- Separate independent read and write data ports with concurrent transactions
- 100% bus utilization DDR READ and WRITE operation
- Four-tick burst for reduced address frequency
- Two input clocks (K and K#) for precise DDR timing at clock rising edges only
- Two output clocks (C and C#) for precise flight time
and clock skew matching-clock and data delivered together to receiving device
- Internally self-timed write control
- Clock-stop capability. Normal operation is restored in 1,024 cycles after clock is resumed.
- User programmable impedance output
- Fast clock cycle time : 3.7 ns (270 MHz) , 4.0 ns (250 MHz) , 5.0 ns (200 MHz)
- Simple control logic for easy depth expansion
- JTAG boundary scan

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Not all products and/or types are available in every country. Please check with an NEC Electronics sales representative for availability and additional information.

Ordering Information

Part number	Cycle Time ns	Clock Frequency MHz	Organization (word x bit)	Core Supply Voltage V	I/O Interface	Package		
μ PD44645084F5-E37-FQ1	3.7	270	8M x 8-bit	1.8 \pm 0.1	HSTL	165-pin PLASTIC BGA (15 x 17)		
μ PD44645084F5-E40-FQ1	4.0	250						
μ PD44645084F5-E50-FQ1	5.0	200						
μ PD44645094F5-E37-FQ1	3.7	270	8M x 9-bit					
μ PD44645094F5-E40-FQ1	4.0	250						
μ PD44645094F5-E50-FQ1	5.0	200						
μ PD44645184F5-E37-FQ1	3.7	270	4M x 18-bit					
μ PD44645184F5-E40-FQ1	4.0	250						
μ PD44645184F5-E50-FQ1	5.0	200						
μ PD44645364F5-E37-FQ1	3.7	270	2M x 36-bit					
μ PD44645364F5-E40-FQ1	4.0	250						
μ PD44645364F5-E50-FQ1	5.0	200						
μ PD44645084F5-E37-FQ1-A	3.7	270	8M x 8-bit	1.8 \pm 0.1	HSTL	165-pin PLASTIC BGA (15 x 17) Lead-free		
μ PD44645084F5-E40-FQ1-A	4.0	250						
μ PD44645084F5-E50-FQ1-A	5.0	200						
μ PD44645094F5-E37-FQ1-A	3.7	270	8M x 9-bit					
μ PD44645094F5-E40-FQ1-A	4.0	250						
μ PD44645094F5-E50-FQ1-A	5.0	200						
μ PD44645184F5-E37-FQ1-A	3.7	270	4M x 18-bit					
μ PD44645184F5-E40-FQ1-A	4.0	250						
μ PD44645184F5-E50-FQ1-A	5.0	200						
μ PD44645364F5-E37-FQ1-A	3.7	270	2M x 36-bit					
μ PD44645364F5-E40-FQ1-A	4.0	250						
μ PD44645364F5-E50-FQ1-A	5.0	200						

Remark Products with -A at the end of the part number are lead-free products.

Pin Configurations

165-pin PLASTIC BGA (15 x 17)

(Top View)

[μPD44645084]

8M x 8-bit

	1	2	3	4	5	6	7	8	9	10	11
A	CQ#	A	A	W#	NW1#	K#	NC	R#	A	A	CQ
B	NC	NC	NC	A	NC	K	NW0#	A	NC	NC	Q3
C	NC	NC	NC	V _{SS}	A	NC	A	V _{SS}	NC	NC	D3
D	NC	D4	NC	V _{SS}	V _{SS}	V _{SS}	V _{SS}	V _{SS}	NC	NC	NC
E	NC	NC	Q4	V _{DDQ}	V _{SS}	V _{SS}	V _{SS}	V _{DDQ}	NC	D2	Q2
F	NC	NC	NC	V _{DDQ}	V _{DD}	V _{SS}	V _{DD}	V _{DDQ}	NC	NC	NC
G	NC	D5	Q5	V _{DDQ}	V _{DD}	V _{SS}	V _{DD}	V _{DDQ}	NC	NC	NC
H	DLL#	V _{REF}	V _{DDQ}	V _{DDQ}	V _{DD}	V _{SS}	V _{DD}	V _{DDQ}	V _{DDQ}	V _{REF}	ZQ
J	NC	NC	NC	V _{DDQ}	V _{DD}	V _{SS}	V _{DD}	V _{DDQ}	NC	Q1	D1
K	NC	NC	NC	V _{DDQ}	V _{DD}	V _{SS}	V _{DD}	V _{DDQ}	NC	NC	NC
L	NC	Q6	D6	V _{DDQ}	V _{SS}	V _{SS}	V _{SS}	V _{DDQ}	NC	NC	Q0
M	NC	NC	NC	V _{SS}	V _{SS}	V _{SS}	V _{SS}	V _{SS}	NC	NC	D0
N	NC	D7	NC	V _{SS}	A	A	A	V _{SS}	NC	NC	NC
P	NC	NC	Q7	A	A	C	A	A	NC	NC	NC
R	TDO	TCK	A	A	A	C#	A	A	A	TMS	TDI

A : Address inputs

D0 to D7 : Data inputs

Q0 to Q7 : Data outputs

R# : Read input

W# : Write input

NW0#, NW1# : Nibble Write data select

K, K# : Input clock

C, C# : Output clock

CQ, CQ# : Echo clock

ZQ : Output impedance matching

DLL# : DLL/PLL disable

TMS : IEEE 1149.1 Test input

TDI : IEEE 1149.1 Test input

TCK : IEEE 1149.1 Clock input

TDO : IEEE 1149.1 Test output

V_{REF} : HSTL input reference input

V_{DD} : Power Supply

V_{DDQ} : Power Supply

V_{SS} : Ground

NC : No connection

Remarks 1. xxx# indicates active LOW signal.

2. Refer to **Package Drawing** for the index mark.

3. 7A is expansion address for 144Mb.

165-pin PLASTIC BGA (15 x 17)

(Top View)

[μPD44645094]

8M x 9-bit

	1	2	3	4	5	6	7	8	9	10	11
A	CQ#	A	A	W#	NC	K#	NC	R#	A	A	CQ
B	NC	NC	NC	A	NC	K	BW0#	A	NC	NC	Q4
C	NC	NC	NC	V _{SS}	A	NC	A	V _{SS}	NC	NC	D4
D	NC	D5	NC	V _{SS}	V _{SS}	V _{SS}	V _{SS}	V _{SS}	NC	NC	NC
E	NC	NC	Q5	V _{DDQ}	V _{SS}	V _{SS}	V _{SS}	V _{DDQ}	NC	D3	Q3
F	NC	NC	NC	V _{DDQ}	V _{DD}	V _{SS}	V _{DD}	V _{DDQ}	NC	NC	NC
G	NC	D6	Q6	V _{DDQ}	V _{DD}	V _{SS}	V _{DD}	V _{DDQ}	NC	NC	NC
H	DLL#	V _{REF}	V _{DDQ}	V _{DDQ}	V _{DD}	V _{SS}	V _{DD}	V _{DDQ}	V _{DDQ}	V _{REF}	ZQ
J	NC	NC	NC	V _{DDQ}	V _{DD}	V _{SS}	V _{DD}	V _{DDQ}	NC	Q2	D2
K	NC	NC	NC	V _{DDQ}	V _{DD}	V _{SS}	V _{DD}	V _{DDQ}	NC	NC	NC
L	NC	Q7	D7	V _{DDQ}	V _{SS}	V _{SS}	V _{SS}	V _{DDQ}	NC	NC	Q1
M	NC	NC	NC	V _{SS}	V _{SS}	V _{SS}	V _{SS}	V _{SS}	NC	NC	D1
N	NC	D8	NC	V _{SS}	A	A	A	V _{SS}	NC	NC	NC
P	NC	NC	Q8	A	A	C	A	A	NC	D0	Q0
R	TDO	TCK	A	A	A	C#	A	A	A	TMS	TDI

A : Address inputs

D0 to D8 : Data inputs

Q0 to Q8 : Data outputs

R# : Read input

W# : Write input

BW0# : Byte Write data select

K, K# : Input clock

C, C# : Output clock

CQ, CQ# : Echo clock

ZQ : Output impedance matching

DLL# : DLL/PLL disable

TMS : IEEE 1149.1 Test input

TDI : IEEE 1149.1 Test input

TCK : IEEE 1149.1 Clock input

TDO : IEEE 1149.1 Test output

V_{REF} : HSTL input reference inputV_{DD} : Power SupplyV_{DDQ} : Power SupplyV_{SS} : Ground

NC : No connection

Remarks 1. xxx# indicates active LOW signal.2. Refer to **Package Drawing** for the index mark.

3. 7A is expansion address for 144Mb.

165-pin PLASTIC BGA (15 x 17)

(Top View)

[μPD44645184]

4M x 18-bit

	1	2	3	4	5	6	7	8	9	10	11
A	CQ#	V _{SS}	A	W#	BW1#	K#	NC	R#	A	A	CQ
B	NC	Q9	D9	A	NC	K	BW0#	A	NC	NC	Q8
C	NC	NC	D10	V _{SS}	A	NC	A	V _{SS}	NC	Q7	D8
D	NC	D11	Q10	V _{SS}	V _{SS}	V _{SS}	V _{SS}	V _{SS}	NC	NC	D7
E	NC	NC	Q11	V _{DDQ}	V _{SS}	V _{SS}	V _{SS}	V _{DDQ}	NC	D6	Q6
F	NC	Q12	D12	V _{DDQ}	V _{DD}	V _{SS}	V _{DD}	V _{DDQ}	NC	NC	Q5
G	NC	D13	Q13	V _{DDQ}	V _{DD}	V _{SS}	V _{DD}	V _{DDQ}	NC	NC	D5
H	DLL#	V _{REF}	V _{DDQ}	V _{DDQ}	V _{DD}	V _{SS}	V _{DD}	V _{DDQ}	V _{DDQ}	V _{REF}	ZQ
J	NC	NC	D14	V _{DDQ}	V _{DD}	V _{SS}	V _{DD}	V _{DDQ}	NC	Q4	D4
K	NC	NC	Q14	V _{DDQ}	V _{DD}	V _{SS}	V _{DD}	V _{DDQ}	NC	D3	Q3
L	NC	Q15	D15	V _{DDQ}	V _{SS}	V _{SS}	V _{SS}	V _{DDQ}	NC	NC	Q2
M	NC	NC	D16	V _{SS}	V _{SS}	V _{SS}	V _{SS}	V _{SS}	NC	Q1	D2
N	NC	D17	Q16	V _{SS}	A	A	A	V _{SS}	NC	NC	D1
P	NC	NC	Q17	A	A	C	A	A	NC	D0	Q0
R	TDO	TCK	A	A	A	C#	A	A	A	TMS	TDI

A : Address inputs

D0 to D17 : Data inputs

Q0 to Q17 : Data outputs

R# : Read input

W# : Write input

BW0#, BW1# : Byte Write data select

K, K# : Input clock

C, C# : Output clock

CQ, CQ# : Echo clock

ZQ : Output impedance matching

DLL# : DLL/PLL disable

TMS : IEEE 1149.1 Test input

TDI : IEEE 1149.1 Test input

TCK : IEEE 1149.1 Clock input

TDO : IEEE 1149.1 Test output

V_{REF} : HSTL input reference inputV_{DD} : Power SupplyV_{DDQ} : Power SupplyV_{SS} : Ground

NC : No connection

Remarks 1. xxx# indicates active LOW signal.2. Refer to **Package Drawing** for the index mark.

3. 2A is expansion address for 144Mb.

2A of this product can also be used as NC.

165-pin PLASTIC BGA (15 x 17)

(Top View)

[μPD44645364]

2M x 36-bit

	1	2	3	4	5	6	7	8	9	10	11
A	CQ#	V _{SS}	A	W#	BW2#	K#	BW1#	R#	A	V _{SS}	CQ
B	Q27	Q18	D18	A	BW3#	K	BW0#	A	D17	Q17	Q8
C	D27	Q28	D19	V _{SS}	A	NC	A	V _{SS}	D16	Q7	D8
D	D28	D20	Q19	V _{SS}	V _{SS}	V _{SS}	V _{SS}	V _{SS}	Q16	D15	D7
E	Q29	D29	Q20	V _{DDQ}	V _{SS}	V _{SS}	V _{SS}	V _{DDQ}	Q15	D6	Q6
F	Q30	Q21	D21	V _{DDQ}	V _{DD}	V _{SS}	V _{DD}	V _{DDQ}	D14	Q14	Q5
G	D30	D22	Q22	V _{DDQ}	V _{DD}	V _{SS}	V _{DD}	V _{DDQ}	Q13	D13	D5
H	DLL#	V _{REF}	V _{DDQ}	V _{DDQ}	V _{DD}	V _{SS}	V _{DD}	V _{DDQ}	V _{DDQ}	V _{REF}	ZQ
J	D31	Q31	D23	V _{DDQ}	V _{DD}	V _{SS}	V _{DD}	V _{DDQ}	D12	Q4	D4
K	Q32	D32	Q23	V _{DDQ}	V _{DD}	V _{SS}	V _{DD}	V _{DDQ}	Q12	D3	Q3
L	Q33	Q24	D24	V _{DDQ}	V _{SS}	V _{SS}	V _{SS}	V _{DDQ}	D11	Q11	Q2
M	D33	Q34	D25	V _{SS}	V _{SS}	V _{SS}	V _{SS}	V _{SS}	D10	Q1	D2
N	D34	D26	Q25	V _{SS}	A	A	A	V _{SS}	Q10	D9	D1
P	Q35	D35	Q26	A	A	C	A	A	Q9	D0	Q0
R	TDO	TCK	A	A	A	C#	A	A	A	TMS	TDI

A : Address inputs

D0 to D35 : Data inputs

Q0 to Q35 : Data outputs

R# : Read input

W# : Write input

BW0# to BW3# : Byte Write data select

K, K# : Input clock

C, C# : Output clock

CQ, CQ# : Echo clock

ZQ : Output impedance matching

DLL# : DLL/PLL disable

TMS : IEEE 1149.1 Test input

TDI : IEEE 1149.1 Test input

TCK : IEEE 1149.1 Clock input

TDO : IEEE 1149.1 Test output

V_{REF} : HSTL input reference inputV_{DD} : Power SupplyV_{DDQ} : Power SupplyV_{SS} : Ground

NC : No connection

Remarks 1. xxx# indicates active LOW signal.2. Refer to **Package Drawing** for the index mark.

3. 10A is expansion address for 144Mb.

2A and 10A of this product can also be used as NC.

Pin Identification

(1/2)

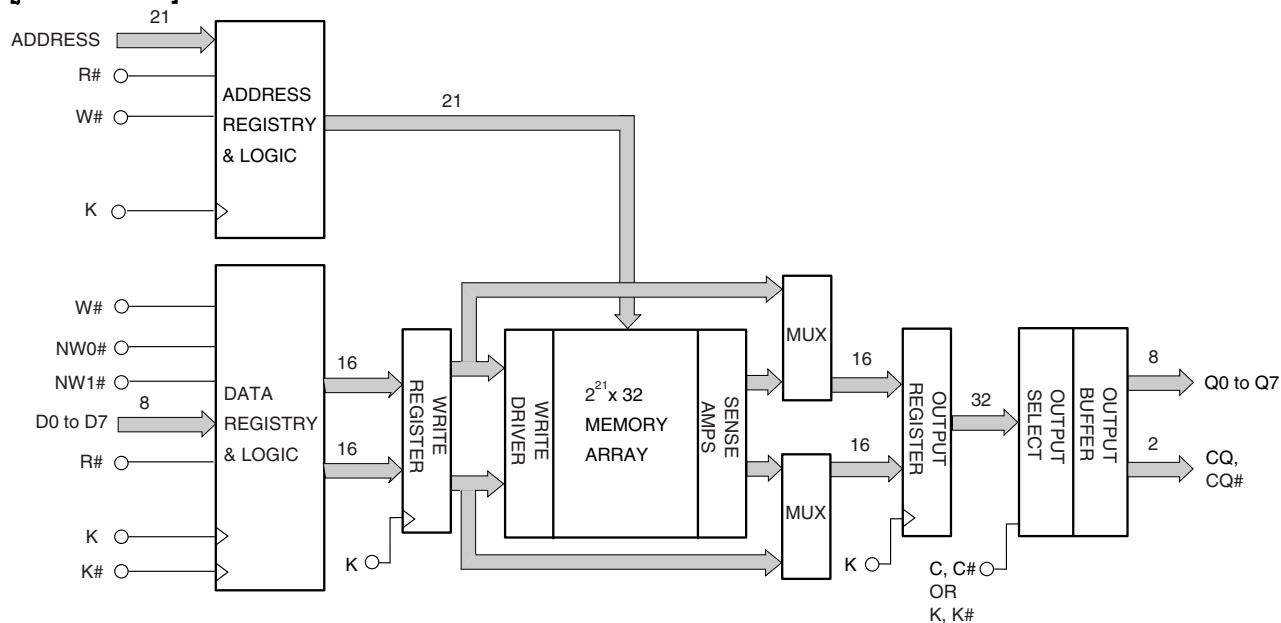
Symbol	Description
A	Synchronous Address Inputs: These inputs are registered and must meet the setup and hold times around the rising edge of K. All transactions operate on a burst of four words (two clock periods of bus activity). These inputs are ignored when device is deselected, i.e., NOP (R# = W# = HIGH).
D0 to Dxx	Synchronous Data Inputs: Input data must meet setup and hold times around the rising edges of K and K# during WRITE operations. See Pin Configurations for ball site location of individual signals. x8 device uses D0 to D7. x9 device uses D0 to D8. x18 device uses D0 to D17. x36 device uses D0 to D35.
Q0 to Qxx	Synchronous Data Outputs: Output data is synchronized to the respective C and C# or to K and K# rising edges if C and C# are tied HIGH. Data is output in synchronization with C and C# (or K and K#), depending on the R# command. See Pin Configurations for ball site location of individual signals. x8 device uses Q0 to Q7. x9 device uses Q0 to Q8. x18 device uses Q0 to Q17. x36 device uses Q0 to Q35.
R#	Synchronous Read: When LOW this input causes the address inputs to be registered and a READ cycle to be initiated. This input must meet setup and hold times around the rising edge of K. If a READ command (R# = LOW) is input, an input of R# on the subsequent rising edge of K is ignored.
W#	Synchronous Write: When LOW this input causes the address inputs to be registered and a WRITE cycle to be initiated. This input must meet setup and hold times around the rising edge of K. If a WRITE command (W# = LOW) is input, an input of W# on the subsequent rising edge of K is ignored.
BWx# NWx#	Synchronous Byte Writes (Nibble Writes on x8): When LOW these inputs cause their respective byte or nibble to be registered and written during WRITE cycles. These signals must meet setup and hold times around the rising edges of K and K# for each of the two rising edges comprising the WRITE cycle. See Pin Configurations for signal to data relationships. x8 device uses NW0#, NW1#. x9 device uses BW0#. x18 device uses BW0#, BW1#. x36 device uses BW0# to BW3#. See Byte Write Operation for relation between BWx#, NWx# and Dxx.
K, K#	Input Clock: This input clock pair registers address and control inputs on the rising edge of K, and registers data on the rising edge of K and the rising edge of K#. K# is ideally 180 degrees out of phase with K. All synchronous inputs must meet setup and hold times around the clock rising edges.
C, C#	Output Clock: This clock pair provides a user controlled means of tuning device output data. The rising edge of C# is used as the output timing reference for first and third output data. The rising edge of C is used as the output reference for second and fourth output data. Ideally, C# is 180 degrees out of phase with C. When use of K and K# as the reference instead of C and C#, then fixed C and C# to HIGH. Operation cannot be guaranteed unless C and C# are fixed to HIGH (i.e. toggle of C and C#).

(2/2)

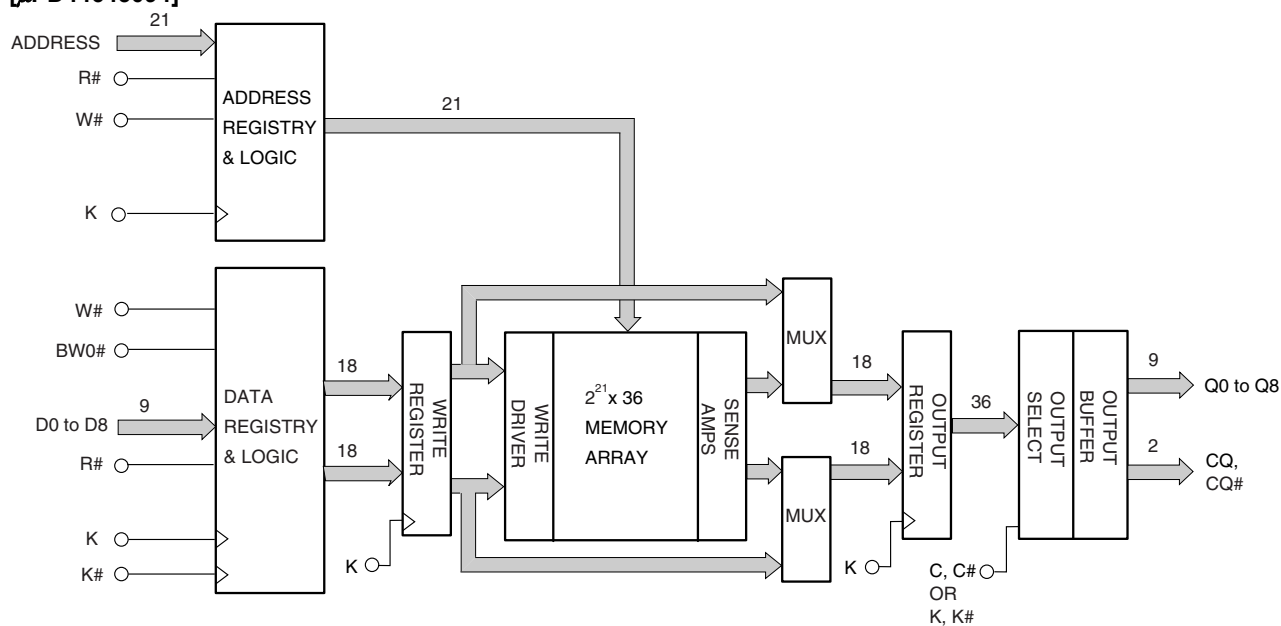
Symbol	Description
CQ, CQ#	Synchronous Echo Clock Outputs. The rising edges of these outputs are tightly matched to the synchronous data outputs and can be used as a data valid indication. These signals run freely and do not stop when Q tristates. If C and C# are stopped (if K and K# are stopped in the single clock mode), CQ and CQ# will also stop.
<R> ZQ	Output Impedance Matching Input: This input is used to tune the device outputs to the system data bus impedance. Q, CQ and CQ# output impedance are set to $0.2 \times RQ$, where RQ is a resistor from this bump to ground. The output impedance can be minimized by directly connect ZQ to V _{DDQ} . This pin cannot be connected directly to GND or left unconnected. The output impedance is adjusted every 1,024 cycles upon power-up to account for drifts in supply voltage and temperature. After replacement for a resistor, the new output impedance is reset by implementing power-on sequence.
<R> DLL#	DLL/PLL Disable: When debugging the system or board, the operation can be performed at a clock frequency slower than TKHKH (MAX.) without the DLL/PLL circuit being used, if DLL# = LOW. The AC/DC characteristics cannot be guaranteed. For normal operation, DLL# must be HIGH and it can be connected to V _{DDQ} through a 10 kΩ or less resistor.
TMS	IEEE 1149.1 Test Inputs: 1.8 V I/O level. These balls may be left Not Connected if the JTAG function is not used in the circuit.
TDI	
TCK	IEEE 1149.1 Clock Input: 1.8 V I/O level. This pin must be tied to V _{SS} if the JTAG function is not used in the circuit.
TDO	IEEE 1149.1 Test Output: 1.8 V I/O level.
VREF	HSTL Input Reference Voltage: Nominally V _{DDQ} /2. Provides a reference voltage for the input buffers.
VDD	Power Supply: 1.8 V nominal. See Recommended DC Operating Conditions and DC Characteristics for range.
VDDQ	Power Supply: Isolated Output Buffer Supply. Nominally 1.5 V. 1.8 V is also permissible. See Recommended DC Operating Conditions and DC Characteristics for range.
VSS	Power Supply: Ground
<R> NC	No Connect: These signals are not connected internally.

Block Diagram

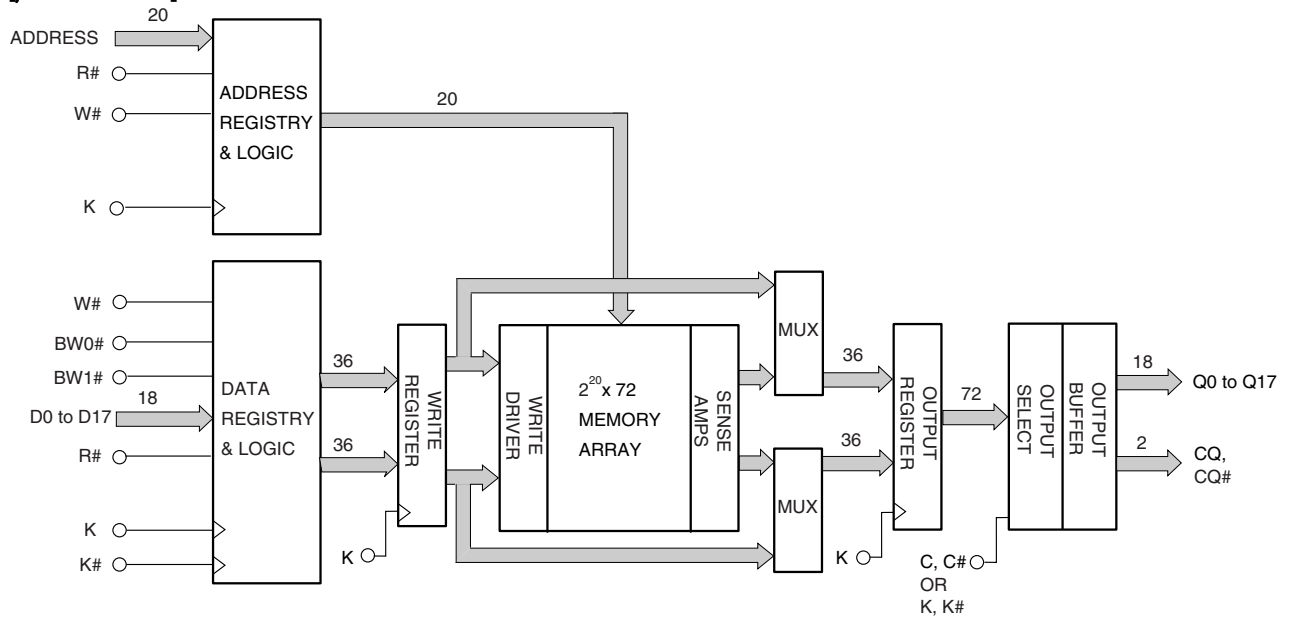
[μ PD44645084]



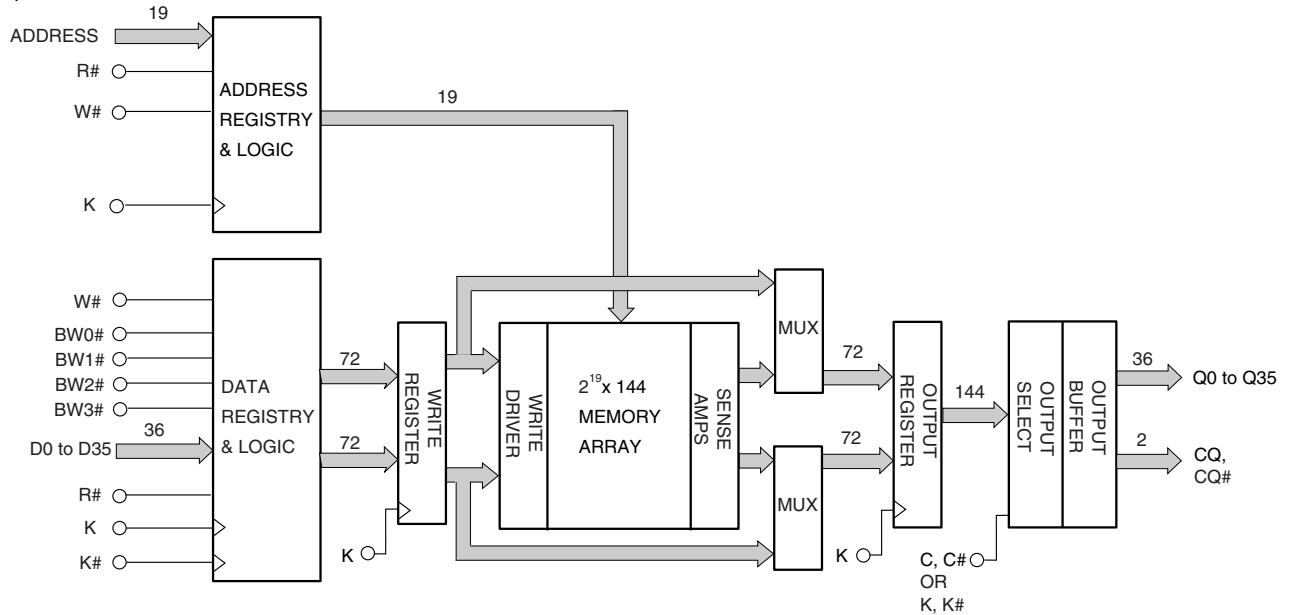
[μ PD44645094]



[μPD44645184]



[μPD44645364]



<R> **Power-On Sequence in QDR II SRAM**

QDR II SRAMs must be powered up and initialized in a predefined manner to prevent undefined operations. The following timing charts show the recommended power-on sequence.

The following power-up supply voltage application is recommended: V_{SS} , V_{DD} , V_{DDQ} , V_{REF} , then V_{IN} . V_{DD} and V_{DDQ} can be applied simultaneously, as long as V_{DDQ} does not exceed V_{DD} by more than 0.5V during power-up. The following power-down supply voltage removal sequence is recommended: V_{IN} , V_{REF} , V_{DDQ} , V_{DD} , V_{SS} . V_{DD} and V_{DDQ} can be removed simultaneously, as long as V_{DDQ} does not exceed V_{DD} by more than 0.5V during power-down.

Power-On Sequence

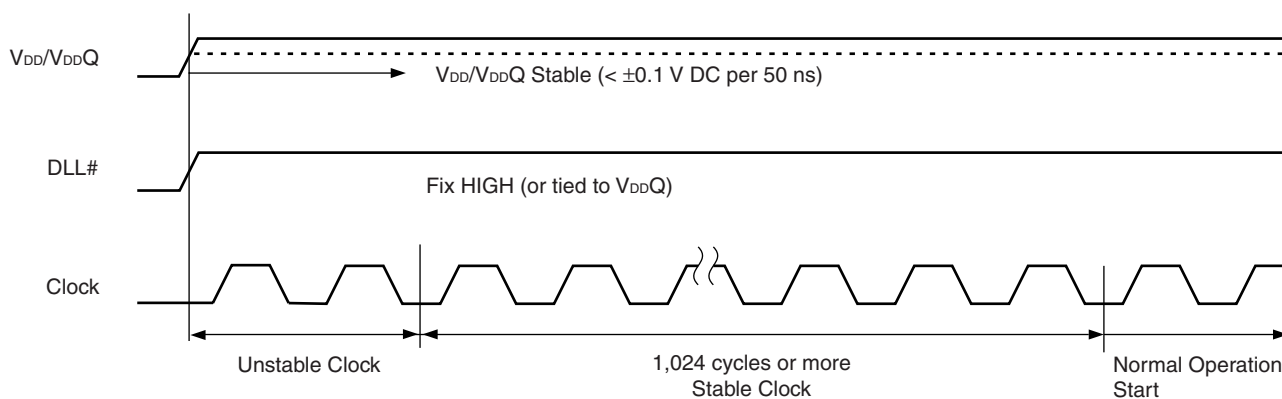
Apply power and tie DLL# to HIGH.

- Apply V_{DD} before V_{DDQ} .
- Apply V_{DDQ} before V_{REF} or at the same time as V_{REF} .

Provide stable clock for more than 1,024 cycles to lock the DLL/PLL.

DLL/PLL Constraints

The DLL/PLL uses K clock as its synchronizing input and the input should have low phase jitter which is specified as TKC var. The DLL/PLL can cover 120 MHz as the lowest frequency. If the input clock is unstable and the DLL/PLL is enabled, then the DLL/PLL may lock onto an undesired clock frequency.

Power-On Waveforms

Truth Table

Operation	CLK	R#	W#	D or Q				
WRITE cycle Load address, input write data on two consecutive K and K# rising edge	L → H	H	L	Data in				
				Input data	D _A (A+0)	D _A (A+1)	D _A (A+2)	D _A (A+3)
				Input clock	K(t+1) ↑	K#(t+1) ↑	K(t+2) ↑	K#(t+2) ↑
READ cycle Load address, read data on two consecutive C and C# rising edge	L → H	L	×	Data out				
				Output data	Q _A (A+0)	Q _A (A+1)	Q _A (A+2)	Q _A (A+3)
				Output clock	C#(t+1) ↑	C(t+2) ↑	C#(t+2) ↑	C(t+3) ↑
NOP (No operation)	L → H	H	H	D = ×, Q = High-Z				
Clock stop	Stopped	×	×	Previous state				

Remarks 1. H : HIGH, L : LOW, × : don't care, ↑ : rising edge.

2. Data inputs are registered at K and K# rising edges. Data outputs are delivered at C and C# rising edges except if C and C# are HIGH then data outputs are delivered at K and K# rising edges.
3. R# and W# must meet setup/hold times around the rising edge (LOW to HIGH) of K and are registered at the rising edge of K.
4. This device contains circuitry that ensure the outputs to be in high impedance during power-up.
5. Refer to state diagram and timing diagrams for clarification.
6. It is recommended that K = K# = C = C# when clock is stopped. This is not essential but permits most rapid restart by overcoming transmission line charging symmetrically.
7. If R# was LOW to initiate the previous cycle, this signal becomes a don't care for this WRITE operation however it is strongly recommended that this signal is brought HIGH as shown in the truth table.
8. W# during write cycle and R# during read cycle were HIGH on previous K clock rising edge. Initiating consecutive READ or WRITE operations on consecutive K clock rising edges is not permitted. The device will ignore the second request.

Byte Write Operation

[μ PD44645084]

Operation	K	K#	NW0#	NW1#
Write D0 to D7	L \rightarrow H	—	0	0
	—	L \rightarrow H	0	0
Write D0 to D3	L \rightarrow H	—	0	1
	—	L \rightarrow H	0	1
Write D4 to D7	L \rightarrow H	—	1	0
	—	L \rightarrow H	1	0
Write nothing	L \rightarrow H	—	1	1
	—	L \rightarrow H	1	1

Remarks 1. H : HIGH, L : LOW, \rightarrow : rising edge.

2. Assumes a WRITE cycle was initiated. NW0# and NW1# can be altered for any portion of the BURST WRITE operation provided that the setup and hold requirements are satisfied.

[μ PD44645094]

Operation	K	K#	BW0#
Write D0 to D8	L \rightarrow H	—	0
	—	L \rightarrow H	0
Write nothing	L \rightarrow H	—	1
	—	L \rightarrow H	1

Remarks 1. H : HIGH, L : LOW, \rightarrow : rising edge.

2. Assumes a WRITE cycle was initiated. BW0# can be altered for any portion of the BURST WRITE operation provided that the setup and hold requirements are satisfied.

[μ PD44645184]

Operation	K	K#	BW0#	BW1#
Write D0 to D17	L \rightarrow H	—	0	0
	—	L \rightarrow H	0	0
Write D0 to D8	L \rightarrow H	—	0	1
	—	L \rightarrow H	0	1
Write D9 to D17	L \rightarrow H	—	1	0
	—	L \rightarrow H	1	0
Write nothing	L \rightarrow H	—	1	1
	—	L \rightarrow H	1	1

Remarks 1. H : HIGH, L : LOW, \rightarrow : rising edge.

2. Assumes a WRITE cycle was initiated. BW0# and BW1# can be altered for any portion of the BURST WRITE operation provided that the setup and hold requirements are satisfied.

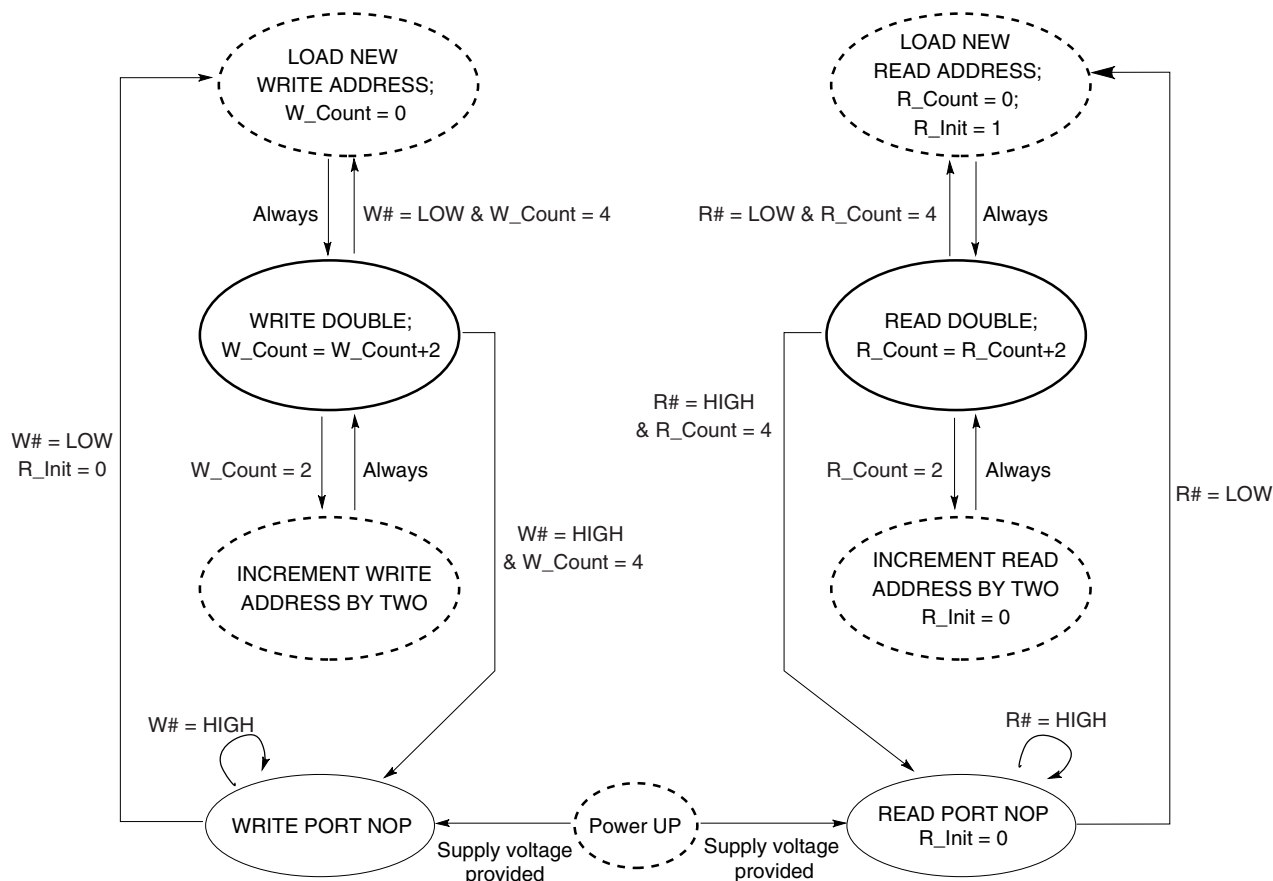
[μPD44645364]

Operation	K	K#	BW0#	BW1#	BW2#	BW3#
Write D0 to D35	L → H	—	0	0	0	0
	—	L → H	0	0	0	0
Write D0 to D8	L → H	—	0	1	1	1
	—	L → H	0	1	1	1
Write D9 to D17	L → H	—	1	0	1	1
	—	L → H	1	0	1	1
Write D18 to D26	L → H	—	1	1	0	1
	—	L → H	1	1	0	1
Write D27 to D35	L → H	—	1	1	1	0
	—	L → H	1	1	1	0
Write nothing	L → H	—	1	1	1	1
	—	L → H	1	1	1	1

Remarks 1. H : HIGH, L : LOW, → : rising edge.

2. Assumes a WRITE cycle was initiated. BW0# to BW3# can be altered for any portion of the BURST WRITE operation provided that the setup and hold requirements are satisfied.

Bus Cycle State Diagram



- Remarks**
1. The address is concatenated with two additional internal LSBs to facilitate burst operation. The address order is always fixed as: xxx...xxx+0, xxx...xxx+1, xxx...xxx+2, xxx...xxx+3. Bus cycle is terminated at the end of this sequence (burst count = 4).
 2. Read and write state machines can be active simultaneously. Read and write cannot be simultaneously initiated. Read takes precedence.
 3. State machine control timing is controlled by K.

Electrical Specifications

Absolute Maximum Ratings

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Supply voltage	V _{DD}		−0.5		+2.5	V
Output supply voltage	V _{DDQ}		−0.5		V _{DD}	V
Input voltage	V _{IN}		−0.5		V _{DD} + 0.5 (2.5 V MAX.)	V
Input / Output voltage	V _{I/O}		−0.5		V _{DDQ} + 0.5 (2.5 V MAX.)	V
Operating ambient temperature	T _A		0		70	°C
Storage temperature	T _{stg}		−55		+125	°C

Caution Exposing the device to stress above those listed in Absolute Maximum Ratings could cause permanent damage. The device is not meant to be operated under conditions outside the limits described in the operational section of this specification. Exposure to Absolute Maximum Rating conditions for extended periods may affect device reliability.

Recommended DC Operating Conditions (T_A = 0 to 70°C)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit	Note
Supply voltage	V _{DD}		1.7		1.9	V	
Output supply voltage	V _{DDQ}		1.4		V _{DD}	V	1
Input HIGH voltage	V _{IH} (DC)		V _{REF} + 0.1		V _{DDQ} + 0.3	V	1, 2
Input LOW voltage	V _{IL} (DC)		−0.3		V _{REF} − 0.1	V	1, 2
Clock input voltage	V _{IN}		−0.3		V _{DDQ} + 0.3	V	1, 2
Reference voltage	V _{REF}		0.68		0.95	V	

Notes 1. During normal operation, V_{DDQ} must not exceed V_{DD}.

2. Power-up: V_{IH} ≤ V_{DDQ} + 0.3 V and V_{DD} ≤ 1.7 V and V_{DDQ} ≤ 1.4 V for t ≤ 200 ms

Recommended AC Operating Conditions (T_A = 0 to 70°C)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit	Note
Input HIGH voltage	V _{IH} (AC)		V _{REF} + 0.2		—	V	1
Input LOW voltage	V _{IL} (AC)		—		V _{REF} − 0.2	V	1

<R>

Note 1. Overshoot: V_{IH} (AC) ≤ V_{DD} + 0.7 V (2.5 V MAX.) for t ≤ TKHKH/2

Undershoot: V_{IL} (AC) ≥ −0.5 V for t ≤ TKHKH/2

Control input signals may not have pulse widths less than TKHKL (MIN.) or operate at cycle rates less than TKHKH (MIN.).

<R> DC Characteristics (T_A = 0 to 70°C, V_{DD} = 1.8 ± 0.1 V)

Parameter	Symbol	Test condition			MIN.	TYP.	MAX.			Unit	Note
							x8, x9	x18	x36		
Input leakage current	I _{LI}				-2	-	+2			μA	
I/O leakage current	I _{LO}				-2	-	+2			μA	
Operating supply current (Read cycle / Write cycle)	I _{DD}	Note1	100% read cycles	-E37			T.B.D.			mA	
			and	-E40			T.B.D.				
			100% write cycles	-E50			T.B.D.				
			50% read cycles	-E37			T.B.D.				
			and	-E40			T.B.D.				
			50% write cycles	-E50			T.B.D.				
Standby supply current (NOP)	I _{SB1}	Note1		-E37			T.B.D.			mA	
				-E40			T.B.D.				
				-E50			T.B.D.				
Output HIGH voltage	V _{OH(Low)}	I _{OH} ≤ 0.1 mA			V _{DDQ} - 0.2	-	V _{DDQ}			V	4, 5
	V _{OH}	Note2			V _{DDQ} /2-0.12	-	V _{DDQ} /2+0.12			V	4, 5
Output LOW voltage	V _{OL(Low)}	I _{OL} ≤ 0.1 mA			V _{SS}	-	0.2			V	4, 5
	V _{OL}	Note3			V _{DDQ} /2-0.12	-	V _{DDQ} /2+0.12			V	4, 5

Notes 1. V_{IN} ≤ V_{IL} or V_{IN} ≥ V_{IH}, I_{I/O} = 0 mA, Cycle = MAX.

2. Outputs are impedance-controlled. |I_{OH}| = (V_{DDQ}/2)/(R_Q/5) ±15% for values of 175 Ω ≤ R_Q ≤ 350 Ω.

3. Outputs are impedance-controlled. I_{OL} = (V_{DDQ}/2)/(R_Q/5) ±15% for values of 175 Ω ≤ R_Q ≤ 350 Ω.

4. AC load current is higher than the shown DC values.

5. HSTL outputs meet JEDEC HSTL Class I standards.

Capacitance (T_A = 25°C, f = 1 MHz)

Parameter	Symbol	Test conditions	MIN.	TYP.	MAX.	Unit
Input capacitance (Address, Control)	C _{IN}	V _{IN} = 0 V		4	5	pF
Input / Output capacitance (D, Q, CQ, CQ#)	C _{I/O}	V _{I/O} = 0 V		6	7	pF
Clock Input capacitance	C _{clk}	V _{clk} = 0 V		5	6	pF

Remark These parameters are periodically sampled and not 100% tested.

Thermal Resistance

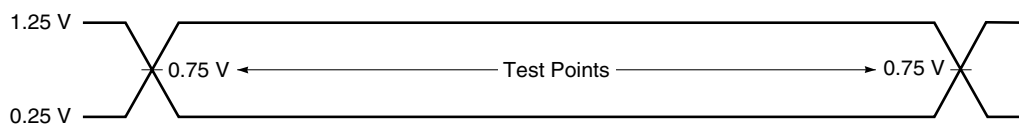
Parameter	Symbol	Test conditions	MIN.	TYP.	MAX.	Unit
Thermal resistance (junction – ambient)	θ _{j-a}			T.B.D.		°C/W
Thermal resistance (junction – case)	θ _{j-c}			T.B.D.		°C/W

Remark These parameters are simulated under the condition of air flow velocity = 1 m/s.

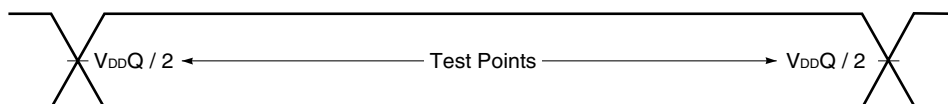
AC Characteristics ($T_A = 0$ to 70°C , $V_{DD} = 1.8 \pm 0.1$ V)

AC Test Conditions ($V_{DD} = 1.8 \pm 0.1$ V, $V_{DDQ} = 1.4$ V to V_{DD})

Input waveform (Rise / Fall time ≤ 0.3 ns)

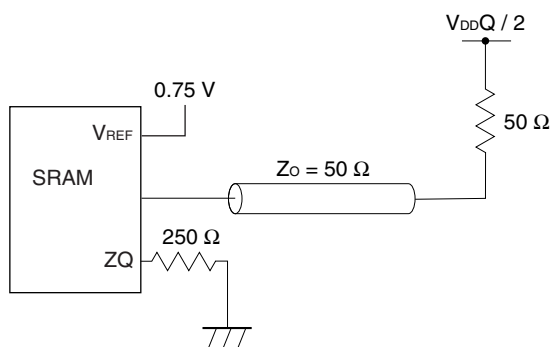


Output waveform



Output load condition

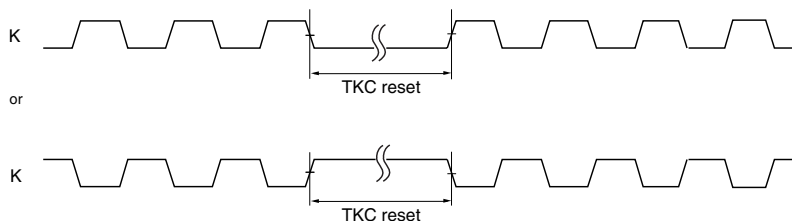
Figure 1. External load at test



Read and Write Cycle

Parameter		Symbol	-E37 (270 MHz)		-E40 (250 MHz)		-E50 (200 MHz)		Unit	Note
			MIN.	MAX.	MIN.	MAX.	MIN.	MAX.		
Clock										
Average Clock cycle time (K, K#, C, C#)		TKHKH	3.7	8.4	4.0	8.4	5.0	8.4	ns	1
Clock phase jitter (K, K#, C, C#)		TKC var	–	0.2	–	0.2	–	0.2	ns	2
Clock HIGH time (K, K#, C, C#)		TKHKL	1.5	–	1.6	–	2.0	–	ns	
Clock LOW time (K, K#, C, C#)		TKLKH	1.5	–	1.6	–	2.0	–	ns	
Clock HIGH to Clock# HIGH (K → K#, C → C#)		TKHK#H	1.7	–	1.8	–	2.2	–	ns	
Clock# HIGH to Clock HIGH (K# → K, C# → C)		TK#HKH	1.7	–	1.8	–	2.2	–	ns	
Clock to data clock (K → C, K# → C#)	250 to 270 MHz	TKHCH	0	1.65	–	–	–	–	ns	
	200 to 250 MHz		0	1.8	0	1.8	–	–		
	167 to 200 MHz		0	2.3	0	2.3	0	2.3		
	133 to 167 MHz		0	2.8	0	2.8	0	2.8		
	< 133 MHz		0	3.55	0	3.55	0	3.55		
DLL/PLL lock time (K, C)		TKC lock	1,024	–	1,024	–	1,024	–	Cycle	3
K static to DLL/PLL reset		TKC reset	30	–	30	–	30	–	ns	4
Output Times										
CQ HIGH to CQ# HIGH (CQ → CQ#)		TCQHCQ#H	1.5	–	1.65	–	2.15	–	ns	5
CQ# HIGH to CQ HIGH (CQ# → CQ)		TCQ#HCQH	1.5	–	1.65	–	2.15	–	ns	5
C, C# HIGH to output valid		TCHQV	–	0.45	–	0.45	–	0.45	ns	
C, C# HIGH to output hold		TCHQX	–0.45	–	–0.45	–	–0.45	–	ns	
C, C# HIGH to echo clock valid		TCHCQV	–	0.45	–	0.45	–	0.45	ns	
C, C# HIGH to echo clock hold		TCHCQX	–0.45	–	–0.45	–	–0.45	–	ns	
CQ, CQ# HIGH to output valid		TCQHCV	–	0.3	–	0.3	–	0.35	ns	6
CQ, CQ# HIGH to output hold		TCQHCVX	–0.3	–	–0.3	–	–0.35	–	ns	6
C HIGH to output High-Z		TCHQZ	–	0.45	–	0.45	–	0.45	ns	
C HIGH to output Low-Z		TCHQX1	–0.45	–	–0.45	–	–0.45	–	ns	
Setup Times										
Address valid to K rising edge		TAVKH	0.5	–	0.5	–	0.6	–	ns	7
Control inputs (R#, W#) valid to K rising edge		TIVKH	0.5	–	0.5	–	0.6	–	ns	7
Data inputs and write data select inputs (BWx#, NWx#) valid to K, K# rising edge		TDVKH	0.35	–	0.35	–	0.4	–	ns	7
Hold Times										
K rising edge to address hold		TKHAX	0.5	–	0.5	–	0.6	–	ns	7
K rising edge to control inputs (R#, W#) hold		TKHIX	0.5	–	0.5	–	0.6	–	ns	7
K, K# rising edge to data inputs and write data select inputs (BWx#, NWx#) hold		TKHDX	0.35	–	0.35	–	0.4	–	ns	7

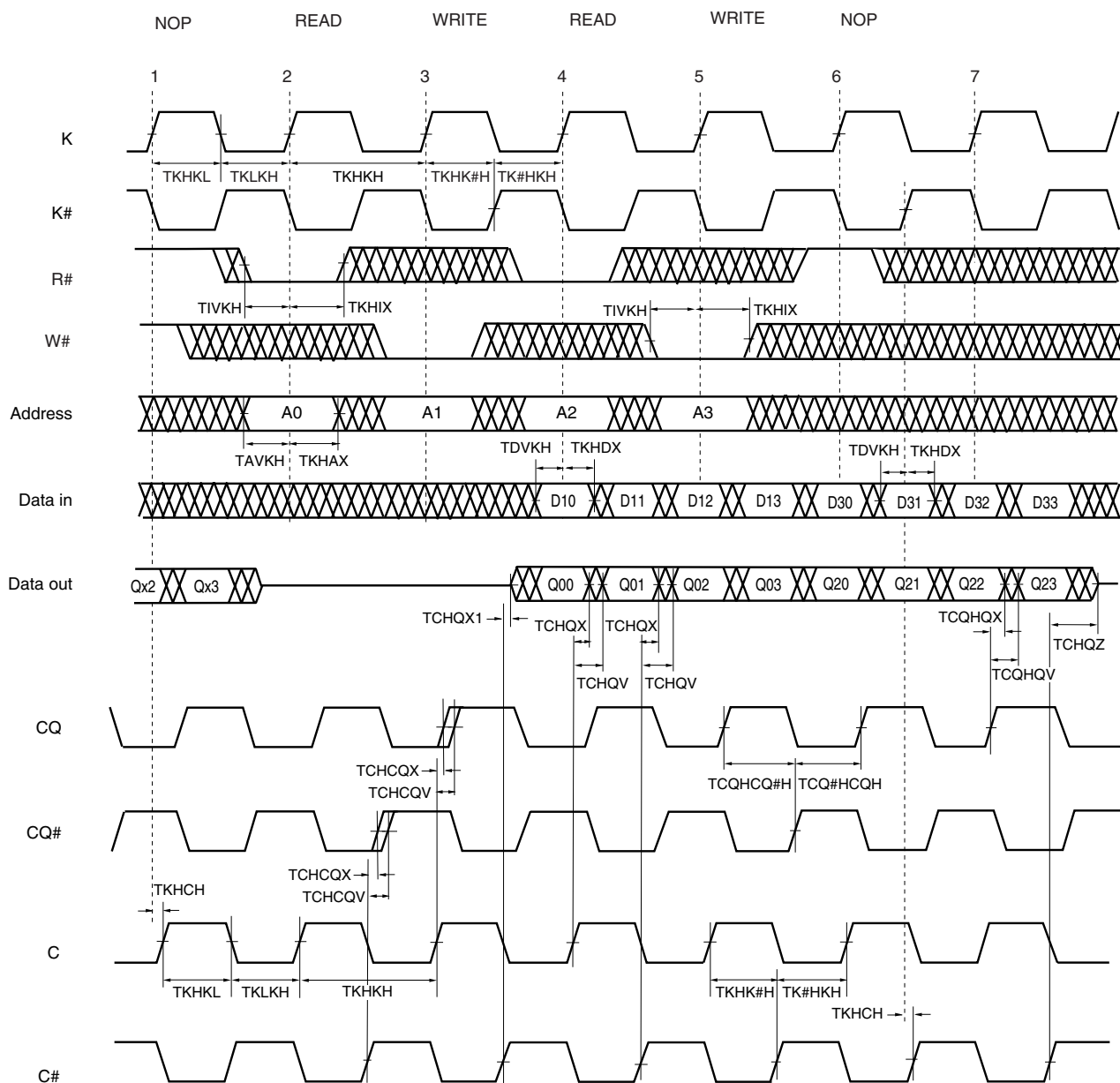
- <R> **Notes**
1. When debugging the system or board, these products can operate at a clock frequency slower than TKHKH (MAX.) without the DLL/PLL circuit being used, if DLL# = LOW. Read latency (RL) is changed to 1.0 clock in this operation. The AC/DC characteristics cannot be guaranteed, however.
 2. Clock phase jitter is the variance from clock rising edge to the next expected clock rising edge. TKC var (MAX.) indicates a peak-to-peak value.
 3. V_{DD} slew rate must be less than 0.1 V DC per 50 ns for DLL/PLL lock retention.
DLL/PLL lock time begins once V_{DD} and input clock are stable.
It is recommended that the device is kept NOP (R# = W# = HIGH) during these cycles.
 4. K input is monitored for this operation. See below for the timing.



- <R>
5. Guaranteed by design.
 6. Echo clock is very tightly controlled to data valid / data hold. By design, there is a ± 0.1 ns variation from echo clock to data. The data sheet parameters reflect tester guardbands and test setup variations.
 7. This is a synchronous device. All addresses, data and control lines must meet the specified setup and hold times for all latching clock edges.

- Remarks**
1. This parameter is sampled.
 2. Test conditions as specified with the output loading as shown in AC Test Conditions unless otherwise noted.
 3. Control input signals may not be operated with pulse widths less than TKHKL (MIN.).
 4. If C, C# are tied HIGH, K, K# become the references for C, C# timing parameters.
 5. V_{DDQ} is 1.5 V DC.

<R> Read and Write Timing



Remarks 1. Q00 refers to output from address A0+0.

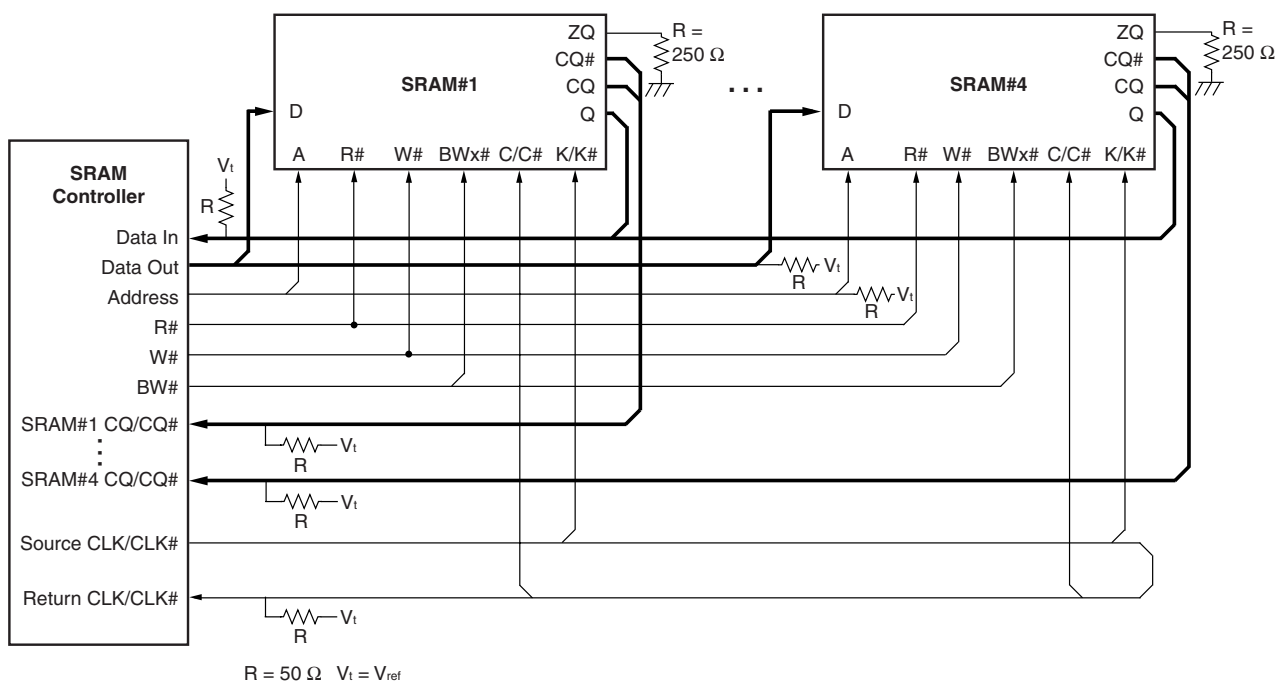
Q01 refers to output from the next internal burst address following A0, i.e., A0+1.

2. Outputs are disabled (high impedance) 3.5 clocks after the last READ ($R\# = \text{LOW}$) is input in the sequences of [READ]-[NOP]-[NOP], [READ]-[WRITE]-[NOP] and [READ]-[NOP]-[WRITE].

3. In this example, if address A2 = A1, data Q20 = D10, Q21 = D11, Q22 = D12 and Q23 = D13.

Write data is forwarded immediately as read results.

Application Example



Remark AC specifications are defined at the condition of SRAM outputs, CQ, CQ# and Q with termination.

JTAG Specification

These products support a limited set of JTAG functions as in IEEE standard 1149.1.

Test Access Port (TAP) Pins

Pin name	Pin assignments	Description
TCK	2R	Test Clock Input. All input are captured on the rising edge of TCK and all outputs propagate from the falling edge of TCK.
TMS	10R	Test Mode Select. This is the command input for the TAP controller state machine.
TDI	11R	Test Data Input. This is the input side of the serial registers placed between TDI and TDO. The register placed between TDI and TDO is determined by the state of the TAP controller state machine and the instruction that is currently loaded in the TAP instruction.
TDO	1R	Test Data Output. This is the output side of the serial registers placed between TDI and TDO. Output changes in response to the falling edge of TCK.

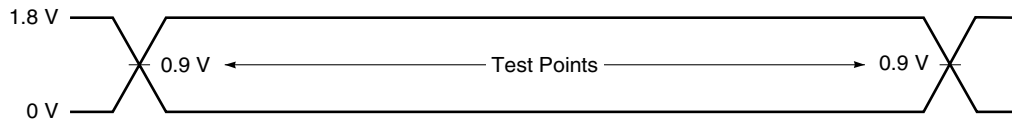
Remark The device does not have TRST (TAP reset). The Test-Logic Reset state is entered while TMS is held HIGH for five rising edges of TCK. The TAP controller state is also reset on the SRAM POWER-UP.

JTAG DC Characteristics (T_A = 0 to 70°C, V_{DD} = 1.8 ± 0.1 V, unless otherwise noted)

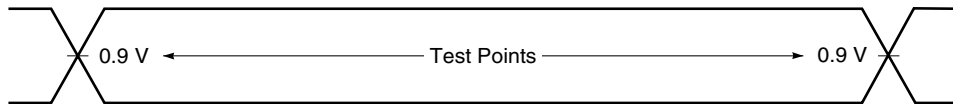
Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
JTAG Input leakage current	I _{LI}	0 V ≤ V _{IN} ≤ V _{DD}	−5.0	—	+5.0	μA
JTAG I/O leakage current	I _{LO}	0 V ≤ V _{IN} ≤ V _{DDQ} , Outputs disabled	−5.0	—	+5.0	μA
JTAG input HIGH voltage	V _{IH}		1.3	—	V _{DD} +0.3	V
JTAG input LOW voltage	V _{IL}		−0.3	—	+0.5	V
JTAG output HIGH voltage	V _{OH1}	I _{OHC} = 100 μA	1.6	—	—	V
	V _{OH2}	I _{OHT} = 2 mA	1.4	—	—	V
JTAG output LOW voltage	V _{OL1}	I _{OLC} = 100 μA	—	—	0.2	V
	V _{OL2}	I _{OLT} = 2 mA	—	—	0.4	V

JTAG AC Test Conditions

Input waveform (Rise / Fall time ≤ 1 ns)

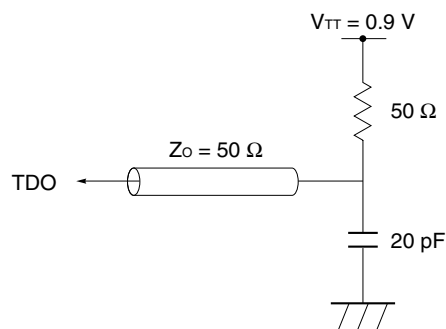


Output waveform



Output load

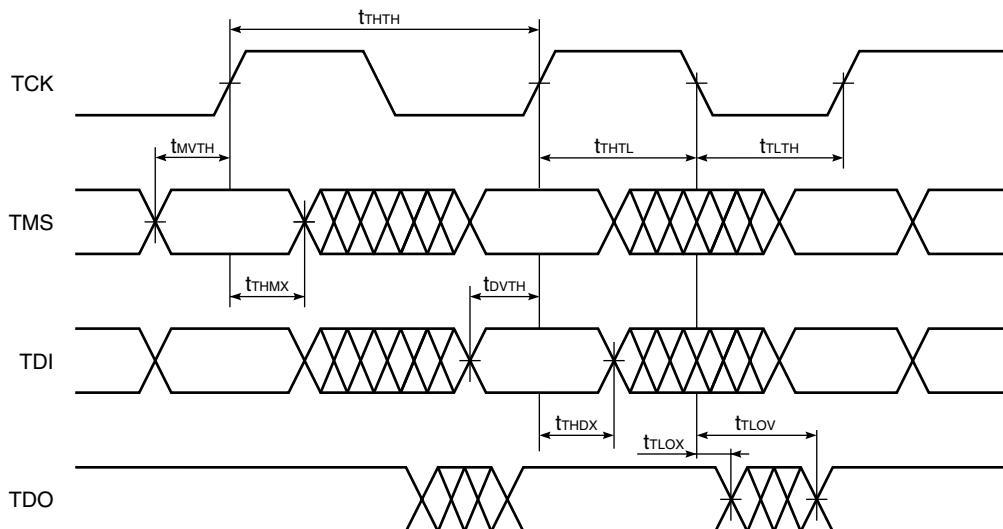
Figure 2. External load at test



JTAG AC Characteristics ($T_A = 0$ to 70°C)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Clock						
Clock cycle time	t_{THTH}		50	—	—	ns
Clock frequency	f_{TF}		—	—	20	MHz
Clock HIGH time	t_{HTHL}		20	—	—	ns
Clock LOW time	t_{LTHL}		20	—	—	ns
Output time						
TCK LOW to TDO unknown	t_{TLOX}		0	—	—	ns
TCK LOW to TDO valid	t_{TLOV}		—	—	10	ns
Setup time						
TMS setup time	t_{MVTH}		5	—	—	ns
TDI valid to TCK HIGH	t_{DVTH}		5	—	—	ns
Capture setup time	t_{CS}		5	—	—	ns
Hold time						
TMS hold time	t_{THMX}		5	—	—	ns
TCK HIGH to TDI invalid	t_{THDX}		5	—	—	ns
Capture hold time	t_{CH}		5	—	—	ns

JTAG Timing Diagram



Scan Register Definition (1)

Register name	Description
Instruction register	The instruction register holds the instructions that are executed by the TAP controller when it is moved into the run-test/idle or the various data register state. The register can be loaded when it is placed between the TDI and TDO pins. The instruction register is automatically preloaded with the IDCODE instruction at power-up whenever the controller is placed in test-logic-reset state.
Bypass register	The bypass register is a single bit register that can be placed between TDI and TDO. It allows serial test data to be passed through the RAMs TAP to another device in the scan chain with as little delay as possible.
ID register	The ID Register is a 32 bit register that is loaded with a device and vendor specific 32 bit code when the controller is put in capture-DR state with the IDCODE command loaded in the instruction register. The register is then placed between the TDI and TDO pins when the controller is moved into shift-DR state.
Boundary register	The boundary register, under the control of the TAP controller, is loaded with the contents of the RAMs I/O ring when the controller is in capture-DR state and then is placed between the TDI and TDO pins when the controller is moved to shift-DR state. Several TAP instructions can be used to activate the boundary register. The Scan Exit Order tables describe which device bump connects to each boundary register location. The first column defines the bit's position in the boundary register. The second column is the name of the input or I/O at the bump and the third column is the bump number.

Scan Register Definition (2)

Register name	Bit size	Unit
Instruction register	3	bit
Bypass register	1	bit
ID register	32	bit
Boundary register	109	bit

ID Register Definition

Part number	Organization	ID [31:28] vendor revision no.	ID [27:12] part no.	ID [11:1] vendor ID no.	ID [0] fix bit
μPD44645084	8M x 8	XXXX	0000 0000 1000 1000	00000010000	1
μPD44645094	8M x 9	XXXX	0000 0000 1000 1001	00000010000	1
μPD44645184	4M x 18	XXXX	0000 0000 1000 1010	00000010000	1
μPD44645364	2M x 36	XXXX	0000 0000 1000 1011	00000010000	1

SCAN Exit Order

Bit no.	Signal name				Bump ID
	x8	x9	x18	x36	
1	C#				6R
2	C				6P
3	A				6N
4	A				7P
5	A				7N
6	A				7R
7	A				8R
8	A				8P
9	A				9R
10	NC	Q0	Q0	Q0	11P
11	NC	D0	D0	D0	10P
12	NC	NC	NC	D9	10N
13	NC	NC	NC	Q9	9P
14	NC	NC	Q1	Q1	10M
15	NC	NC	D1	D1	11N
16	NC	NC	NC	D10	9M
17	NC	NC	NC	Q10	9N
18	Q0	Q1	Q2	Q2	11L
19	D0	D1	D2	D2	11M
20	NC	NC	NC	D11	9L
21	NC	NC	NC	Q11	10L
22	NC	NC	Q3	Q3	11K
23	NC	NC	D3	D3	10K
24	NC	NC	NC	D12	9J
25	NC	NC	NC	Q12	9K
26	Q1	Q2	Q4	Q4	10J
27	D1	D2	D4	D4	11J
28	ZQ				11H
29	NC	NC	NC	D13	10G
30	NC	NC	NC	Q13	9G
31	NC	NC	Q5	Q5	11F
32	NC	NC	D5	D5	11G
33	NC	NC	NC	D14	9F
34	NC	NC	NC	Q14	10F
35	Q2	Q3	Q6	Q6	11E
36	D2	D3	D6	D6	10E

Bit no.	Signal name				Bump ID
	x8	x9	x18	x36	
37	NC	NC	NC	D15	10D
38	NC	NC	NC	Q15	9E
39	NC	NC	Q7	Q7	10C
40	NC	NC	D7	D7	11D
41	NC	NC	NC	D16	9C
42	NC	NC	NC	Q16	9D
43	Q3	Q4	Q8	Q8	11B
44	D3	D4	D8	D8	11C
45	NC	NC	NC	D17	9B
46	NC	NC	NC	Q17	10B
47	CQ				11A
48	A	A	A	V _{SS}	10A
49	A				9A
50	A				8B
51	A				7C
52	NC				6C
53	R#				8A
54	NC	NC	NC	BW1#	7A
55	NW0#	BW0#	BW0#	BW0#	7B
56	K				6B
57	K#				6A
58	NC	NC	NC	BW3#	5B
59	NW1#	NC	BW1#	BW2#	5A
60	W#				4A
61	A				5C
62	A				4B
63	A				3A
64	A	A	V _{SS}	V _{SS}	2A
65	CQ#				1A
66	NC	NC	Q9	Q18	2B
67	NC	NC	D9	D18	3B
68	NC	NC	NC	D27	1C
69	NC	NC	NC	Q27	1B
70	NC	NC	Q10	Q19	3D
71	NC	NC	D10	D19	3C
72	NC	NC	NC	D28	1D

Bit no.	Signal name				Bump ID
	x8	x9	x18	x36	
73	NC	NC	NC	Q28	2C
74	Q4	Q5	Q11	Q20	3E
75	D4	D5	D11	D20	2D
76	NC	NC	NC	D29	2E
77	NC	NC	NC	Q29	1E
78	NC	NC	Q12	Q21	2F
79	NC	NC	D12	D21	3F
80	NC	NC	NC	D30	1G
81	NC	NC	NC	Q30	1F
82	Q5	Q6	Q13	Q22	3G
83	D5	D6	D13	D22	2G
84	DLL#				1H
85	NC	NC	NC	D31	1J
86	NC	NC	NC	Q31	2J
87	NC	NC	Q14	Q23	3K
88	NC	NC	D14	D23	3J
89	NC	NC	NC	D32	2K
90	NC	NC	NC	Q32	1K
91	Q6	Q7	Q15	Q24	2L
92	D6	D7	D15	D24	3L
93	NC	NC	NC	D33	1M
94	NC	NC	NC	Q33	1L
95	NC	NC	Q16	Q25	3N
96	NC	NC	D16	D25	3M
97	NC	NC	NC	D34	1N
98	NC	NC	NC	Q34	2M
99	Q7	Q8	Q17	Q26	3P
100	D7	D8	D17	D26	2N
101	NC	NC	NC	D35	2P
102	NC	NC	NC	Q35	1P
103	A				3R
104	A				4R
105	A				4P
106	A				5P
107	A				5N
108	A				5R
109	—				Internal

Remark Bump ID 10A of bit no. 48 can also be used as NC if the product is x36.

Bump ID 2A of bit no. 64 can also be used as NC if the product is x18 or x36.

The register always indicates LOW, however.

JTAG Instructions

Instructions	Description
EXTEST	The EXTEST instruction allows circuitry external to the component package to be tested. Boundary-scan register cells at output pins are used to apply test vectors, while those at input pins capture test results. Typically, the first test vector to be applied using the EXTEST instruction will be shifted into the boundary scan register using the PRELOAD instruction. Thus, during the update-IR state of EXTEST, the output drive is turned on and the PRELOAD data is driven onto the output pins.
IDCODE	The IDCODE instruction causes the ID ROM to be loaded into the ID register when the controller is in capture-DR mode and places the ID register between the TDI and TDO pins in shift-DR mode. The IDCODE instruction is the default instruction loaded in at power up and any time the controller is placed in the test-logic-reset state.
BYPASS	When the BYPASS instruction is loaded in the instruction register, the bypass register is placed between TDI and TDO. This occurs when the TAP controller is moved to the shift-DR state. This allows the board level scan path to be shortened to facilitate testing of other devices in the scan path.
SAMPLE / PRELOAD	SAMPLE / PRELOAD is a Standard 1149.1 mandatory public instruction. When the SAMPLE / PRELOAD instruction is loaded in the instruction register, moving the TAP controller into the capture-DR state loads the data in the RAMs input and Q pins into the boundary scan register. Because the RAM clock(s) are independent from the TAP clock (TCK) it is possible for the TAP to attempt to capture the I/O ring contents while the input buffers are in transition (i.e., in a metastable state). Although allowing the TAP to sample metastable input will not harm the device, repeatable results cannot be expected. RAM input signals must be stabilized for long enough to meet the TAPs input data capture setup plus hold time (t_{cs} plus t_{ch}). The RAMs clock inputs need not be paused for any other TAP operation except capturing the I/O ring contents into the boundary scan register. Moving the controller to shift-DR state then places the boundary scan register between the TDI and TDO pins.
SAMPLE-Z	If the SAMPLE-Z instruction is loaded in the instruction register, all RAM Q pins are forced to an inactive drive state (high impedance) and the boundary register is connected between TDI and TDO when the TAP controller is moved to the shift-DR state.

JTAG Instruction Coding

IR2	IR1	IR0	Instruction	Note
0	0	0	EXTEST	
0	0	1	IDCODE	
0	1	0	SAMPLE-Z	1
0	1	1	RESERVED	2
1	0	0	SAMPLE / PRELOAD	
1	0	1	RESERVED	2
1	1	0	RESERVED	2
1	1	1	BYPASS	

- Notes**
1. TRISTATE all Q pins and CAPTURE the pad values into a SERIAL SCAN LATCH.
 2. Do not use this instruction code because the vendor uses it to evaluate this product.

Output Pin States of CQ, CQ# and Q

Instructions	Control-Register Status	Output Pin Status	
		CQ, CQ#	Q
EXTEST	0	Update	High-Z
	1	Update	Update
IDCODE	0	SRAM	SRAM
	1	SRAM	SRAM
SAMPLE-Z	0	High-Z	High-Z
	1	High-Z	High-Z
SAMPLE	0	SRAM	SRAM
	1	SRAM	SRAM
BYPASS	0	SRAM	SRAM
	1	SRAM	SRAM

Remark The output pin statuses during each instruction vary according to the Control-Register status (value of Boundary Scan Register, bit no. 109).

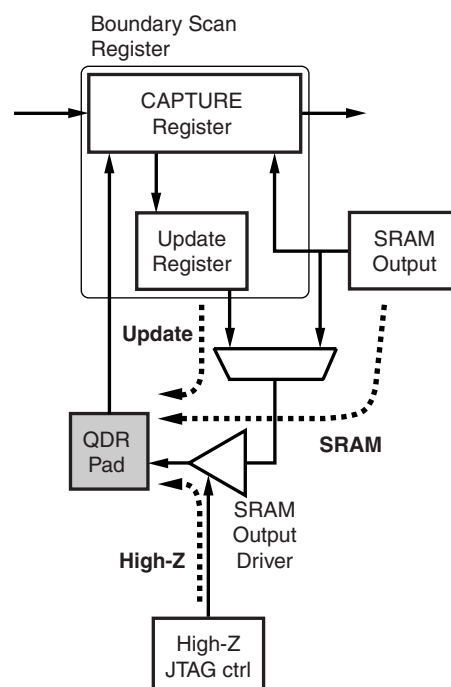
There are three statuses:

Update : Contents of the "Update Register" are output to the output pin (QDR Pad).

SRAM : Contents of the SRAM internal output "SRAM Output" are output to the output pin (QDR Pad).

High-Z : The output pin (QDR Pad) becomes high impedance by controlling of the "High-Z JTAG ctrl".

The Control-Register status is set during Update-DR at the EXTEST or SAMPLE instruction.



Boundary Scan Register Status of Output Pins CQ, CQ# and Q

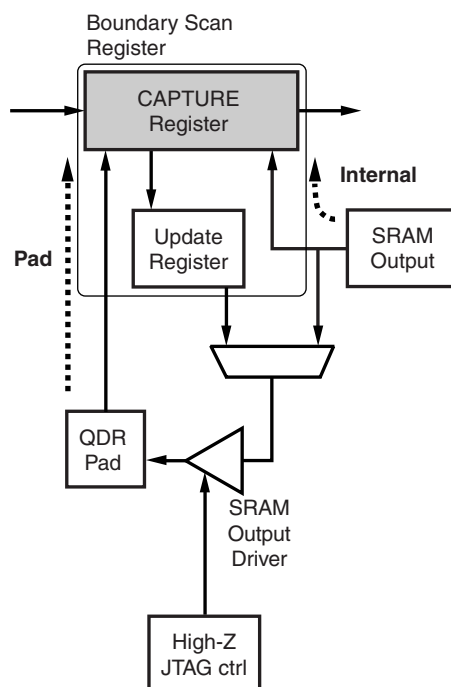
Instructions	SRAM Status	Boundary Scan Register Status		Note
		CQ, CQ#	Q	
EXTEST	READ (Low-Z)	Pad	Pad	
	NOP (High-Z)	Pad	Pad	
IDCODE	READ (Low-Z)	–	–	No definition
	NOP (High-Z)	–	–	
SAMPLE-Z	READ (Low-Z)	Pad	Pad	
	NOP (High-Z)	Pad	Pad	
SAMPLE	READ (Low-Z)	Internal	Internal	
	NOP (High-Z)	Internal	Pad	
BYPASS	READ (Low-Z)	–	–	No definition
	NOP (High-Z)	–	–	

Remark The Boundary Scan Register statuses during execution each instruction vary according to the instruction code and SRAM operation mode.

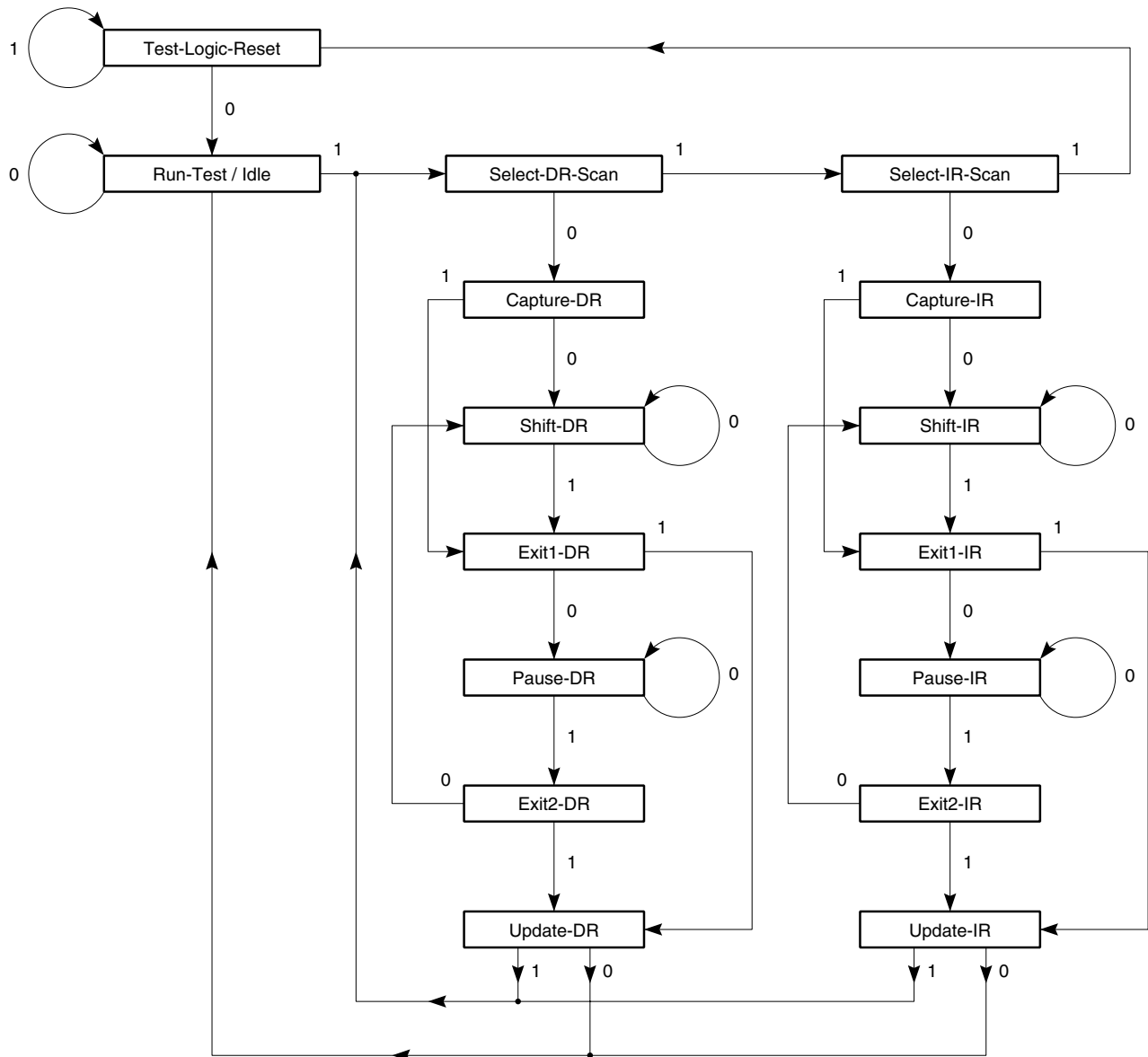
There are two statuses:

Pad : Contents of the output pin (QDR Pad) are captured in the “CAPTURE Register” in the Boundary Scan Register.

Internal : Contents of the SRAM internal output “SRAM Output” are captured in the “CAPTURE Register” in the Boundary Scan Register.



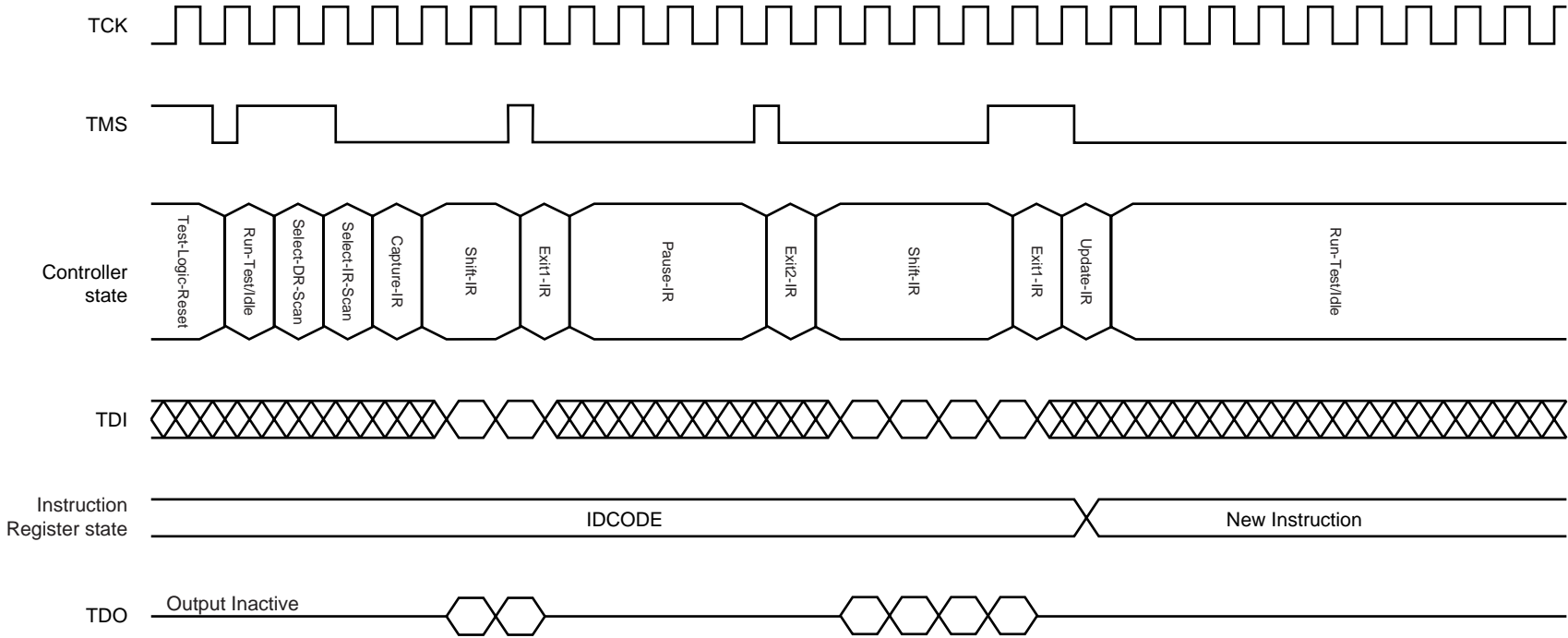
TAP Controller State Diagram



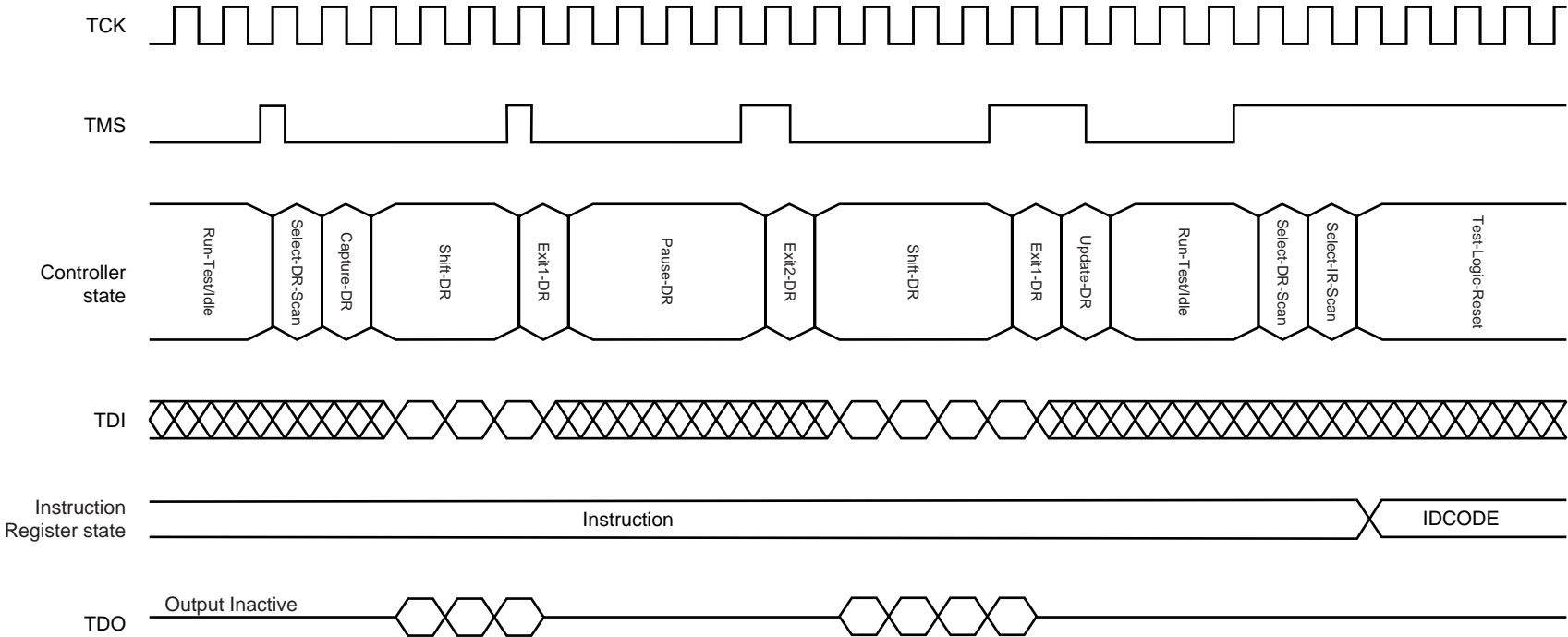
Disabling the Test Access Port

It is possible to use this device without utilizing the TAP. To disable the TAP Controller without interfering with normal operation of the device, TCK must be tied to V_{SS} to preclude mid level inputs. TDI and TMS may be left open but fix them to V_{DD} via a resistor of about 1 kΩ when the TAP controller is not used. TDO should be left unconnected also when the TAP controller is not used.

Test Logic Operation (Instruction Scan)

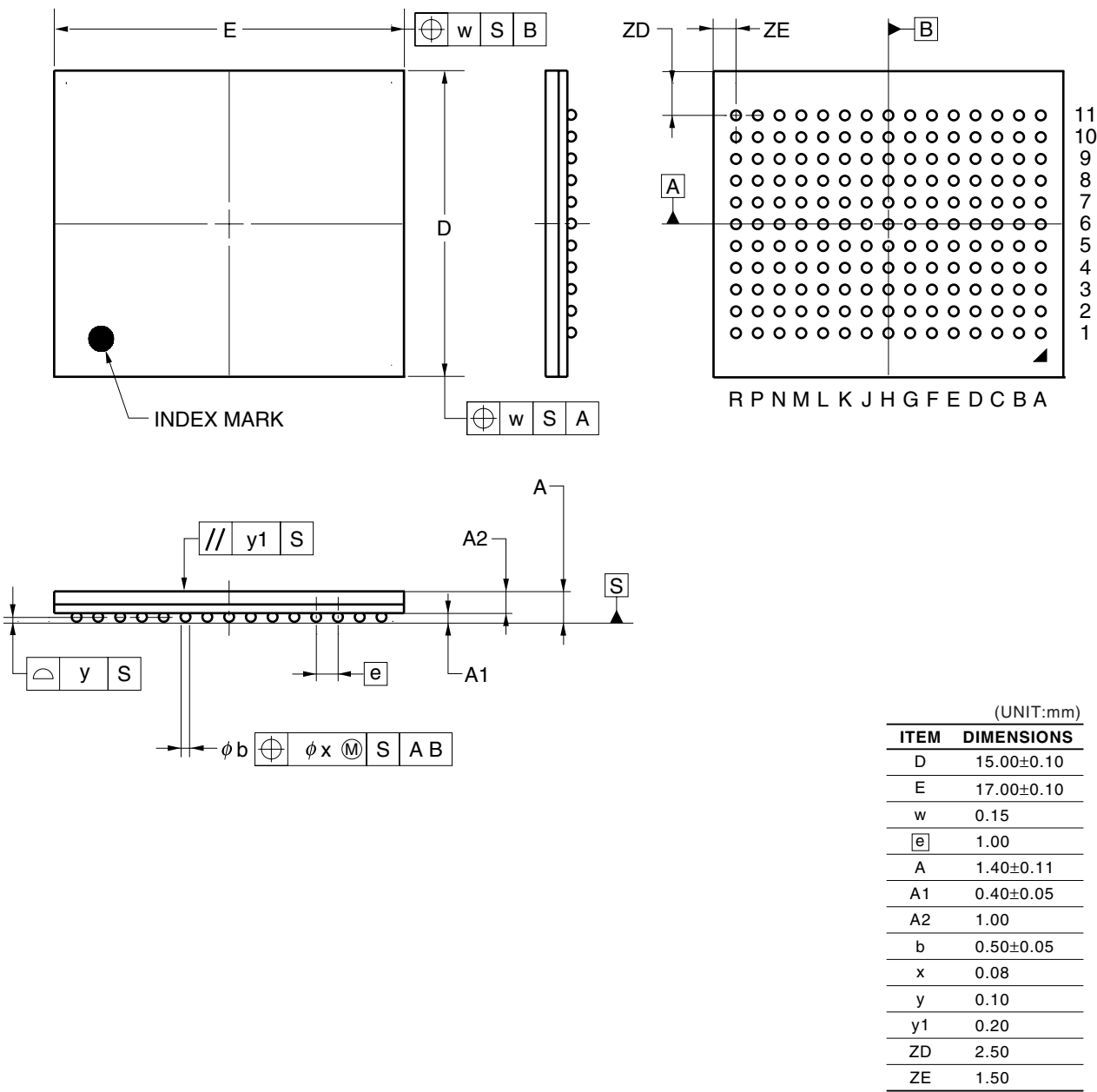


Test Logic (Data Scan)



Package Drawing

165-PIN PLASTIC BGA (15x17)



This package drawing is a preliminary version. It may be changed in the future.

Recommended Soldering Condition

Please consult with our sales offices for soldering conditions of these products.

Types of Surface Mount Devices

μPD44645084F5-FQ1 : 165-pin PLASTIC BGA (15 x 17)

μPD44645094F5-FQ1 : 165-pin PLASTIC BGA (15 x 17)

μPD44645184F5-FQ1 : 165-pin PLASTIC BGA (15 x 17)

μPD44645364F5-FQ1 : 165-pin PLASTIC BGA (15 x 17)

μPD44645084F5-FQ1-A : 165-pin PLASTIC BGA (15 x 17)

μPD44645094F5-FQ1-A : 165-pin PLASTIC BGA (15 x 17)

μPD44645184F5-FQ1-A : 165-pin PLASTIC BGA (15 x 17)

μPD44645364F5-FQ1-A : 165-pin PLASTIC BGA (15 x 17)

Revision History

Edition/ Date	Page		Type of revision	Location	Description (Previous edition → This edition)
	This edition	Previous edition			
2nd edition/ Feb. 2007	p.8	p.8	Modification	Pin Identification ZQ, DLL#, NC	Text has been modified.
	p.11	pp.11, 12	Modification	Power-On Sequence in QDR II SRAM	Text and timing chart have been modified.
	p.16	p.17	Modification	Recommended AC Operating Conditions	Note 1 has been modified.
	p.17	p.18	Modification	DC Characteristics	Operating supply current has been modified.
	p.19	p.20	Addition	Read and Write Cycle	TCQHCQ#H and TCQ#HCQH have been added.
	p.20	p.21	Modification		Note 1 has been modified.
			Addition		Note 4, 5 have been added.
	p.21	p.22	Addition	Read and Write Timing	TCQHGX, TCQHCQ#H and TCQ#HCQH have been added.
			Modification		Remark 2 has been modified.

[MEMO]

[MEMO]

NOTES FOR CMOS DEVICES

① VOLTAGE APPLICATION WAVEFORM AT INPUT PIN

Waveform distortion due to input noise or a reflected wave may cause malfunction. If the input of the CMOS device stays in the area between V_{IL} (MAX) and V_{IH} (MIN) due to noise, etc., the device may malfunction. Take care to prevent chattering noise from entering the device when the input level is fixed, and also in the transition period when the input level passes through the area between V_{IL} (MAX) and V_{IH} (MIN).

② HANDLING OF UNUSED INPUT PINS

Unconnected CMOS device inputs can be cause of malfunction. If an input pin is unconnected, it is possible that an internal input level may be generated due to noise, etc., causing malfunction. CMOS devices behave differently than Bipolar or NMOS devices. Input levels of CMOS devices must be fixed high or low by using pull-up or pull-down circuitry. Each unused pin should be connected to V_{DD} or GND via a resistor if there is a possibility that it will be an output pin. All handling related to unused pins must be judged separately for each device and according to related specifications governing the device.

③ PRECAUTION AGAINST ESD

A strong electric field, when exposed to a MOS device, can cause destruction of the gate oxide and ultimately degrade the device operation. Steps must be taken to stop generation of static electricity as much as possible, and quickly dissipate it when it has occurred. Environmental control must be adequate. When it is dry, a humidifier should be used. It is recommended to avoid using insulators that easily build up static electricity. Semiconductor devices must be stored and transported in an anti-static container, static shielding bag or conductive material. All test and measurement tools including work benches and floors should be grounded. The operator should be grounded using a wrist strap. Semiconductor devices must not be touched with bare hands. Similar precautions need to be taken for PW boards with mounted semiconductor devices.

④ STATUS BEFORE INITIALIZATION

Power-on does not necessarily define the initial status of a MOS device. Immediately after the power source is turned ON, devices with reset functions have not yet been initialized. Hence, power-on does not guarantee output pin levels, I/O settings or contents of registers. A device is not initialized until the reset signal is received. A reset operation must be executed immediately after power-on for devices with reset functions.

⑤ POWER ON/OFF SEQUENCE

In the case of a device that uses different power supplies for the internal operation and external interface, as a rule, switch on the external power supply after switching on the internal power supply. When switching the power supply off, as a rule, switch off the external power supply and then the internal power supply. Use of the reverse power on/off sequences may result in the application of an overvoltage to the internal elements of the device, causing malfunction and degradation of internal elements due to the passage of an abnormal current.

The correct power on/off sequence must be judged separately for each device and according to related specifications governing the device.

⑥ INPUT OF SIGNAL DURING POWER OFF STATE

Do not input signals or an I/O pull-up power supply while the device is not powered. The current injection that results from input of such a signal or I/O pull-up power supply may cause malfunction and the abnormal current that passes in the device at this time may cause degradation of internal elements. Input of signals during the power off state must be judged separately for each device and according to related specifications governing the device.

QDR RAMs and Quad Data Rate RAMs comprise a new series of products developed by Cypress Semiconductor, Renesas, IDT, NEC Electronics, and Samsung.

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