PAL22V10G
PAL22VP10G

Universal PAL® Device

Features

- **Ultra high speed supports today's and tomorrow's fastest microprocessors**
  - **— t_{PD} = 4 ns**
  - **— t_S = 2.5 ns**
  - **— f_{MAX} = 166 MHz (External)**
- **Reduced ground bounce and undershoot**
- **PLCC and LCC packages with additional V_{CC} and V_{SS} pins for lowest ground bounce**
- **Up to 22 inputs and 10 outputs for more logic power**
- **Variable product terms**
  - **— 8 to 16 per output**
- **10 user-programmable output macrocells**
  - **— Output polarity control**
  - **— Registered or combinatorial operation**
  - **— 2 new feedback paths (PAL22VP10G)**
- **Synchronous PRESET, asynchronous RESET, and PRELOAD capability for flexible design and testability**
- **High reliability**
  - **— Proven Ti-W fuse technology**
  - **— AC and DC tested at the factory**
- **Security Fuse**

Functional Description

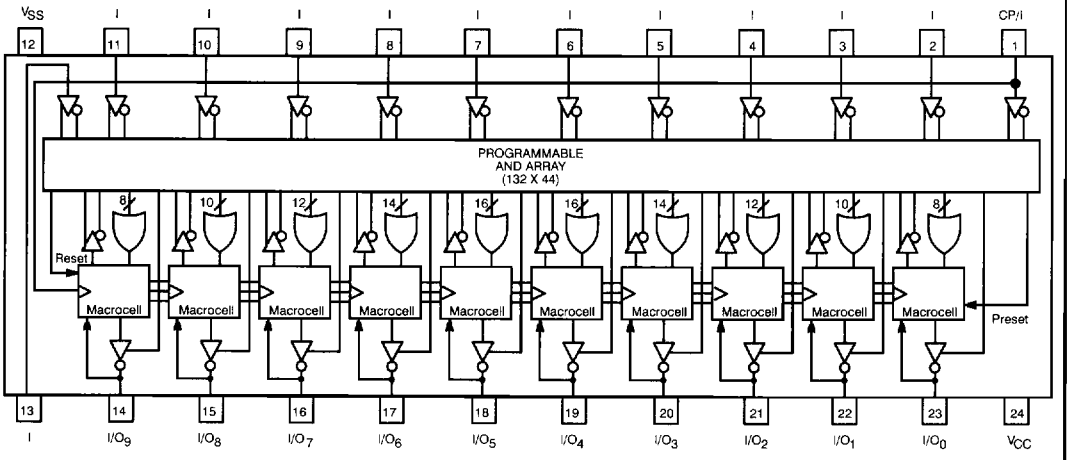
The Cypress PAL22V10G and PAL22VP10G are second-generation programmable array logic devices. Using BiCMOS process and Ti-W fuses, the PAL22V10G and PAL22VP10G use the familiar sum-of-products (AND-OR) logic structure and a new concept, the programmable macrocell.

Both the PAL22V10G and PAL22VP10G provide 12 dedicated input pins and 10 I/O pins (see Logic Block Diagram). By selecting each I/O pin as either permanent or temporary input, up to 22 inputs can be achieved. Applications requiring up to 21 inputs and a single output, down to 12 inputs and 10 outputs can be realized. The output enable product term available on each I/O allows this selection.

The PAL22V10G and PAL22VP10G feature variable product term architecture, where 8 to 16 product terms are allocated to each output. This structure permits more applications to be implemented with these devices than with other PAL devices that have fixed number of product terms for each output.

2

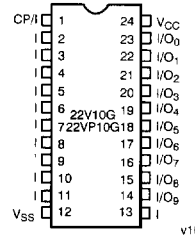
Logic Block Diagram and PDIP (P)/CDIP (D) Pin Configuration



v10g-1

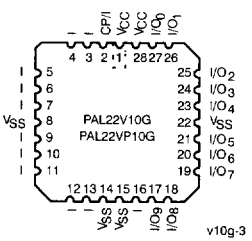
Pin Configurations

DIP (P, D)
Top View



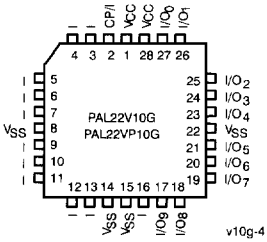
v10g-2

LCC (L)
Top View



v10g-3

PLCC (J)
Top View



v10g-4

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Functional Description (continued)

Additional features include common synchronous preset and asynchronous reset product terms. They eliminate the need to use standard product terms for initialization functions

Both the PAL22V10G and PAL22VP10G automatically reset on power-up. In addition, the preload capability allows the output registers to be set to any desired state during testing.

A security fuse is provided on each of these two devices to prevent copying of the device fuse pattern.

With the programmable macrocells and variable product term architecture, the PAL22V10G and PAL22VP10G can implement logic functions in the 700 to 800 gate array complexity, with the inherent advantages of programmable logic.

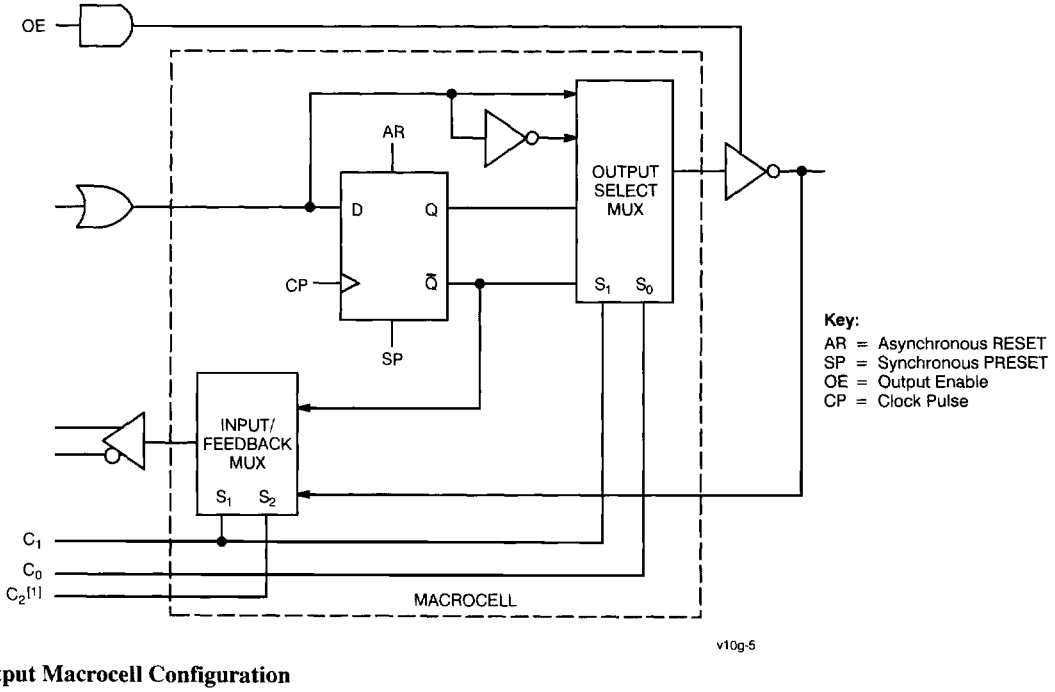
Programmable Macrocell

The PAL22V10G and PAL22VP10G each has 10 programmable output macrocells (see Macrocell figure). On the PAL22V10G two fuses (C_1 and C_0) can be programmed to configure output in one of four ways. Accordingly, each output can be registered or combinatorial with an active HIGH or active LOW polarity. The feedback to the array is also from this output (see *Figure 1*). An additional fuse (C_2) in the PAL22VP10G provides for two feedback paths (see *Figure 2*).

Programming

The PAL22V10G and PAL22VP10G can be programmed using the *Impulse3* programmer available from Cypress Semiconductor and also with Data I/O, Logical Devices, STAG and other programmers. Please contact your local Cypress representative for further information.

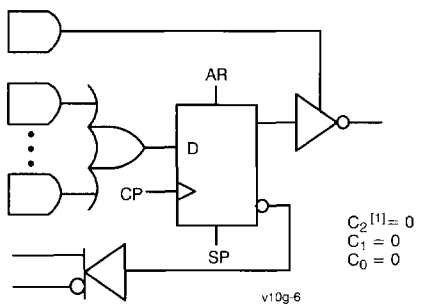
Macrocell



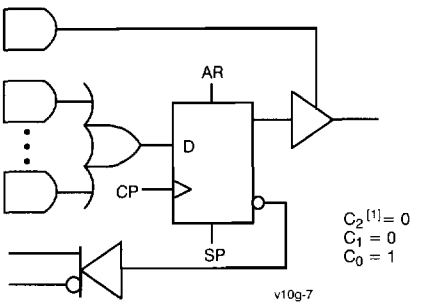
Output Macrocell Configuration

C_2[1]	C_1	C_0	Output Type	Polarity	Feedback
0	0	0	Registered	Active LOW	Registered
0	0	1	Registered	Active HIGH	Registered
X	1	0	Combinatorial	Active LOW	I/O
X	1	1	Combinatorial	Active HIGH	I/O
1	0	0	Registered	Active LOW	I/O[1]
1	0	1	Registered	Active HIGH	I/O[1]

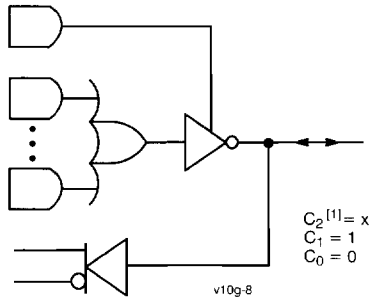
Notes:
1. PAL22VP10G only.



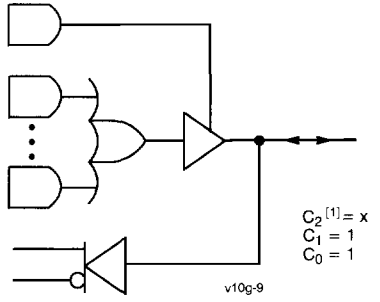
REGISTER FEEDBACK, REGISTERED, ACTIVE-LOW OUTPUT



REGISTER FEEDBACK, REGISTERED, ACTIVE-HIGH OUTPUT

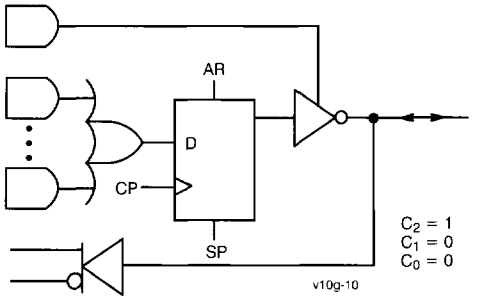


I/O FEEDBACK, COMBINATORIAL, ACTIVE-LOW OUTPUT

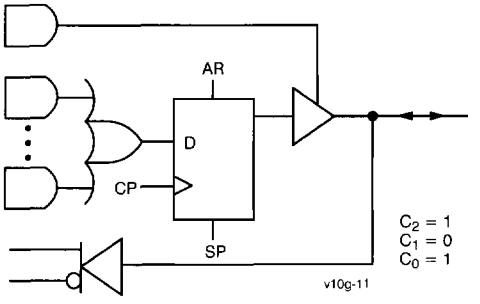


I/O FEEDBACK, COMBINATORIAL, ACTIVE-HIGH OUTPUT

Figure 1. PAL22V10G and PAL22VP10G Macrocell Configurations



I/O FEEDBACK, REGISTERED, ACTIVE-LOW OUTPUT



I/O FEEDBACK, REGISTERED, ACTIVE-HIGH OUTPUT

Figure 2. Additional Macrocell Configurations for the PAL22VP10G

Selection Guide

		22V10G-4 22VP10G-4	22V10G-5 22VP10G-5	22V10G-6 22VP10G-6	22V10G-7 22VP10G-7	22V10G-10 22VP10G-10
I_{CC} (mA)	Commercial	190	190	190	190	190
	Military				190	190
t_{PD} (ns)	Commercial	4	5	6.0	7.5	10
	Military				7.5	10
t_S (ns)	Commercial	2.5	2.5	3.0	3.0	3.6
	Military				3.0	3.6
t_{CO} (ns)	Commercial	3.5	4/4.5	5.5	6.0	7.5
	Military				6.0	7.5
f_{MAX} (MHz) (External)	Commercial	166	153.8	117	111	90
	Military				111	90

Maximum Ratings

(Above which the useful life may be impaired. For user guidelines, not tested.)

Storage Temperature ..... −65°C to +150°C

Ambient Temperature with Power Applied ..... −55°C to +125°C

Supply Voltage to Ground Potential ..... −0.5V to +7.0V

DC Voltage Applied to Outputs in High Z State ..... −0.5V to V_{CC}

DC Input Voltage ..... −0.5V to V_{CC}

DC Input Current ..... − 30 mA to +5 mA (except during programming)

DC Program Voltage 10V

Junction Temperature (PLCC) ..... 150°C

Operating Range

Range	Ambient Temperature	V_{CC}
Commercial	0°C to +70°C	5V ± 5%
Military[2]	−55°C to +125°C	5V ± 10%

DC Electrical Characteristics Over the Operating Range

Parameter	Description	Test Conditions			Min.	Max.	Unit
V_{OH}	Output HIGH Voltage	V_{CC} = Min., V_{IN} = V_{IH} or V_{IL}	I_{OH} = −3.2 mA	Com'l	2.4		V
			I_{OH} = −2 mA	Mil	2.4		V
V_{OL}	Output LOW Voltage	V_{CC} = Min., V_{IN} = V_{IH} or V_{IL}	I_{OL} = 16 mA	Com'l		0.5	V
			I_{OL} = 12 mA	Mil		0.5	V
V_{IH}	Input HIGH Voltage	Guaranteed Input Logical HIGH Voltage for All Inputs[3]			2.0		V
V_{IL}	Input LOW Voltage	Guaranteed Input Logical LOW Voltage for All Inputs[3]				0.8	V
I_{IX}	Input Leakage Current	$V_{SS} \le V_{IN} \le 2.7V$, V_{CC} = Max.			−250	50	µA
I_I	Maximum Input Current	V_{IN} = V_{CC}, V_{CC} = Max.		Com'l		100	µA
				Mil		250	µA
I_{OZ}	Output Leakage Current	V_{CC} = Max., $V_{SS} \le V_{OUT} \le V_{CC}$			−100	100	µA
I_{SC}	Output Short Circuit Current	V_{CC} = Max., V_{OUT} = 0.5V[4]			−30	−120	mA
I_{CC}	Power Supply Current	V_{CC} = Max., V_{IN} = GND, Outputs Open		Com'l		190	mA
				Mil		190	

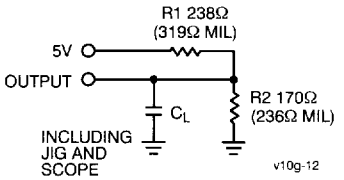
Notes:

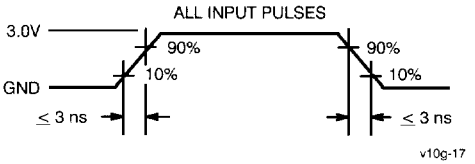
2. t_A is the "instant on" case temperature.
3. These are absolute values with respect to device ground. All overshoots due to system or tester noise are included.
4. Not more than one output should be tested at a time. Duration of the short circuit should not be more than one second. V_{OUT} = 0.5V has been chosen to avoid test problems caused by tester ground degradation.

Capacitance[5]

Parameter	Description	Typ.	Unit
C_{IN}	Input Capacitance	6	pF
C_{OUT}	Output Capacitance	8	pF

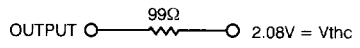
AC Test Loads and Waveforms





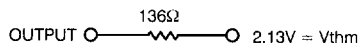
C_L[6] = 50 pF

Equivalent to: THÉVENIN EQUIVALENT

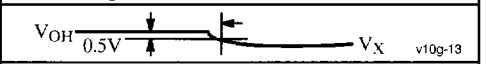
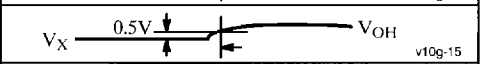
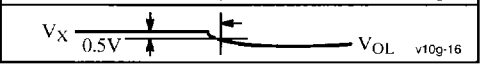


Commercial

Equivalent to: THÉVENIN EQUIVALENT



Military

Parameter	V_X	Output Waveform—Measurement Level
$t_{ER(-)}$	1.5V	 v10g-13
$t_{ER(+)}$	2.6V	 v10g-14
$t_{EA(+)}$	1.5V	 v10g-15
$t_{EA(-)}$	1.5V	 v10g-16

Notes:
5. Tested initially and after any design or process changes that may affect these parameters.
6. C_L = 5 pF for t_{ER} measurement for all packages.

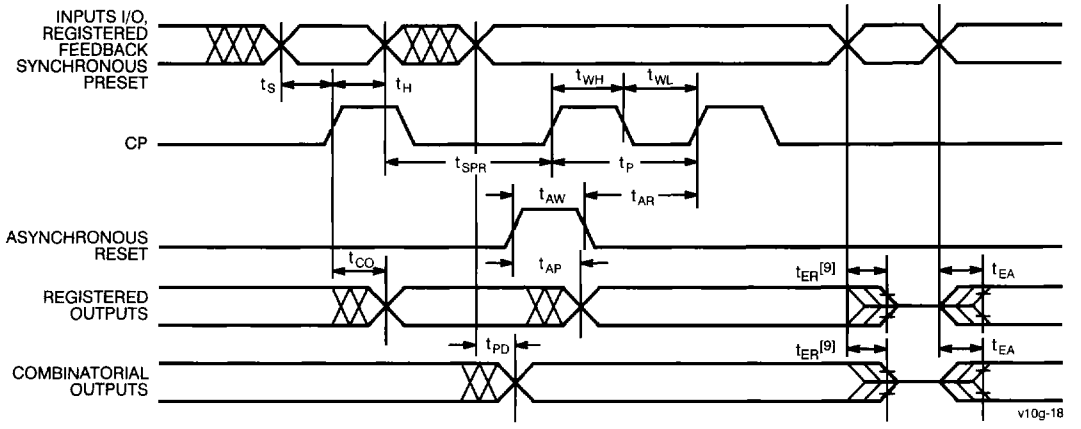
Switching Characteristics[7]

Parameter	Description	22V10G−4 22VP10G−4		22V10G−5 22VP10G−5		22V10G−6 22VP10G−6		22V10G−7 22VP10G−7		22V10G−10 22VP10G−10		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
t_{PD}	Input to Output Propagation Delay[8]	1	4	1	5	1	6	2	7.5	2	10	ns
t_{EA}	Input to Output Enable Delay	1	5	1	6	1	6	2	7.5	2	10	ns
t_{ER}	Input to Output Disable Delay[9]	1	4	1	5	1	6	2	7.5	2	10	ns
t_{CO}	Clock to Output Delay[8]	1	3.5	1	4	1	5.5	1	6.0	1	7.5	ns
t_S	Input or Feedback Set-Up Time	2.5		2.5		3		3		3.6		ns
t_H	Input Hold Time	0		0		0		0		0		ns
t_P	External Clock Period (t_{CO} + t_S)	6.0		6.5		8.5		9		11.1		ns
t_{WH}	Clock Width HIGH[5]	2.0		2.5		3		3		3		ns
t_{WL}	Clock Width LOW[5]	2.0		2.5		3		3		3		ns
f_{MAX1}	External Maximum Frequency ($1/(t_{CO} + t_S)$)[10]	166		153.8		117		111		90		MHz
f_{MAX2}	Data Path Maximum Frequency [5, 11, 12]	250		200		166		166		133		MHz
f_{MAX3}	Internal Feedback Maximum Frequency ($1/(t_{CF} + t_S)$)[9, 13]	181.8		181.8		142		133		100		MHz
t_{CF}	Register Clock to Feedback Input[14]		3		3		4		4.5		6.4	ns
t_{AW}	Asynchronous Reset Width	5		6		7.5		8.5		10		ns
t_{AR}	Asynchronous Reset Recovery Time	4		4		4		5		6		ns
t_{AP}	Asynchronous Reset to Registered Output Delay	2	6	2	7	2	11	2	12	2	12	ns
t_{SPR}	Synchronous Preset Recovery Time	4		4		4		5		6		ns
t_{PR}	Power-Up Reset Time[15]	1		1		1		1		1		µs

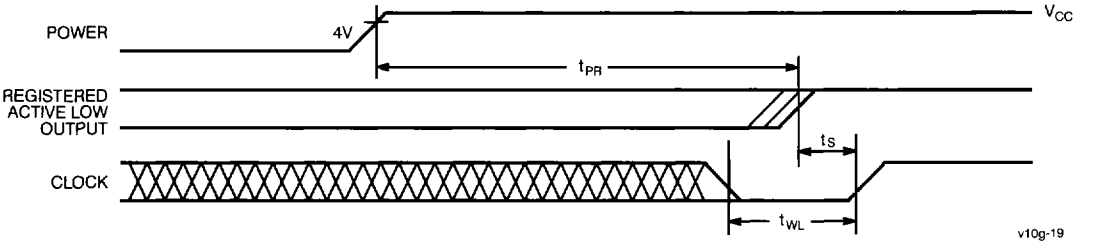
Notes:

7. AC test load used for all parameters except where noted.
8. This specification is guaranteed for all device outputs changing state in a given access cycle.
9. This parameter is measured as the time after output disable input that the previous output data state remains stable on the output. This delay is measured to the point at which a previous HIGH level has fallen to 0.5 volts below V_{OH} min. or a previous LOW level has risen to 0.5 volts above V_{OL} max.
10. This specification indicates the guaranteed maximum frequency at which a state machine configuration with external feedback can operate.
11. This specification indicates the guaranteed maximum frequency at which an individual output register can be cycled.
12. Lesser of $1/(t_{WH} + t_{WL})$, $1/t_{CO}$ or $1/(t_S + t_H)$.
13. This specification indicates the guaranteed maximum frequency at which a state machine configuration with internal-only feedback can operate.
14. This parameter is calculated from the clock period at f_{MAX} internal (f_{MAX3}) as measured (see Note 11) minus t_S.
15. The registers in the PAL22V10G and PAL22VP10G have been designed with the capability to reset during system power-up. Following power-up, all registers will be reset to a logic LOW state. The output state will depend on the polarity of the output buffer. This feature is useful in establishing state machine initialization. To insure proper operation, the rise in V_{CC} must be monotonic and the timing constraints depicted in power-up reset waveforms must be satisfied.

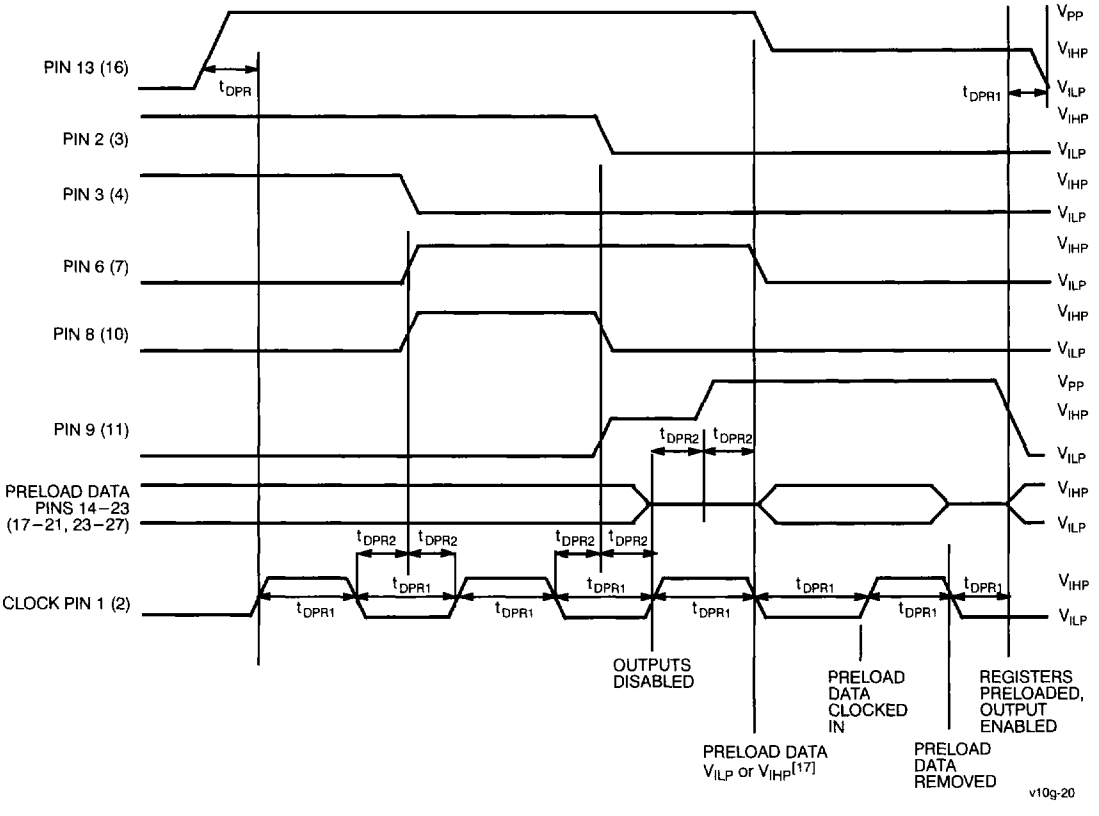
Switching Waveform



Power-Up Reset Waveform[15]



Preload Waveform[16]

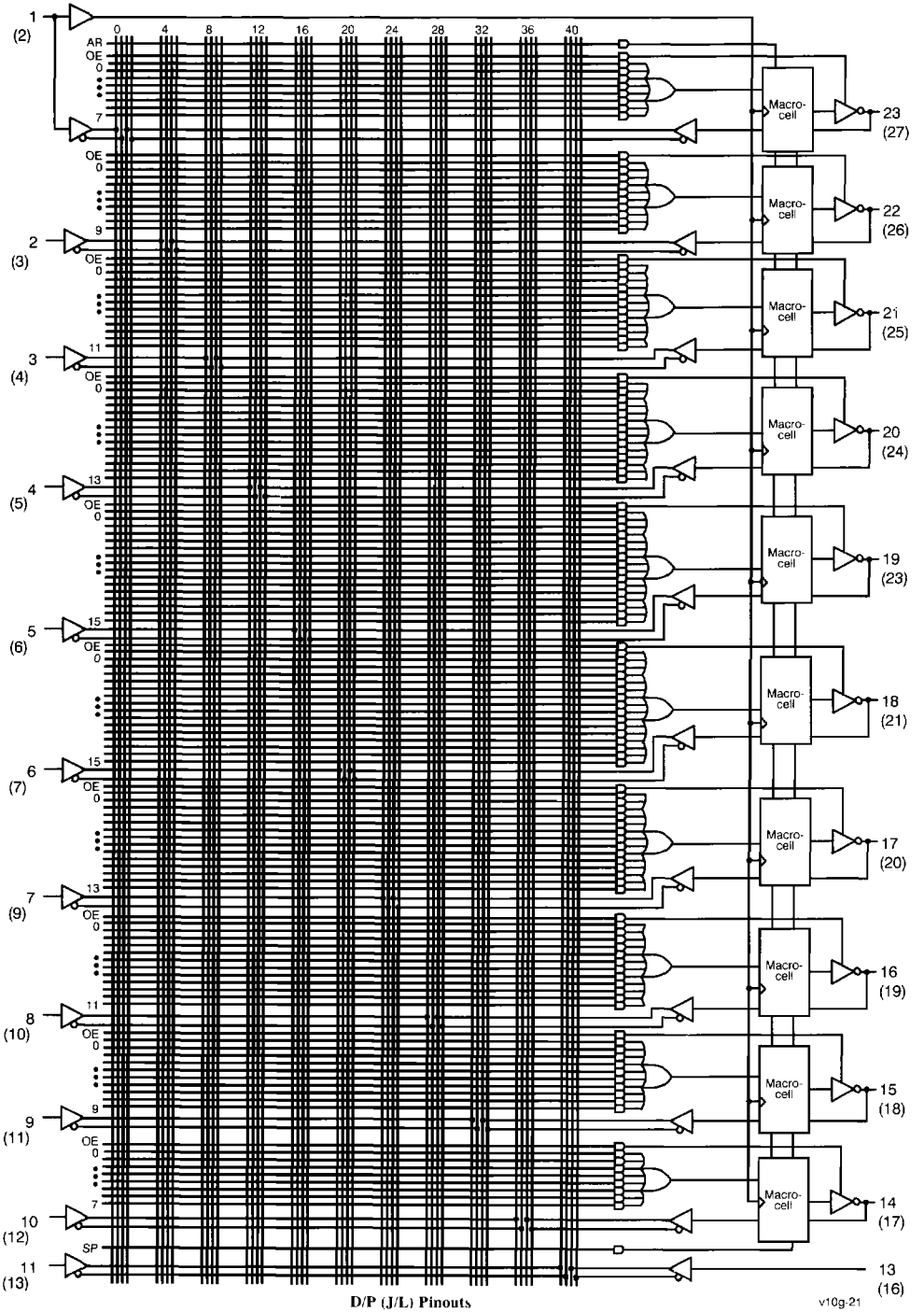


Notes (the numbers in parantheses refer to J and L packages):
16. Pins 4 (5), 5 (6), 7 (9) at V_{ILP}; Pins 10 (12) and 11 (13) at V_{IHP}; V_{CC} (Pin 24 (1 and 28)) at V_{CCP}.
17. Pins 2–8 (3–7, 9, 10), 10 (12), 11 (13) can be set at V_{IHP} or V_{ILP} to insure asynchronous reset is not active.

Forced Level on Register Pin During Preload	Register Q Output State After Preload
V_{IHP}	HIGH
V_{ILP}	LOW

Name	Description	Min.	Max.	Unit
V_{PP}	Programming Voltage	9.25	9.75	V
t_{DPR1}	Delay for Preload	1		µs
t_{DPR2}	Delay for Preload	0.5		µs
V_{ILP}	Input LOW Voltage	0	0.4	V
V_{IHP}	Input HIGH Voltage	3	4.75	V
V_{CCP}	V_{CC} for Preload	4.75	5.25	V

Functional Logic Diagram for PAL22V10G/PAL22VP10G



D/P (J/L) Pinouts

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Ordering Information

I_{CC} (mA)	t_{PD} (ns)	f_{MAX} (MHz)	Ordering Code	Package Name	Package Type	Operating Range
190	4	166	PAL22V10G–4JC	J64	28-Lead Plastic Leaded Chip Carrier	Commercial
	5	153.8	PAL22V10G–5JC	J64	28-Lead Plastic Leaded Chip Carrier	Commercial
	6	117	PAL22V10G–6JC	J64	28-Lead Plastic Leaded Chip Carrier	Commercial
	7.5	111	PAL22V10G–7JC	J64	28-Lead Plastic Leaded Chip Carrier	Commercial
			PAL22V10G–7PC	P13	24-Lead (300-Mil) Molded DIP	
			PAL22V10G–7LMB	L64	28-Pin Square Leadless Chip Carrier	Military
	10	90	PAL22V10G–10JC	J64	28-Lead Plastic Leaded Chip Carrier	
			PAL22V10G–10PC	P13	24-Lead (300-Mil) Molded DIP	
			PAL22V10G–10LMB	L64	28-Pin Square Leadless Chip Carrier	Military

I_{CC} (mA)	t_{PD} (ns)	f_{MAX} (MHz)	Ordering Code	Package Type	Package Type	Operating Range
190	4	166	PAL22VP10G–4JC	J64	28-Lead Plastic Leaded Chip Carrier	Commercial
	5	153.8	PAL22VP10G–5JC	J64	28-Lead Plastic Leaded Chip Carrier	Commercial
	6	117	PAL22VP10G–6JC	J64	28-Lead Plastic Leaded Chip Carrier	Commercial
	7.5	111	PAL22VP10G–7JC	J64	28-Lead Plastic Leaded Chip Carrier	Commercial
			PAL22VP10G–7PC	P13	24-Lead (300-Mil) Molded DIP	
			PAL22VP10G–7LMB	L64	28-Pin Square Leadless Chip Carrier	Military
	10	90	PAL22VP10G–10JC	J64	28-Lead Plastic Leaded Chip Carrier	
			PAL22VP10G–10PC	P13	24-Lead (300-Mil) Molded DIP	
			PAL22VP10G–10LMB	L64	28-Pin Square Leadless Chip Carrier	Military

Shaded area contains advanced information.

MILITARY SPECIFICATIONS

Group A Subgroup Testing

DC Characteristerics

Parameters	Subgroups
V_{OH}	1, 2, 3
V_{OL}	1, 2, 3
V_{IH}	1, 2, 3
V_{IL}	1, 2, 3
I_{IX}	1, 2, 3
I_{OZ}	1, 2, 3
I_{CC}	1, 2, 3

Switching Characteristics

Parameters	Subgroups
t_{PD}	7, 8, 9, 10, 11
t_{CO}	7, 8, 9, 10, 11
t_S	7, 8, 9, 10, 11
t_H	7, 8, 9, 10, 11

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